Chapter 2 System Overview

2.1 Address Mapping

RK3288 support to boot from internal bootrom, which support remap function by software programming. Remap is controlled by SGRF_SOC_CON0 bit[11].

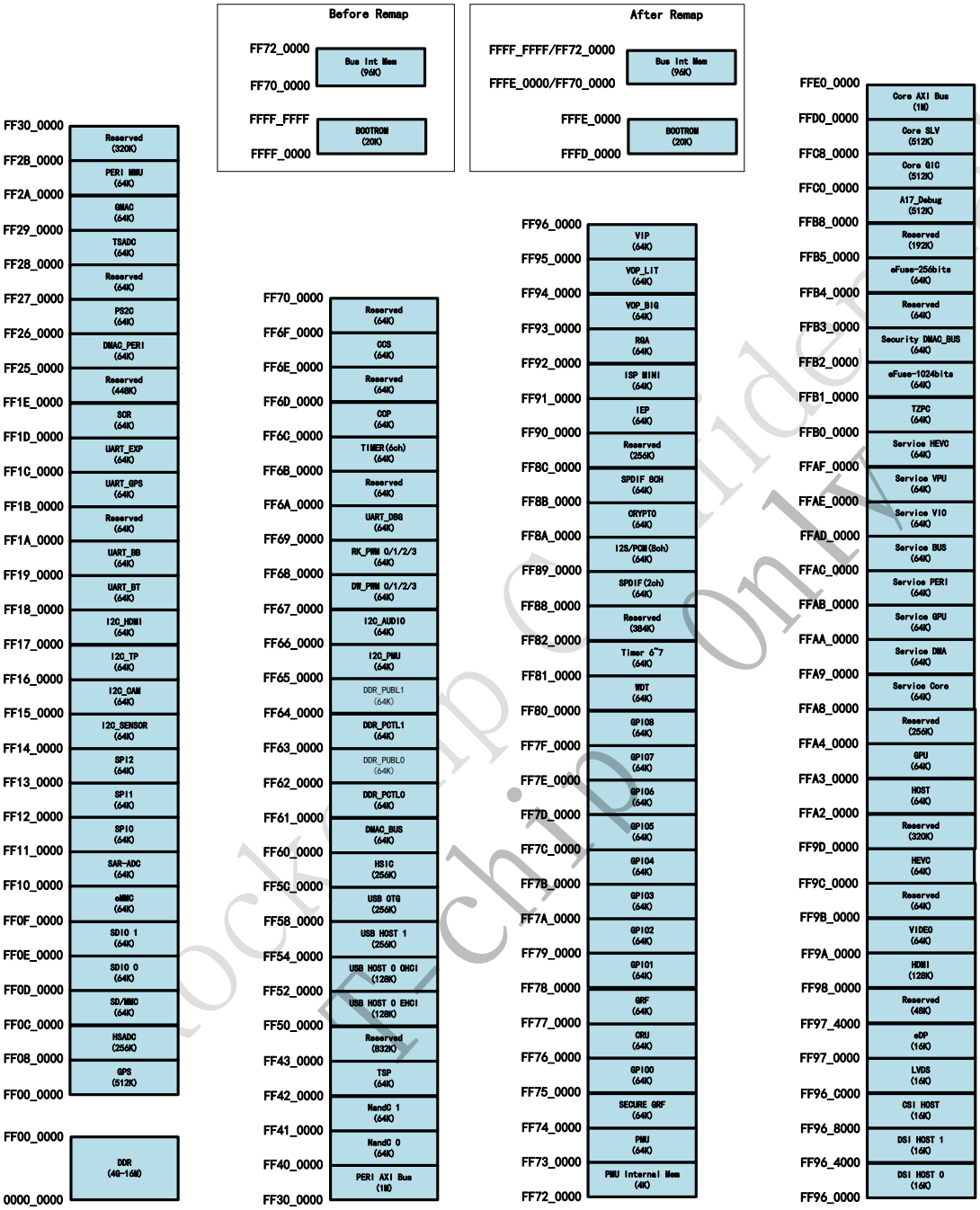

Fig. 2-1 RK3288 Address Mapping

2.2 System Boot

RK3288 provides system boot from off-chip devices such as SDMMC card, 8bits async nand flash or toggle nand flash, SPI nor or nand, and eMMC memory. When boot code is not ready

in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal bootrom. The following is the whole boot procedure for boot code, which will be stored in bootrom in advance.

The following features are supports.

- Support secure boot mode and non-secure boot mode
- Support system boot from the following device:
  - 8bits Async Nand Flash
  - 8bits Toggle Nand Flash
  - SPI2_CS0 interface
  - eMMC interface
  - SDMMC Card
- Support system code download by USB OTG

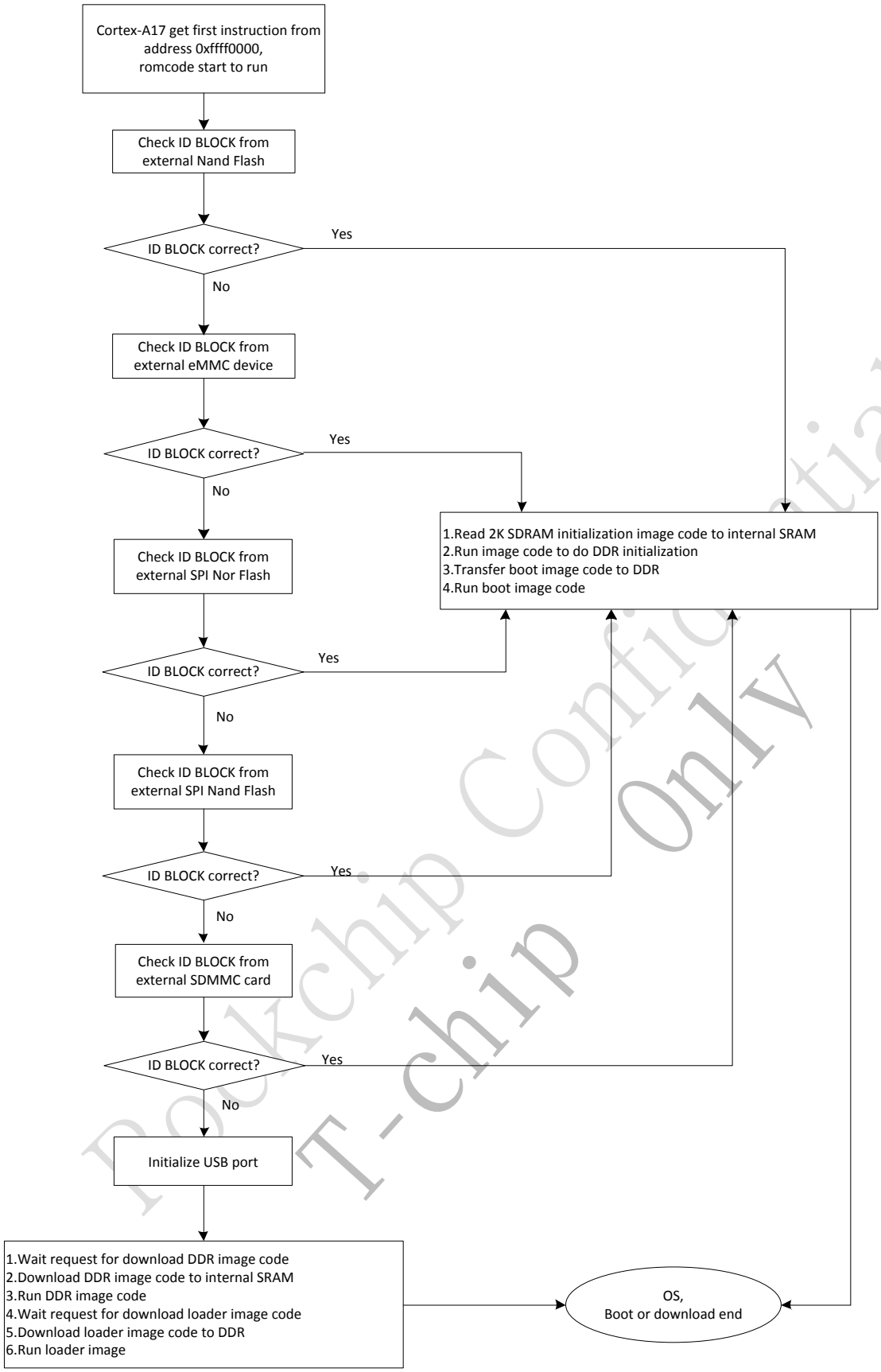

Fig. 2-2 RK3288 boot procedure flow

2.3 System Interrupt connection

RK3288 provides an general interrupt controller(GIC) for Cortex-A17 MPCore processor, which

has 112 SPI (shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupts is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table. For detailed GIC setting, please refer to Chapter 12.

Table 2-1 RK3288 Interrupt connection list

IRQ Type	IRQ ID	Source(spi)	Polarity
PPI	26	HYPERVISOR TIMER	High level
	27	VIRTUAL TIMER	High level
	29	SECURE PHYSICAL TIMER	High level
	30	NON-SECURE PHY TIMER	High level
SPI	32	DMAC_BUS (0)	High level
	33	DMAC_BUS (1)	High level
	34	DMAC_PERI (0)	High level
	35	DMAC_PERI (1)	High level
	36	UPCTL 0	High level
	37	UPCTL 1	High level
	38	GPU_IRQJOB	High level
	39	GPU_IRQMMU	High level
	40	GPU_IRQGPU	High level
	41	VIDEO ENCODER	High level
	42	VIDEO DECODER	High level
	43	VIDEO MMU	High level
	44	HEVC	High level
	45	VIP	High level
	46	ISP	High level
	47	VOP_BIG	High level
	48	VOP_LIT	High level
	49	IEP	High level
	50	RGA	High level
	51	DSI 0 HOST	High level
	52	DSI 1 HOST	High level
	53	CSI HOST 0	High level
	54	CSI HOST 1	High level
	55	USB OTG	High level
	56	USB HOST 0 EHCI	High level
	57	USB HOST 1	High level
	58	HSIC	High level
	59	GMAC	High level
	60	GMAC PMT	High level
	61	GPS	High level
	62	GPS TIMER	High level
	63	HS-ADC/TSI	High level
	64	SD/MMC	High level
	65	SDIO 0	High level
	66	SDIO 1	High level

	67	eMMC	High level
	68	SARADC	High level
	69	TSADC	High level
	70	NANDC 0	High level
	71	PERI MMU	High level
	72	NANDC 1	High level
	73	USB HOST 0 OHCI	High level
	74	TPS	High level
	75	SCR	High level
	76	SPI0	High level
	77	SPI1	High level
	78	SPI2	High level
	79	PS2C	High level
	80	CRYPTO	High level
	81	HOST PULSE 0	High level
	82	HOST PULSE 1	High level
	83	HOST 0	High level
	84	HOST 1	High level
	85	I2S/PCM (8ch)	High level
	86	SPDIF(8ch)	High level
	87	UART_BT	High level
	88	UART_BB	High level
	89	UART_DBG	High level
	90	UART_GPS	High level
	91	UART_EXP	High level
	92	I2C_PMU	High level
	93	I2C_AUDIO	High level
	94	I2C_SENSOR	High level
	95	I2C_CAM	High level
	96	I2C_TP	High level
	97	I2C_HDMI	High level
	98	TIMER 6CH 0	High level
	99	TIMER 6CH 1	High level
	100	TIMER 6CH 2	High level
	101	TIMER 6CH 3	High level
	102	TIMER 6CH 4	High level
	103	TIMER 6CH 5	High level
	104	TIMER 2CH 0	High level
	105	TIMER 2CH 1	High level
	106	PWM0	High level
	107	PWM1	High level
	108	PWM2	High level
	109	PWM3	High level
	110	RK_PWM	High level
	111	WDT	High level

	112	PMU	High level
	113	GPIO0	High level
	114	GPIO1	High level
	115	GPIO2	High level
	116	GPIO3	High level
	117	GPIO4	High level
	118	GPIO5	High level
	119	GPIO6	High level
	120	GPIO7	High level
	121	GPIO8	High level
	122	AHB ARBITER0 (USB)	High level
	123	AHB ARBITER1 (EMEM)	High level
	124	AHB ARBITER2 (MMC)	High level
	125	USBOTG_ID	High level
	126	USBOTG_BVALID	High level
	127	USBOTG_LINESTATE	High level
	128	USBHOST0_LINESTATE	High level
	129	USBHOST1_LINESTATE	High level
	130	eDP DP	High level
	131	SDMMC_DETECT_N	High level
	132	SDIO0_DETECT_N	High level
	133	SDIO1_DETECT_N	High level
	134	HDMI WAKEUP	High level
	135	HDMI	High level
	136	CCP	High level
	137	CCS	High level
	138	SDMMC DETECT DUAL EDGE	High level
	139	GPIO7_B3 DUAL EDGE	High level
	140	GPIO7_C6_DUAL EDGE	High level
	141	GPIO8_A2_DUAL EDGE	High level
	142	eDP HDMI	High level
	143	HEVC MMU	High level
	186	PMUIRQ[0]	High level
	187	PMUIRQ[1]	High level
	188	PMUIRQ[2]	High level
	189	PMUIRQ[3]	High level

2.4 System DMA hardware request connection

RK3288 provides 2 DMA controllers: DMAC_BUS inside bus system and DMAC_PERI inside peripheral system. As for DMAC_BUS, there are 6 hardware request ports. Another, 15 hardware request ports are used in DMAC_PERI, the trigger type for each of them is high level, not programmable. For detailed descriptions of DMAC_BUS and DMAC_PERI, please refer to Chapter 10 and Chapter 11.

Table 2-2 RK3288 DMAC_BUS Hardware request connection list

Req Number	Source	Polarity
0	I2S/PCM(8CH) TX	High level
1	I2S/PCM(8CH) RX	High level
2	SPDIF(2CH) TX	High level
3	SPDIF(8CH) TX	High level
4	UART_DBG TX	High level
5	UART_DBG RX	High level

Table 2-3 RK3288 DMAC_PERI Hardware request connection list

Req Number	Source	Polarity
0	HS-ADC/TSI	High level
1	UART_BT TX	High level
2	UART_BT RX	High level
3	UART_BB TX	High level
4	UART_BB RX	High level
5	N/A	N/A
6	N/A	N/A
7	UART_GPS TX	High level
8	UART_GPS RX	High level
9	UART_EXP TX	High level
10	UART_EXP RX	High level
11	SPI0 TX	High level
12	SPI0 RX	High level
13	SPI1 TX	High level
14	SPI1 RX	High level
15	SPI2 TX	High level
16	SPI2 RX	High level