Chapter 3 Clock & Reset Unit (CRU)

3.1 Overview

The CRU is an APB slave module that is designed for generating all of the system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset.

CRU supports the following features:

- Compliance to the AMBA APB interface
- Embedded five PLLs
- Flexible selection of clock source
- Supports the respective gating of all clocks
- Supports the respective software reset of all modules

3.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

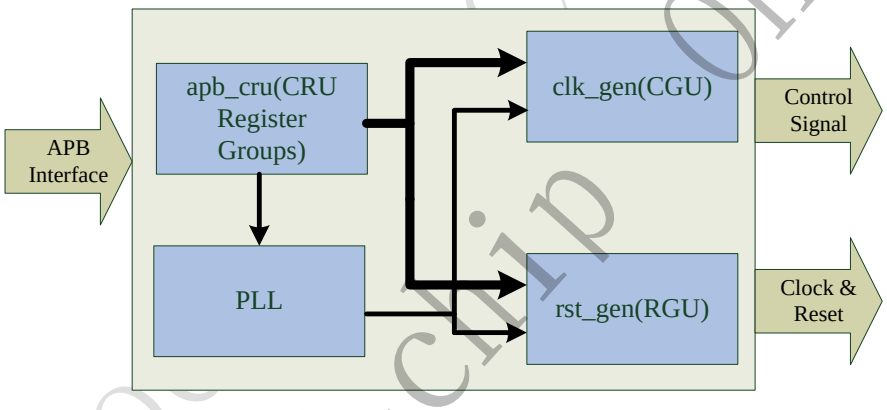

Fig. 3-1 CRU Architecture

3.3 System Clock Solution

3.3.1 CRU architecture

The following diagrams show CRU clock architecture (mux and divider information).

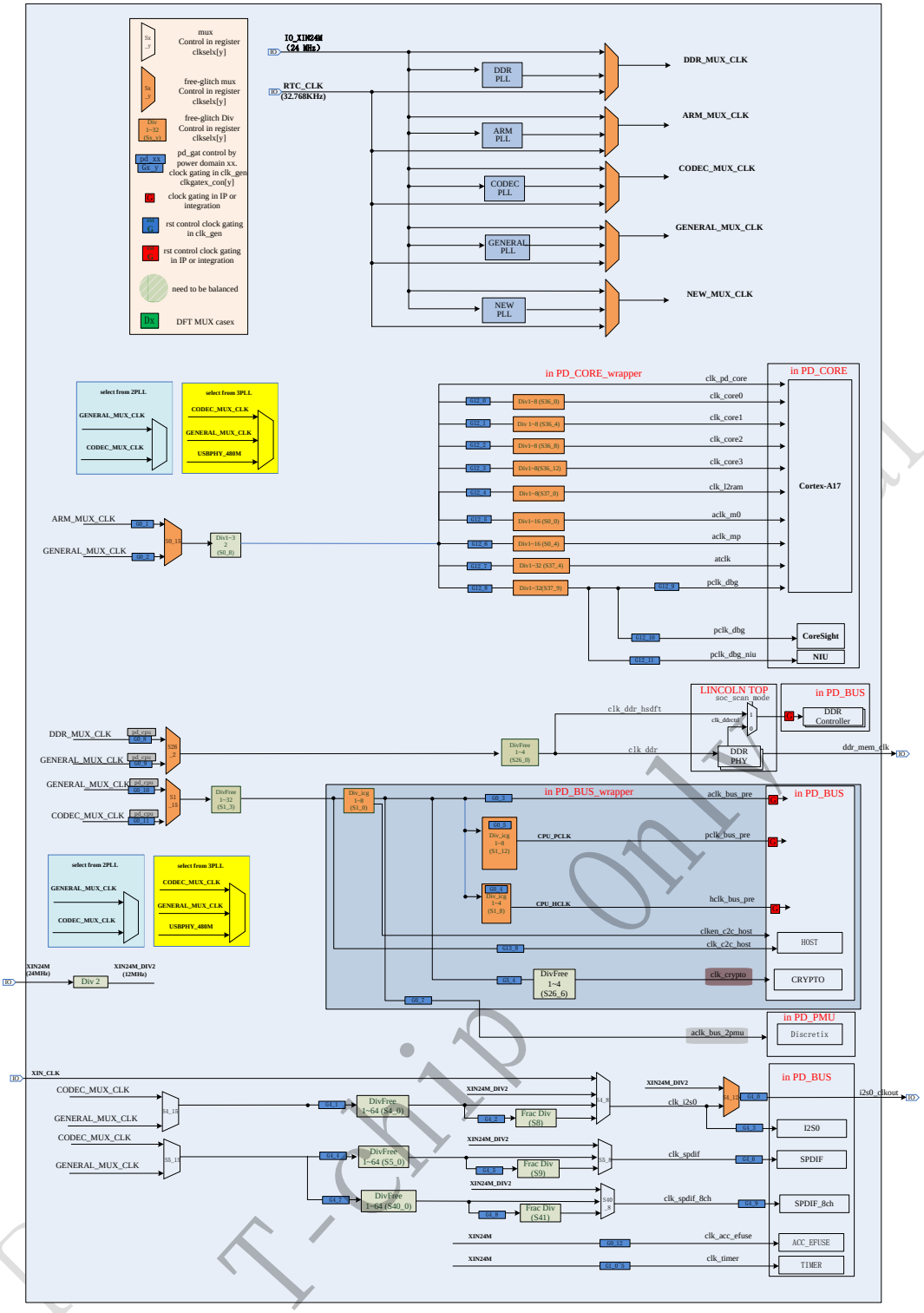

Fig. 3-2 CRU Clock Architecture Diagram 1

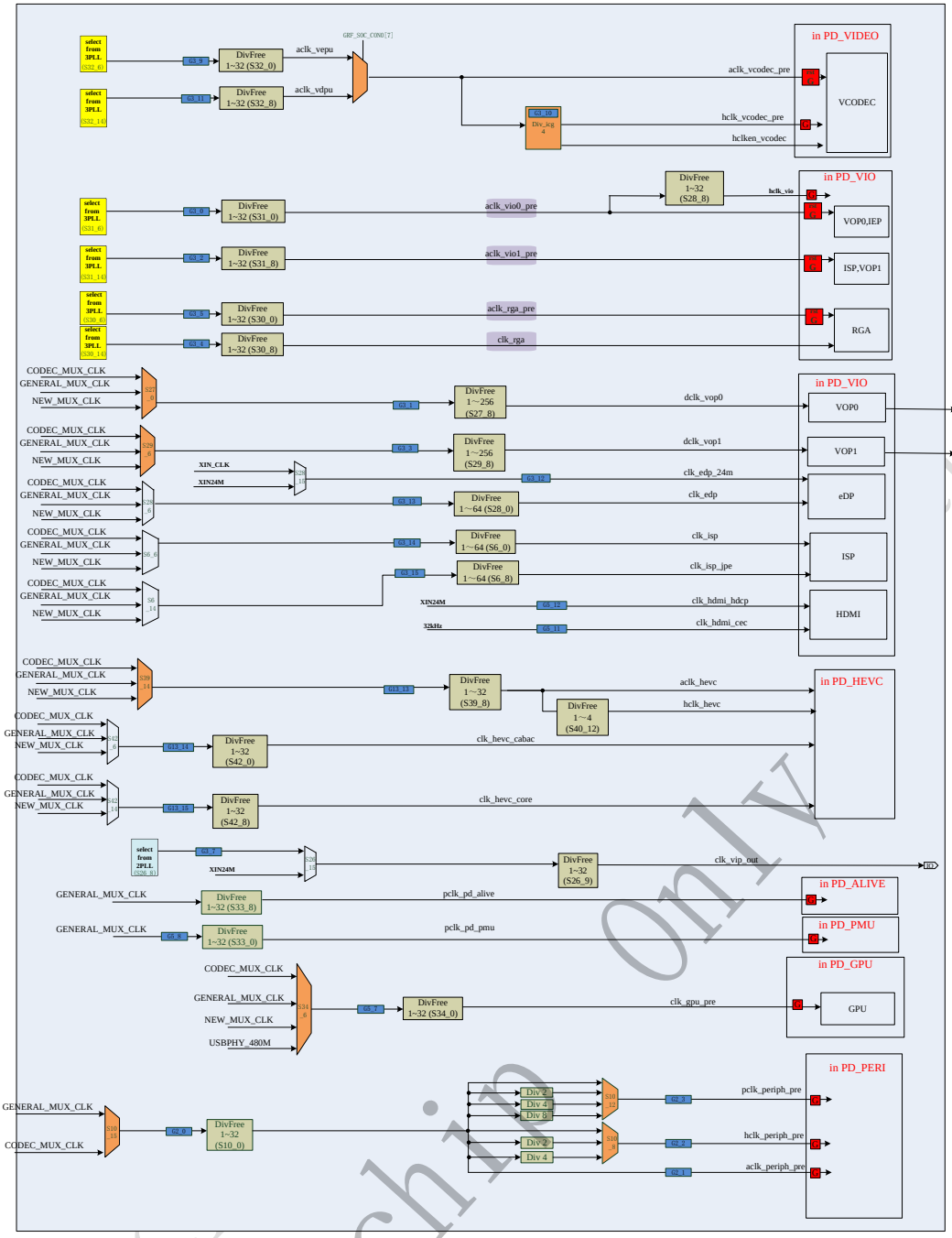

Fig. 3-3 CRU Clock Architecture Diagram 2

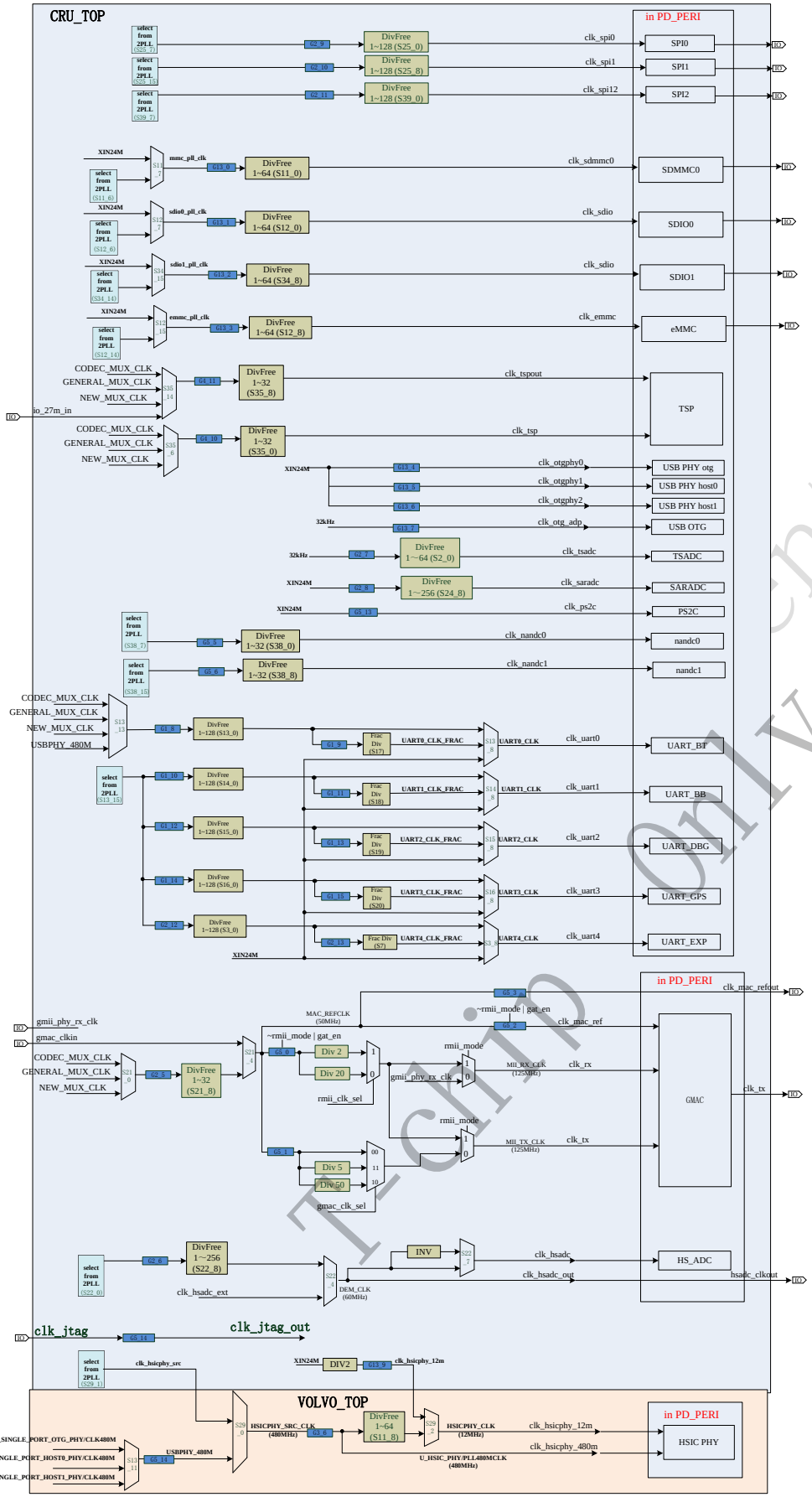

Fig. 3-4 CRU Clock Architecture Diagram 3

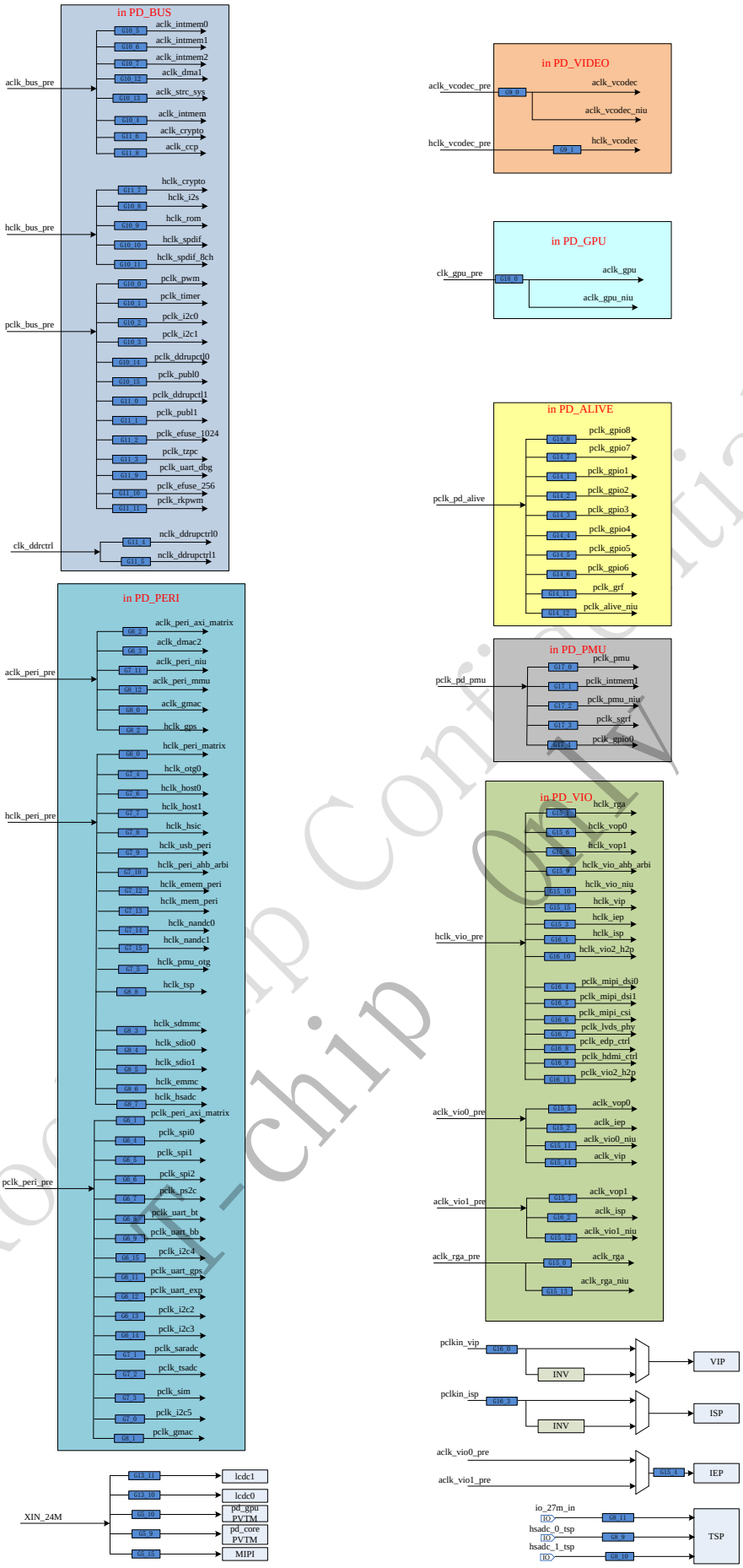

Fig. 3-5 CRU Clock Architecture Diagram 4

3.4 System Reset Solution

The following diagrams show reset architecture in this block.

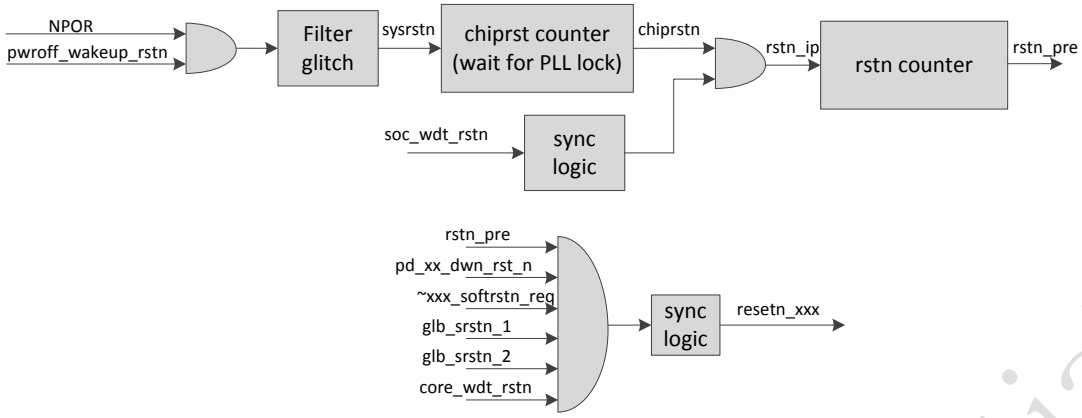

Fig. 3-6 Reset Architecture Diagram

Reset source of each reset signal includes hardware reset (NPOR), power-off mode wakeup reset (pwroff_wakeup_rstn), soc watch dog reset (soc_wdt_rstn), power domain power down reset (pd_xx_dwn_rst_n), software reset request (xxx_softrstn_req), global software reset1 (glb_srstn_1), global software reset2 (glb_srstn_2) and A9 core watch dog reset (core_wdt_rstn).

The 'xx' of pd_xx_dwn_rst_n represents core0, core1, core2, core3, cs, cpu, peri, vio, video or gpu. The 'xxx' of resetn_xxx and xxx_softrstn_req is the module name.

Pwroff_wakeup_rstn is the reset when wakeup from the power-off mode, it will reset the all SOC logic except internal PMU.

Soc_wdt_rstn is the reset from watch-dog IP in the SoC, but core_wdt_rstn is the reset from A9 core watch-dog block.

Glb_srstn_1 and glb_srstn_2 are the global software reset by programming CRU register. When writing register CRU_GLB_SRST_FST_VALUE as 0xfdb9, glb_srstn_1 will be asserted, and when writing register CRU_GLB_SRST_SND_VALUE as 0xeca8, glb_srstn_2 will be asserted. The two software resets will be self-clear by hardware. Glb_srstn_1 will reset the all logic except PMU_SYS_REG0~3. And Glb_srstn_2 will reset the all logic except PMU_SYS_REG0~3, GRF and all GPIOs.

3.5 Function Description

There are five PLLs:

ARM PLL, DDR PLL, CODEC PLL, GENERAL PLL and NEW PLL in CRU.

PLLs all can be set to slow mode or deep slow mode, directly output selectable 24MHz or 32.768kHz. When power on or changing PLL setting, we must force PLL into slow mode to ensure output stable clock.

To maximize the flexibility, some of clocks can select divider source from three PLLs (CODEC PLL, GENERAL PLL and NEW PLL).

To provide some specific frequency, another solution is integrated: fractional divider. In order to be sure the performance for divided clock, there is some usage limit, we can only get low frequency and divider factor must be larger than 20.

All clocks can be software gated and all reset can be software generated.

3.6 PLL Introduction

3.6.1 Overview

This chip uses 2.2GHz PLL for all four PLLs. The 2.2GHz PLL is a general purpose, high-performance PLL-based clock generator. The VCO operates from 440 MHz to 2200MHz. It has a programmable output frequency, which ranges from 27.5 MHz to 2200 MHz configured through a 6-bit input divider, a 13-bit feedback divider and a 4-bit output divider. Around 50% duty cycle of output clocks can be achieved by enabling the output divider. It can also be used as a clock buffer through a bypass mode that bypasses and powers down the PLL. A full power-down mode is also available.

2.2GHz PLL supports the following features:

- Fully integrated, including loop filter
- Power supply: 1.0V single power supply
- VCO operating range: 440MHz – 2200MHz
- Output frequency range: 27.5MHz – 2200MHz
- Input frequency range: 269kHz – 2200MHz
- PFD comparison frequency range: 269kHz – 2200MHz
- Low power consumption: 3mA @ 1100MHz during normal operation
- Contains 6-bit input, 13-bit feedback and 4-bit output dividers
- Input divider value range: 1–64
- Feedback divider value range: 1–4096
- Output divider value range: 1, 2-16 (even only)
- Bandwidth adjustment of div. reference: 1–4096
- Output duty cycle: +/-5% (/1), +/-2% (/N)
- Period jitter (P-P) (max): +/-2.5% output cycle
- Reset pulse width (min): 5us
- Lock time (min allowed): 500 div. reference cycles
- Freq. overshot (full-~/half-~) (max): 40%/50%
- Ref. input jitter (long-term, P-P) (max): 2% div. reference cycle
- Reference H/L pulse width (min) : 230ps
- Bypass and Power-down mode
- Lock detector

3.6.2 Block diagram

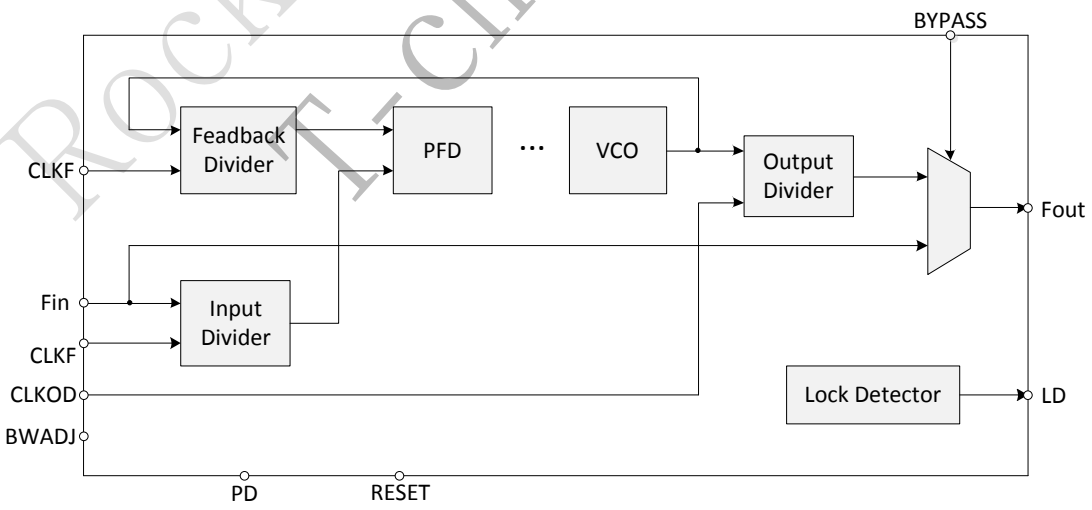

Fig. 3-7 PLL Block Diagram

3.6.3 Operation mode

A. Locked

The positive edges of the PLL feedback and reference signals are phase aligned in normal operation. Because the feedback signal is internal, NO phase relationship is guaranteed between RCLK and CLKOUT. The output clock frequency is programmable through the divider setting of CLKR[5:0], CLKF[12:0] and CLKOD[3:0].

B. Reset (RESET=1)

The PLL outputs a fixed free-running frequency in the range of 20MHz to 200MHz for a divide by 1 output depending on the specific PLL type.

C. Power-down (PWRDN=1)

All analog circuitry in the PLL is turned off so as to only dissipate leakage current. The digital dividers are not affected.

D. Bypass (BYPASS=1)

The reference input is bypassed directly to the outputs.

E. Test (TEST=1)

The reference input drives all dividers cascaded one after the other for production testing.

3.6.4 PLL Bandwidth Adjustment

The loop bandwidth (BW) of the PLL can be adjusted using BWADJ[11:0]. The bandwidth is given by: BW = nom_BW*sqrt(NF / 2 / NB), where nom_BW is approximately given by: nom_BW = Fref / (NR*20), and Fref is the reference clock frequency. The damping factor (D) is approximately given by: D = nom_D*sqrt(NF / 2 / NB), where nom_D is approximately 1. Because the damping factor changes with bandwidth settings, the bandwidth is practically limited to: nom_BW/sqrt(2) < BW < nom_BW*sqrt(2), in order to limit the damping factor range to 0.7 - 1.4. The -3dB bandwidth (Fbw_3dB) is approximately given by: Fbw_3dB = 2.4 * nom_BW * (NF / 2 / NB). The recommended setting for NB is NF / 2, which will yield the nominal bandwidth. Note that nom_BW and nom_D are chosen to result in optimal PLL loop dynamics.

3.7 Register Description

This section describes the control/status registers of the design.

3.7.1 CRU Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_APLL_CON0	0x0000	W	0x00000b01	ARM PLL configuration register0
CRU_APLL_CON1	0x0004	W	0x000003e7	ARM PLL configuration register1
CRU_APLL_CON2	0x0008	W	0x000001f3	ARM PLL configuration register2

Name	Offset	Size	Reset Value	Description
CRU_APLL_CON3	0x000c	W	0x00000008	ARM PLL configuration register3
CRU_DPLL_CON0	0x0010	W	0x00000b03	DDR PLL configuration register0
CRU_DPLL_CON1	0x0014	W	0x0000031f	DDR PLL configuration register1
CRU_DPLL_CON2	0x0018	W	0x0000018f	DDR PLL configuration register2
CRU_DPLL_CON3	0x001c	W	0x00000008	DDR PLL configuration register3
CRU_CPLL_CON0	0x0020	W	0x00000b03	CODEC PLL configuration register0
CRU_CPLL_CON1	0x0024	W	0x000002ff	CODEC PLL configuration register1
CRU_CPLL_CON2	0x0028	W	0x0000017f	CODEC PLL configuration register2
CRU_CPLL_CON3	0x002c	W	0x00000008	CODEC PLL configuration register3
CRU_GPLL_CON0	0x0030	W	0x00000b01	GENERAL PLL configuration register0
CRU_GPLL_CON1	0x0034	W	0x00000251	GENERAL PLL configuration register1
CRU_GPLL_CON2	0x0038	W	0x00000128	GENERAL PLL configuration register2
CRU_GPLL_CON3	0x003c	W	0x00000008	GENERAL PLL configuration register3
CRU_NPLL_CON0	0x0040	W	0x00000b03	NEW PLL configuration register0
CRU_NPLL_CON1	0x0044	W	0x000003e7	NEW PLL configuration register1
CRU_NPLL_CON2	0x0048	W	0x000001f3	NEW PLL configuration register2
CRU_NPLL_CON3	0x004c	W	0x00000008	NEW PLL configuration register3
CRU_MODE_CON	0x0050	W	0x00000000	System work mode control register
CRU_CLKSEL0_CON	0x0060	W	0x00000031	Internal clock select and divide register0
CRU_CLKSEL1_CON	0x0064	W	0x0000b109	Internal clock select and divide register1
CRU_CLKSEL2_CON	0x0068	W	0x00000020	Internal clock select and divide register2
CRU_CLKSEL3_CON	0x006c	W	0x00000200	Internal clock select and divide register3

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL4_CON	0x0070	W	0x00000300	Internal clock select and divide register4
CRU_CLKSEL5_CON	0x0074	W	0x00000200	Internal clock select and divide register5
CRU_CLKSEL6_CON	0x0078	W	0x00000101	Internal clock select and divide register6
CRU_CLKSEL7_CON	0x007c	W	0x0bb8ea60	Internal clock select and divide register7
CRU_CLKSEL8_CON	0x0080	W	0x0bb8ea60	Internal clock select and divide register8
CRU_CLKSEL9_CON	0x0084	W	0x0bb8ea60	Internal clock select and divide register9
CRU_CLKSEL10_CON	0x0088	W	0x0000a101	Internal clock select and divide register10
CRU_CLKSEL11_CON	0x008c	W	0x00002780	Internal clock select and divide register11
CRU_CLKSEL12_CON	0x0090	W	0x00008080	Internal clock select and divide register12
CRU_CLKSEL13_CON	0x0094	W	0x00000200	Internal clock select and divide register13
CRU_CLKSEL14_CON	0x0098	W	0x00000200	Internal clock select and divide register14
CRU_CLKSEL15_CON	0x009c	W	0x00000200	Internal clock select and divide register15
CRU_CLKSEL16_CON	0x00a0	W	0x00000200	Internal clock select and divide register16
CRU_CLKSEL17_CON	0x00a4	W	0x0bb8ea60	Internal clock select and divide register17
CRU_CLKSEL18_CON	0x00a8	W	0x0bb8ea60	Internal clock select and divide register18
CRU_CLKSEL19_CON	0x00ac	W	0x0bb8ea60	Internal clock select and divide register19
CRU_CLKSEL20_CON	0x00b0	W	0x0bb8ea60	Internal clock select and divide register20
CRU_CLKSEL21_CON	0x00b4	W	0x00000b00	Internal clock select and divide register21
CRU_CLKSEL22_CON	0x00b8	W	0x00000900	Internal clock select and divide register22
CRU_CLKSEL23_CON	0x00bc	W	0x001f05dc	Internal clock select and divide register23
CRU_CLKSEL24_CON	0x00c0	W	0x00001700	Internal clock select and divide register24
CRU_CLKSEL25_CON	0x00c4	W	0x00000707	Internal clock select and divide register25

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL26_CON	0x00c8	W	0x00000ec0	Internal clock select and divide register26
CRU_CLKSEL27_CON	0x00cc	W	0x00000700	Internal clock select and divide register27
CRU_CLKSEL28_CON	0x00d0	W	0x00000f03	Internal clock select and divide register28
CRU_CLKSEL29_CON	0x00d4	W	0x00000742	Internal clock select and divide register29
CRU_CLKSEL30_CON	0x00d8	W	0x00000000	Internal clock select and divide register30
CRU_CLKSEL31_CON	0x00dc	W	0x00000000	Internal clock select and divide register31
CRU_CLKSEL32_CON	0x00e0	W	0x00000101	Internal clock select and divide register32
CRU_CLKSEL33_CON	0x00e4	W	0x00000303	Internal clock select and divide register33
CRU_CLKSEL34_CON	0x00e8	W	0x00008000	Internal clock select and divide register34
CRU_CLKSEL35_CON	0x00ec	W	0x00000303	Internal clock select and divide register35
CRU_CLKSEL36_CON	0x00f0	W	0x00000000	Internal clock select and divide register36
CRU_CLKSEL37_CON	0x00f4	W	0x00001ef3	Internal clock select and divide register37
CRU_CLKSEL38_CON	0x00f8	W	0x00000303	Internal clock select and divide register38
CRU_CLKSEL39_CON	0x00fc	W	0x00000007	Internal clock select and divide register39
CRU_CLKSEL40_CON	0x0100	W	0x00000200	Internal clock select and divide register40
CRU_CLKSEL41_CON	0x0104	W	0x0bb8ea60	Internal clock select and divide register41
CRU_CLKSEL42_CON	0x0108	W	0x00000000	Internal clock select and divide register42
CRU_CLKGATE0_CON	0x0160	W	0x00000000	Internal clock gating control register0
CRU_CLKGATE1_CON	0x0164	W	0x00000000	Internal clock gating control register1
CRU_CLKGATE2_CON	0x0168	W	0x00000000	Internal clock gating control register2
CRU_CLKGATE3_CON	0x016c	W	0x00000000	Internal clock gating control register3
CRU_CLKGATE4_CON	0x0170	W	0x00000000	Internal clock gating control register4

Name	Offset	Size	Reset Value	Description
CRU_CLKGATE5_CON	0x0174	W	0x00000000	Internal clock gating control register5
CRU_CLKGATE6_CON	0x0178	W	0x00000000	Internal clock gating control register6
CRU_CLKGATE7_CON	0x017c	W	0x00000000	Internal clock gating control register7
CRU_CLKGATE8_CON	0x0180	W	0x00000000	Internal clock gating control register8
CRU_CLKGATE9_CON	0x0184	W	0x00000000	Internal clock gating control register9
CRU_CLKGATE10_CON	0x0188	W	0x00000000	Internal clock gating control register10
CRU_CLKGATE11_CON	0x018c	W	0x00000000	Internal clock gating control register11
CRU_CLKGATE12_CON	0x0190	W	0x00000000	Internal clock gating control register12
CRU_CLKGATE13_CON	0x0194	W	0x00000000	Internal clock gating control register13
CRU_CLKGATE14_CON	0x0198	W	0x00000000	Internal clock gating control register14
CRU_CLKGATE15_CON	0x019c	W	0x00000000	Internal clock gating control register15
CRU_CLKGATE16_CON	0x01a0	W	0x00000000	Internal clock gating control register16
CRU_CLKGATE17_CON	0x01a4	W	0x00000000	Internal clock gating control register17
CRU_CLKGATE18_CON	0x01a8	W	0x00000000	Internal clock gating control register18
CRU_GLB_SRST_FST_VALUE	0x01b0	W	0x00000000	The first global software reset config value
CRU_GLB_SRST_SND_VALUE	0x01b4	W	0x00000000	The second global software reset config value
CRU_SOFTRST0_CON	0x01b8	W	0x00000000	Internal software reset control register0
CRU_SOFTRST1_CON	0x01bc	W	0x00000000	Internal software reset control register1
CRU_SOFTRST2_CON	0x01c0	W	0x00000000	Internal software reset control register2
CRU_SOFTRST3_CON	0x01c4	W	0x00000000	Internal software reset control register3
CRU_SOFTRST4_CON	0x01c8	W	0x00000000	Internal software reset control register4
CRU_SOFTRST5_CON	0x01cc	W	0x00000000	Internal software reset control register5

Name	Offset	Size	Reset Value	Description
CRU_SOFTRST6_CON	0x01d0	W	0x00000000	Internal software reset control register6
CRU_SOFTRST7_CON	0x01d4	W	0x00000000	Internal software reset control register7
CRU_SOFTRST8_CON	0x01d8	W	0x00000000	Internal software reset control register8
CRU_SOFTRST9_CON	0x01dc	W	0x00000000	Internal software reset control register9
CRU_SOFTRST10_CON	0x01e0	W	0x00000000	Internal software reset control register10
CRU_SOFTRST11_CON	0x01e4	W	0x00000000	Internal software reset control register11
CRU_MISC_CON	0x01e8	W	0x00000000	SCU control register
CRU_GLB_CNT_TH	0x01ec	W	0x00000064	global reset wait counter threshold
CRU_GLB_RST_CON	0x01f0	W	0x00000000	global reset trigger select
CRU_GLB_RST_ST	0x01f8	W	0x00000000	global reset status
CRU_SDMMC_CON0	0x0200	W	0x00000002	sdmmc control0
CRU_SDMMC_CON1	0x0204	W	0x00000000	sdmmc control1
CRU_SDIO0_CON0	0x0208	W	0x00000002	sdio0 control0
CRU_SDIO0_CON1	0x020c	W	0x00000000	sdio0 control1
CRU_SDIO1_CON0	0x0210	W	0x00000002	sdio1 control0
CRU_SDIO1_CON1	0x0214	W	0x00000000	sdio1 control1
CRU_EMMC_CON0	0x0218	W	0x00000002	emmc control0
CRU_EMMC_CON1	0x021c	W	0x00000000	emmc control1

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

3.7.2 Detail Register Description

CRU_APLL_CON0
Address: Operational Base + offset (0x0000)
ARM PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKF + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x1	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_APLL_CON1
Address: Operational Base + offset (0x0004)
ARM PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x03e7	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_APLL_CON2
Address: Operational Base + offset (0x0008)
ARM PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x1f3	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_APLL_CON3
Address: Operational Base + offset (0x000c)
ARM PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode

Bit	Attr	Reset Value	Description
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_DPLL_CON0
Address: Operational Base + offset (0x0010)
DDR PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKF + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_DPLL_CON1
Address: Operational Base + offset (0x0014)
DDR PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x031f	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_DPLL_CON2
Address: Operational Base + offset (0x0018)
DDR PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x18f	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_DPLL_CON3
Address: Operational Base + offset (0x001c)
DDR PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down

Bit	Attr	Reset Value	Description
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_CPLL_CON0
Address: Operational Base + offset (0x0020)
CODEC PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKF + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_CPLL_CON1
Address: Operational Base + offset (0x0024)
CODEC PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x02ff	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_CPLL_CON2
Address: Operational Base + offset (0x0028)
CODEC PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x17f	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_CPLL_CON3
Address: Operational Base + offset (0x002c)
CODEC PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_GPLL_CON0
Address: Operational Base + offset (0x0030)
GENERAL PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKF + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x1	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_GPLL_CON1
Address: Operational Base + offset (0x0034)
GENERAL PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x0251	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_GPLL_CON2
Address: Operational Base + offset (0x0038)
GENERAL PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x128	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_GPLL_CON3

Address: Operational Base + offset (0x003c)

GENERAL PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_NPLL_CON0
Address: Operational Base + offset (0x0040)
NEW PLL configuration register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	clkr_mask CLKR value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
23:20	RO	0x0	reserved
19:16	WO	0x0	clkod_mask Clock OD value write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0b	clkr PLL CLKR factor control NR = CLKF + 1 NR: 1-64
7:4	RO	0x0	reserved
3:0	RW	0x3	clkod PLL CLKOD factor control NO = CLKOD + 1 NO: 1, 2-16 (even only)

CRU_NPLL_CON1
Address: Operational Base + offset (0x0044)
NEW PLL configuration register1

Bit	Attr	Reset Value	Description
31	RW	0x0	lock PLL lock status 1'b0: unlock 1'b1: lock
30:13	RO	0x0	reserved
12:0	RW	0x03e7	clkf PLL CLKF factor control NF = CLKF + 1 NF: 1-4096

CRU_NPLL_CON2
Address: Operational Base + offset (0x0048)
NEW PLL configuration register2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x1f3	bwadj PLL loop bandwidth adjust NB = BWADJ + 1

CRU_NPLL_CON3
Address: Operational Base + offset (0x004c)
NEW PLL configuration register3

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	WO	0x0	reset_mask Reset configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
20	WO	0x0	test_mask Test configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
19	WO	0x0	ensat_mask Ensat configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
18	WO	0x0	fasten_mask Fasten configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
17	WO	0x0	power_down_mask Power down configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
16	WO	0x0	bypass_mask Bypass configuration write mask. When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reset PLL reset control 1'b0: normal 1'b1: reset
4	RW	0x0	test PLL test control 1'b0: normal 1'b1: test mode
3	RW	0x1	ensat PLL saturation behavior enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
2	RW	0x0	fasten PLL enable fast locking circuit 1'b0: disable 1'b1: enable
1	RW	0x0	power_down PLL power down control 1'b0: no power down 1'b1: power down
0	RW	0x0	bypass PLL bypass mode control 1'b0: no bypass 1'b1: bypass

CRU_MODE_CON
Address: Operational Base + offset (0x0050)
System work mode control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	npll_work_mode NEW PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
13:12	RW	0x0	gpll_work_mode GENERAL PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
11:10	RO	0x0	reserved
9:8	RW	0x0	cpll_work_mode CODEC PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:4	RW	0x0	dpll_work_mode DDR PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
3:2	RO	0x0	reserved
1:0	RW	0x0	apll_work_mode ARM PLL work mode select 2'b00: Slow mode, clock from external 24MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz

CRU_CLKSEL0_CON
Address: Operational Base + offset (0x0060)
Internal clock select and divide register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	core_clk_pll_sel CORE clock pll source selection 1'b0: select ARM PLL 1'b1: select GENERAL PLL
14:13	RO	0x0	reserved
12:8	RW	0x00	a17_core_div_con Control A17 core clock divider frequency clk_core=clk_src/(div_con+1)
7:4	RW	0x3	aclk_core_mp_div_con Control core MP AXI clock divider frequency clk=clk_src/(div_con+1)
3:0	RW	0x1	aclk_core_m0_div_con Control core M0 AXI clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL1_CON
Address: Operational Base + offset (0x0064)
Internal clock select and divide register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	bus_aclk_pll_sel pd_bus axi clock pll source selection 1'b0: select CODEC PLL 1'b1: select GENERAL PLL
14:12	RW	0x3	pd_bus_pclk_div_con Control pd_bus APB clock divider frequency clk=clk_src/(div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x1	pd_bus_hclk_div_con Control pd_bus AHB clock divider frequency 2'b00: aclk_bus:hclk_bus = 1:1 2'b01: aclk_bus:hclk_bus = 2:1 2'b11: aclk_bus:hclk_bus = 4:1
7:3	RW	0x01	pd_bus_aclk_div_con Control pd_bus aclk divider frequency clk=clk_src/(div_con+1)
2:0	RW	0x1	pd_bus_clk_div_con1 Control pd_bus AXI clock divider1 frequency clk=clk_src/(div_con+1)

CRU_CLKSEL2_CON

Address: Operational Base + offset (0x0068)

Internal clock select and divide register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	testout_div_con test out clk divider frequency clk_testout=testout_clk_src/(testout_div_con+1)
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x20	tsadc_div_con Control tsadc divider frequency clk_tsadc=tsadc_clk_src/(tsadc_div_con+1)

CRU_CLKSEL3_CON
Address: Operational Base + offset (0x006c)
Internal clock select and divide register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart4_clk_sel Control UART4 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart4_div_con Control UART4 divider frequency clk_uart0=uart_clk_src/(uart0_div_con+1)

CRU_CLKSEL4_CON
Address: Operational Base + offset (0x0070)
Internal clock select and divide register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	i2s_pll_sel Control I2S PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x0	i2s0_outclk_sel Control I2S clock work frequency selection 1'b0: select clk_i2s 1'b1: select 12MHz
11:10	RO	0x0	reserved
9:8	RW	0x3	i2s0_clk_sel Control I2S clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select clock from IO input 2'b11: select 12MHz from osc input
7	RO	0x0	reserved
6:0	RW	0x00	i2s0_pll_div_con Control I2S PLL output divider freuency i2s1_div_clk=i2s1_div_src/(i2s1_pll_div_con+1)

CRU_CLKSEL5_CON
Address: Operational Base + offset (0x0074)
Internal clock select and divide register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	spdif_pll_sel Control SPDIF PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:10	RO	0x0	reserved
9:8	RW	0x2	spdif_clk_sel Control SPDIF clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 12MHz from osc inpu
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	spdif_pll_div_con Control SPDIF PLL output divider freuency spdif_div_clk=spdif_div_src/(spdif_pll_div_con+1)

CRU_CLKSEL6_CON
Address: Operational Base + offset (0x0078)
Internal clock select and divide register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	isp_jpeg_pll_sel Control ISP jpeg PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13:8	RW	0x01	isp_jpeg_div_con Control isp jpeg divider freuency jpeg_div_clk=jpeg_div_src/(isp_jpeg_div_con+1)
7:6	RW	0x0	isp_pll_sel Control ISP PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5:0	RW	0x01	isp_div_con Control isp divider freuency isp_div_clk=isp_div_src/(isp_pll_div_con+1)

CRU_CLKSEL7_CON
Address: Operational Base + offset (0x007c)
Internal clock select and divide register7

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart4_frac_factor Control uart4 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL8_CON

Address: Operational Base + offset (0x0080)
Internal clock select and divide register8

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	i2s0_frac_factor Control I2S fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL9_CON
Address: Operational Base + offset (0x0084)
Internal clock select and divide register9

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	spdif_frac_factor Control SPDIF fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL10_CON
Address: Operational Base + offset (0x0088)
Internal clock select and divide register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	peri_pll_sel Control peripheral clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14	RO	0x0	reserved
13:12	RW	0x2	peri_pclk_div_con Control the divider ratio between aclk_periph and pclk_periph 2'b00: aclk_periph:pclk_periph = 1:1 2'b01: aclk_periph:pclk_periph = 2:1 2'b10: aclk_periph:pclk_periph = 4:1 2'b11: aclk_periph:pclk_periph = 8:1
11:10	RO	0x0	reserved
9:8	RW	0x1	peri_hclk_div_con Control the divider ratio between aclk_periph and hclk_periph 2'b00: aclk_periph:hclk_periph = 1:1 2'b01: aclk_periph:hclk_periph = 2:1 2'b10: aclk_periph:hclk_periph = 4:1

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4:0	RW	0x01	peri_aclk_div_con Control periphral clock divider frequency aclk_periph=periph_clk_src/(peri_aclk_div_con+1)

CRU_CLKSEL11_CON
Address: Operational Base + offset (0x008c)
Internal clock select and divide register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x27	hsicphy_div_con Control HSICPHY divider frequency clk_hsicphy_12m=clk_hsicphy_480m/(hsicphy_div_con+1)
7:6	RW	0x2	mmc0_pll_sel Control mmc0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
5:0	RW	0x00	mmc0_div_con Control SDMMC0 divider frequency clk_sdmmc0=general_pll_clk/(mmc0_div_con+1)

CRU_CLKSEL12_CON
Address: Operational Base + offset (0x0090)
Internal clock select and divide register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x2	emmc_pll_sel Control emmc clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
13:8	RW	0x00	emmc_div_con Control EMMC divider frequency clk_emmc=general_pll_clk/(emmc_div_con+1)
7:6	RW	0x2	sdio0_pll_sel Control sdio0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
5:0	RW	0x00	sdio0_div_con Control SDIO0 divider frequency clk_sdio=general_pll_clk/(sdio_div_con+1)

CRU_CLKSEL13_CON
Address: Operational Base + offset (0x0094)
Internal clock select and divide register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	uart_pll_sel Control UART1~4 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RW	0x0	uart0_src_sel UART0 clock source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 480M USBPHY clock 2'b11: select new pll clock
12:11	RW	0x0	usbphy_480m_sel USBPHY 480M clock source selection 2'b00: select HOST0 USB pll clock 2'b01: select HOST1 USB pll clock 2'b10: select OTG USB pll clock
10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RW	0x2	uart0_clk_sel Control UART0 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart0_div_con Control UART0 divider frequency clk_uart0=uart_clk_src/(uart0_div_con+1)

CRU_CLKSEL14_CON
Address: Operational Base + offset (0x0098)
Internal clock select and divide register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart1_clk_sel Control UART1 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart1_div_con Control UART1 divider frequency clk_uart1=uart_clk_src/(uart1_div_con+1)

CRU_CLKSEL15_CON
Address: Operational Base + offset (0x009c)
Internal clock select and divide register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:10	RO	0x0	reserved
9:8	RW	0x2	uart2_clk_sel Control UART2 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart2_div_con Control UART2 divider frequency clk_uart2=uart_clk_src/(uart2_div_con+1)

CRU_CLKSEL16_CON
Address: Operational Base + offset (0x00a0)
Internal clock select and divide register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart3_clk_sel Control UART3 clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	uart3_div_con Control UART3 divider frequency clk_uart3=uart_clk_src/(uart3_div_con+1)

CRU_CLKSEL17_CON
Address: Operational Base + offset (0x00a4)
Internal clock select and divide register17

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart0_frac_factor Control UART0 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL18_CON
Address: Operational Base + offset (0x00a8)
Internal clock select and divide register18

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart1_frac_factor Control UART1 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL19_CON
Address: Operational Base + offset (0x00ac)
Internal clock select and divide register19

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart2_frac_factor Control UART2 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL20_CON
Address: Operational Base + offset (0x00b0)
Internal clock select and divide register20

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart3_frac_factor Control UART3 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL21_CON
Address: Operational Base + offset (0x00b4)
Internal clock select and divide register21

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x0b	mac_div_con Control EMAC divider frequency clk_mac_ref=mac_clk_src/(mac_div_con+1)
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	rmii_extclk_sel Control RMII external clock selection 1'b0: select internal divider clock 1'b1: select external input clock
3:2	RO	0x0	reserved
1:0	RW	0x0	mac_pll_sel Control EMAC clock PLL source selection 2'b00: select new pll clock 2'b01: select codec pll clock 2'b10: select general pll clock

CRU_CLKSEL22_CON
Address: Operational Base + offset (0x00b8)
Internal clock select and divide register22

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x09	hsadc_div_con Control HSADC divider frequency clk_hsadc=hsadc_clk_src/(hsadc_div_con+1)
7	RW	0x0	hsadc_inv_sel Control HSADC inverter clock 1'b0: select buffer output 1'b1: select inverter output
6:5	RO	0x0	reserved
4	RW	0x0	hsadc_clk_sel Control HSADC clock work frequency selection 1'b0: select divider ouput from pll divider 1'b1: select external input clock
3:2	RO	0x0	reserved
1	RW	0x0	wifi_pll_sel Control wifi clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
0	RW	0x0	hsadc_pll_sel Control HSADC clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock

CRU_CLKSEL23_CON
Address: Operational Base + offset (0x00bc)
Internal clock select and divide register23

Bit	Attr	Reset Value	Description
31:0	RW	0x001f05dc	wifi_frac_factor Control wifi fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL24_CON
Address: Operational Base + offset (0x00c0)
Internal clock select and divide register24

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x17	saradc_div_con Control SARADC clock divider frequency clk_saradc=24MHz/(saradc_div_con+1)
7:0	RO	0x0	reserved

CRU_CLKSEL25_CON
Address: Operational Base + offset (0x00c4)
Internal clock select and divide register25

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	spi1_pll_sel Control spi1 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:8	RW	0x07	spi1_div_con Control SPI1 clock divider frequency clk_spi1=general_pll_clk/(spi1_div_con+1)
7	RW	0x0	spi0_pll_sel Control spi0 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock

Bit	Attr	Reset Value	Description
6:0	RW	0x07	spi0_div_con Control SPI0 clock divider frequency clk_spi0=general_pll_clk/(spi0_div_con+1)

CRU_CLKSEL26_CON
Address: Operational Base + offset (0x00c8)
Internal clock select and divide register26

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	cif_clk_out_sel CIF clock output selection 1'b0: select PLL divout 1'b1: select 24MHz
14	RO	0x0	reserved
13:9	RW	0x07	cif_clk_div_con cif clock divider frequency clk=clk_src/(div_con+1)
8	RW	0x0	cif_clk_pll_sel CIF clock pll source selection 1'b0: select codec PLL 1'b1: select general PLL
7:6	RW	0x3	crypto_div_con crypto clock divider frequency clk=clk_src/(div_con+1)
5:3	RO	0x0	reserved
2	RW	0x0	ddr_clk_pll_sel DDR clock pll source selection 1'b0: select DDR PLL 1'b1: select GENERAL PLL
1:0	RW	0x0	ddr_div_con Control DDR divider frequency 2'b00: clk_ddr_src:clk_ddrphy = 1:1 2'b01: clk_ddr_src:clk_ddrphy = 2:1 2'b11: clk_ddr_src:clk_ddrphy = 4:1

CRU_CLKSEL27_CON
Address: Operational Base + offset (0x00cc)
Internal clock select and divide register27

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x07	lcdc0_div_con Control LCDC0 clock divider frequency clk_lcdc0=lcdc0_clk_src/(lcdc0_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x0	lcdc0_pll_sel Control LCDC0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock

CRU_CLKSEL28_CON
Address: Operational Base + offset (0x00d0)
Internal clock select and divide register28

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	edp_24m_sel eDP 24M clock source selection 1'b00: select 27M clock 1'b01: select 24M clock
14:13	RO	0x0	reserved
12:8	RW	0x0f	hclk_vio_div_con VIO AHB clock divider frequency clk=clk_src/(div_con+1)
7:6	RW	0x0	edp_pll_sel eDP clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5:0	RW	0x03	edp_div_con eDP clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL29_CON
Address: Operational Base + offset (0x00d4)
Internal clock select and divide register29

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x07	lcdc1_div_con Control LCDC1 clock divider frequency clk_lcdc1=lcdc1_clk_src/(lcdc1_div_con+1)
7:6	RW	0x1	lcdc1_pll_sel Control LCDC1 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4	RW	0x0	cif_clkin_inv_sel CIF clkin invert selection 1'b0: normal 1'b1: invert
3	RW	0x0	isp_clkin_inv_sel ISP clkin invert selection 1'b0: normal 1'b1: invert
2	RW	0x0	hsicphy_12m_sel Control HSICPHY 12m clock selection 1'b0: select 12M from OSC 1'b1: select 12M from divout
1:0	RW	0x2	hsicphy_pll_sel Control HSICPHY clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy 480M clock

CRU_CLKSEL30_CON
Address: Operational Base + offset (0x00d8)
Internal clock select and divide register30

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	rga_core_clk_pll_sel rga func clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
13	RO	0x0	reserved
12:8	RW	0x00	rga_core_clk_div_con rga func clock divider frequency clk_rga_func = clk_rga_func_src/(rga_core_clk_div_con+1)
7:6	RW	0x0	rga_aclk_pll_sel Control rga AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved
4:0	RW	0x00	rga_aclk_div_con Control rga AXI clock divider frequency aclk_lcdc1=lcdc1_aclk_src/(rga_aclk_div_con+1)

CRU_CLKSEL31_CON

Address: Operational Base + offset (0x00dc)

Internal clock select and divide register31

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	vio1_aclk_pll_sel Control VIO1 AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x00	vio1_aclk_div_con Control VIO1 AXI clock divider frequency aclk_vio1=vio1_aclk_src/(vio1_aclk_div_con+1)
7:6	RW	0x0	vio0_aclk_pll_sel Control VIO0 AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved
4:0	RW	0x00	vio0_aclk_div_con Control VIO0 AXI clock divider frequency aclk_vio0=vio0_aclk_src/(vio0_aclk_div_con+1)

CRU_CLKSEL32_CON
Address: Operational Base + offset (0x00e0)
Internal clock select and divide register32

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	vdpu_aclk_pll_sel Control VDPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
13	RO	0x0	reserved
12:8	RW	0x01	vdpu_aclk_div_con Control VDPU AXI clock divider frequency aclk_vdpu=vdpu_aclk_src/(vdpu_aclk_div_con+1)
7:6	RW	0x0	vepu_aclk_pll_sel Control VEPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x01	vepu_aclk_div_con Control VEPU AXI clock divider frequency aclk_vepu=vepu_aclk_src/(vepu_aclk_div_con+1)

CRU_CLKSEL33_CON
Address: Operational Base + offset (0x00e4)
Internal clock select and divide register33

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask When HIGH, enable the writing corresponding bit When LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x03	alive_pclk_div_con alive apb clock divider frequency alive_pclk =alive_pclk_src/(alive_pclk_div_con+1)
7:5	RO	0x0	reserved
4:0	RW	0x03	pmu_pclk_div_con pmu apb clock divider frequency pmu_pclk =pmu_pclk_src/(pmu_pclk_div_con+1)

CRU_CLKSEL34_CON
Address: Operational Base + offset (0x00e8)
Internal clock select and divide register34

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x2	sdio1_pll_sel Control sdio1 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select 24MHz
13:8	RW	0x00	sdio1_div_con Control SDIO1 divider frequency clk_sdio=general_pll_clk/(sdio_div_con+1)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpu_aclk_pll_sel Control GPU AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select usbphy pll 480M clock 2'b11: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x00	gpu_aclk_div_con Control GPU AXI clock divider frequency aclk_gpu=gpu_aclk_src/(gpu_aclk_div_con+1)

CRU_CLKSEL35_CON

Address: Operational Base + offset (0x00ec)

Internal clock select and divide register35

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	tspout_clk_pll_sel Control tspout clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock 2'b11: select 27MHz IO input
13	RO	0x0	reserved
12:8	RW	0x03	tspout_clk_div_con Control tspout clock divider frequency clk=clk_src/(clk_div_con+1)
7:6	RW	0x0	tsp_clk_pll_sel Control tsp clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x03	tsp_clk_div_con Control tsp clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL36_CON

Address: Operational Base + offset (0x00f0)
Internal clock select and divide register36

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	clk_core3_div_con Control clk_core3 clock divider frequency clk=clk_src/(clk_div_con+1)
11	RO	0x0	reserved
10:8	RW	0x0	clk_core2_div_con Control clk_core2 clock divider frequency clk=clk_src/(clk_div_con+1)
7	RO	0x0	reserved
6:4	RW	0x0	clk_core1_div_con Control clk_core1 clock divider frequency clk=clk_src/(clk_div_con+1)
3	RO	0x0	reserved
2:0	RW	0x0	clk_core0_div_con Control clk_core0 clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL37_CON
Address: Operational Base + offset (0x00f4)
Internal clock select and divide register37

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:9	RW	0x0f	pclk_core_dbg_div_con Control core debg APB bus clock divider frequency clk=clk_src/(clk_div_con+1)
8:4	RW	0x0f	atclk_core_div_con Control core ATB BUS clock divider frequency clk=clk_src/(clk_div_con+1)
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x3	clk_l2ram_div_con Control clk_l2ram clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKSEL38_CON
Address: Operational Base + offset (0x00f8)
Internal clock select and divide register38

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	nandc1_clk_pll_sel Control nandc1 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
14:13	RO	0x0	reserved
12:8	RW	0x03	nandc1_clk_div_con Control nandc1 clock divider frequency clk_nandc=nandc_clk_src/(nandc_clk_div_con+1)
7	RW	0x0	nandc0_clk_pll_sel Control nandc0 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
6:5	RO	0x0	reserved
4:0	RW	0x03	nandc0_clk_div_con Control nandc0 clock divider frequency clk_nandc=nandc_clk_src/(nandc_clk_div_con+1)

CRU_CLKSEL39_CON
Address: Operational Base + offset (0x00fc)
Internal clock select and divide register39

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	aclk_hevc_pll_sel HEVC AXI clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13	RO	0x0	reserved
12:8	RW	0x00	aclk_hevc_div_con HEVC AXI clock divider frequency clk=clk_src/(clk_div_con+1)
7	RW	0x0	spi2_pll_sel Control spi2 clock PLL source selection 1'b0: select codec pll clock 1'b1: select general pll clock
6:0	RW	0x07	spi2_div_con Control SPI2 clock divider frequency clk=clk_src/(div_con+1)

CRU_CLKSEL40_CON
Address: Operational Base + offset (0x0100)
Internal clock select and divide register40

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:12	RW	0x0	hclk_hevc_div_con HEVC AHB clock divider frequency clk=clk_src/(clk_div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x2	spdif_8ch_clk_sel Control SPDIF 8ch clock work frequency selection 2'b00: select divider ouput from pll divider 2'b01: select divider ouput from fraction divider 2'b10: select 12MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x00	spdif_8ch_pll_div_con Control SPDIF 8ch PLL output divider freuency spdif_div_clk=spdif_div_src/(spdif_pll_div_con+1)

CRU_CLKSEL41_CON
Address: Operational Base + offset (0x0104)
Internal clock select and divide register41

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	spdif_8ch_frac_factor Control SPDIF 8ch fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL42_CON
Address: Operational Base + offset (0x0108)
Internal clock select and divide register42

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	clk_hevc_core_pll_sel HEVC CORE clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
13	RO	0x0	reserved
12:8	RW	0x00	clk_hevc_core_div_con HEVC CORE clock divider frequency clk=clk_src/(clk_div_con+1)
7:6	RW	0x0	clk_hevc_cabac_pll_sel HEVC CABAC clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select new pll clock
5	RO	0x0	reserved
4:0	RW	0x00	clk_hevc_cabac_div_con HEVC CABAC clock divider frequency clk=clk_src/(clk_div_con+1)

CRU_CLKGATE0_CON
Address: Operational Base + offset (0x0160)
Internal clock gating control register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	clk_acc_efuse_gate_en acc efuse clock disable. When HIGH, disable clock
11	RW	0x0	pd_bus_cpll_clk_gate_en pd_bus clock CPLL path clock disable. When HIGH, disable clock
10	RW	0x0	pd_bus_gpll_clk_gate_en pd_bus clock GPLL path clock disable. When HIGH, disable clock
9	RW	0x0	ddr_gpll_clk_gate_en DDR clock GPLL path clock disable. When HIGH, disable clock
8	RW	0x0	ddr_dpll_clk_gate_en DDR clock DPLL path clock disable. When HIGH, disable clock
7	RW	0x0	aclk_bus_2pmu_gate_en pd_bus AXI clock to pd_pmu clock disable. When HIGH, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_bus_gate_en pd_bus APB clock(pclk_cpu_pre) disable. When HIGH, disable clock
4	RW	0x0	hclk_bus_gate_en pd_bus AHB clock disable. When HIGH, disable clock
3	RW	0x0	aclk_bus_gate_en pd_bus AXI clock disable. When HIGH, disable clock
2	RW	0x0	core_gpll_clk_gate_en CORE clock GPLL path clock disable. When HIGH, disable clock
1	RW	0x0	core_apll_clk_gate_en CORE clock APLL path clock disable. When HIGH, disable clock
0	RO	0x0	reserved

CRU_CLKGATE1_CON

Address: Operational Base + offset (0x0164)

Internal clock gating control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_uart3_frac_src_gate_en UART3 fraction divider source clock disable. When HIGH, disable clock
14	RW	0x0	clk_uart3_src_gate_en UART3 source clock disable. When HIGH, disable clock
13	RW	0x0	clk_uart2_frac_src_gate_en UART2 fraction divider source clock disable. When HIGH, disable clock
12	RW	0x0	clk_uart2_src_gate_en UART2 source clock disable. When HIGH, disable clock
11	RW	0x0	clk_uart1_frac_src_gate_en UART1 fraction divider source clock disable. When HIGH, disable clock
10	RW	0x0	clk_uart1_src_gate_en UART1 source clock disable. When HIGH, disable clock
9	RW	0x0	clk_uart0_frac_src_gate_en UART0 fraction divider source clock disable. When HIGH, disable clock
8	RW	0x0	clk_uart0_src_gate_en UART0 source clock disable. When HIGH, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	clk_timer5_gate_en Timer5 clock(clk_timer5) disable. When HIGH, disable clock
4	RW	0x0	clk_timer4_gate_en Timer4 clock(clk_timer4) disable. When HIGH, disable clock
3	RW	0x0	clk_timer3_gate_en Timer3 clock(clk_timer3) disable. When HIGH, disable clock
2	RW	0x0	clk_timer2_gate_en Timer2 clock(clk_timer2) disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
1	RW	0x0	clk_timer1_gate_en Timer1 clock(clk_timer1) disable. When HIGH, disable clock
0	RW	0x0	clk_timer0_gate_en Timer0 clock(clk_timer0) disable. When HIGH, disable clock

CRU_CLKGATE2_CON

Address: Operational Base + offset (0x0168)

Internal clock gating control register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	clk_uart4_frac_src_gate_en UART4 fraction divider source clock disable. When HIGH, disable clock
12	RW	0x0	clk_uar4_src_gate_en UART4 source clock disable. When HIGH, disable clock
11	RW	0x0	clk_spi2_src_gate_en SPI2 source clock disable. When HIGH, disable clock
10	RW	0x0	clk_spi1_src_gate_en SPI1 source clock disable. When HIGH, disable clock
9	RW	0x0	clk_spi0_src_gate_en SPI0 source clock disable. When HIGH, disable clock
8	RW	0x0	clk_saradc_src_gate_en SARADC source clock disable. When HIGH, disable clock
7	RW	0x0	clk_tsadc_src_gate_en TSADC source clock disable. When HIGH, disable clock
6	RW	0x0	clk_hsadc_src_gate_en Field0000 Abstract When HIGH, disable clock
5	RW	0x0	clk_mac_src_gate_en MAC source clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
4	RO	0x0	reserved
3	RW	0x0	pclk_periph_gate_en PERIPH system APB clock(pclk_periph) disable. When HIGH, disable clock
2	RW	0x0	hclk_periph_gate_en PERIPH system AHB clock(hclk_periph) disable. When HIGH, disable clock
1	RW	0x0	aclk_periph_gate_en PERIPH system AXI clock(aclk_periph) disable. When HIGH, disable clock
0	RW	0x0	clk_periph_src_gate_en PERIPH system source clock disable. When HIGH, disable clock

CRU_CLKGATE3_CON
Address: Operational Base + offset (0x016c)
Internal clock gating control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_isp_jpeg_gate_en ISP jpeg source clock disable. When HIGH, disable clock
14	RW	0x0	clk_isp_gate_en ISP clock clock disable. When HIGH, disable clock
13	RW	0x0	clk_edp_gate_en eDP clock clock disable. When HIGH, disable clock
12	RW	0x0	clk_edp_24m_gate_en eDP 24M ref clock clock disable. When HIGH, disable clock
11	RW	0x0	aclk_vdpu_src_gate_en VDPU AXI source clock disable. When HIGH, disable clock
10	RW	0x0	hclk_vpu_gate_en VPU AHB source clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	aclk_vepu_src_gate_en VEPU AXI source clock disable. When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	clk_cif_out_gate_en CIF output clock disable. When HIGH, disable clock
6	RW	0x0	hsicphy_gate_en HSICPHY clock disable. When HIGH, disable clock
5	RW	0x0	aclk_rga_src_gate_en RGA AXI souce clock disable. When HIGH, disable clock
4	RW	0x0	clk_rga_core_src_gate_en RGA func souce clock disable. When HIGH, disable clock
3	RW	0x0	dclk_lcdc1_src_gate_en LCDC1 DCLK source clock disable. When HIGH, disable clock
2	RW	0x0	aclk_lcdc1_src_gate_en LCDC1 AXI source clock disable. When HIGH, disable clock
1	RW	0x0	dclk_lcdc0_src_gate_en LCDC0 DCLK source clock disable. When HIGH, disable clock
0	RW	0x0	aclk_lcdc0_src_gate_en LCDC0 AXI source clock disable. When HIGH, disable clock

CRU_CLKGATE4_CON
Address: Operational Base + offset (0x0170)
Internal clock gating control register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	testclk_gate_en Test output clock disable When HIGH, disable clock
14	RW	0x0	clk_jtag_gate_en JTAG clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
13	RW	0x0	clk_ddrphy1_gate_en DDRPHY1 clock disable. When HIGH, disable clock
12	RW	0x0	clk_ddrphy0_gate_en DDRPHY0 clock disable. When HIGH, disable clock
11	RW	0x0	clk_tspout_gate_en TSP output clock disable. When HIGH, disable clock
10	RW	0x0	clk_tsp_gate_en TSP clock disable. When HIGH, disable clock
9	RW	0x0	clk_spdif_8ch_gate_en SPDIF 8ch clock disable. When HIGH, disable clock
8	RW	0x0	clk_spdif_8ch_frac_src_gate_en SPDIF 8ch fraction divider source clock disable. When HIGH, disable clock
7	RW	0x0	clk_spdif_8ch_src_gate_en SPDIF 8ch source clock disable. When HIGH, disable clock
6	RW	0x0	clk_spdif_gate_en SPDIF clock disable. When HIGH, disable clock
5	RW	0x0	clk_spdif_frac_src_gate_en SPDIF fraction divider source clock disable. When HIGH, disable clock
4	RW	0x0	clk_spdif_src_gate_en SPDIF source clock disable. When HIGH, disable clock
3	RW	0x0	clk_i2s0_gate_en I2S clock disable. When HIGH, disable clock
2	RW	0x0	clk_i2s0_frac_src_gate_en I2S fraction divider source clock disable. When HIGH, disable clock
1	RW	0x0	clk_i2s0_src_gate_en I2S source clock disable. When HIGH, disable clock
0	RW	0x0	clk_i2s0_out_gate_en I2S output clock disable. When HIGH, disable clock

CRU_CLKGATE5_CON

Address: Operational Base + offset (0x0174)
Internal clock gating control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_mipidsi_24m_gate_en mipi dsi 24M clock disable. When HIGH, disable clock
14	RW	0x0	clk_usbphy480m_gate_en usbphy480M clock disable. When HIGH, disable clock
13	RW	0x0	ps2c_clk_gate_en PS2 controlor clock disable. When HIGH, disable clock
12	RW	0x0	hdmi_hdcp_clk_gate_en HDMI HDCP clock disable. When HIGH, disable clock
11	RW	0x0	hdmi_cec_clk_gate_en HDMI CEC clock disable. When HIGH, disable clock
10	RW	0x0	clk_pvtm_gpu_gate_en pd_gpu PVTM clock disable. When HIGH, disable clock
9	RW	0x0	clk_pvtm_core_gate_en pd_core PVTM clock disable. When HIGH, disable clock
8	RW	0x0	pclk_pmu_gate_en pd_pmu APB bus clock disable. When HIGH, disable clock
7	RW	0x0	clk_gpu_gate_en gpu clock disable. When HIGH, disable clock
6	RW	0x0	clk_nandc1_gate_en nandc1 clock disable. When HIGH, disable clock
5	RW	0x0	clk_nandc0_gate_en nandc0 clock disable. When HIGH, disable clock
4	RW	0x0	clk_crypto_gate_en crypto clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	clk_mac_refout_gate_en MAC ref output clock clock disable. When HIGH, disable clock
2	RW	0x0	clk_mac_ref_gate_en MAC ref clock clock disable. When HIGH, disable clock
1	RW	0x0	clk_mac_tx_gate_en MAC tx clock clock disable. When HIGH, disable clock
0	RW	0x0	clk_mac_rx_gate_en MAC rx clock clock disable. When HIGH, disable clock

CRU_CLKGATE6_CON
Address: Operational Base + offset (0x0178)
Internal clock gating control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_i2c4_gate_en I2C4 APB clock disable. When HIGH, disable clock
14	RW	0x0	pclk_i2c3_gate_en I2C3 APB clock disable. When HIGH, disable clock
13	RW	0x0	pclk_i2c2_gate_en I2C2 APB clock disable. When HIGH, disable clock
12	RW	0x0	pclk_uart_exp_gate_en UART_exp APB clock disable. When HIGH, disable clock
11	RW	0x0	pclk_uart_gps_gate_en UART_gps APB clock disable. When HIGH, disable clock
10	RO	0x0	reserved
9	RW	0x0	pclk_uart_bb_gate_en UART_bb APB clock disable. When HIGH, disable clock
8	RW	0x0	pclk_uart_bt_gate_en UART_bt APB clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	pclk_ps2c0_gate_en PS2C0 APB clock disable. When HIGH, disable clock
6	RW	0x0	pclk_spi2_gate_en SPI2 APB clock disable. When HIGH, disable clock
5	RW	0x0	pclk_spi1_gate_en SPI1 APB clock disable. When HIGH, disable clock
4	RW	0x0	pclk_spi0_gate_en SPI0 APB clock disable. When HIGH, disable clock
3	RW	0x0	aclk_dmac_peri_gate_en DMAC peri AXI clock disable. When HIGH, disable clock
2	RW	0x0	aclk_peri_axi_matrix_gate_en Peripheral matrix axi clock disable. When HIGH, disable clock
1	RW	0x0	pclk_peri_axi_matrix_gate_en Peripheral matrix apb clock disable. When HIGH, disable clock
0	RW	0x0	hclk_peri_matrix_gate_en Peripheral matrix ahb clock disable. When HIGH, disable clock

CRU_CLKGATE7_CON
Address: Operational Base + offset (0x017c)
Internal clock gating control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_nand1_gate_en NAND1 AHB clock disable. When HIGH, disable clock
14	RW	0x0	hclk_nand0_gate_en NAND0 AHB clock disable. When HIGH, disable clock
13	RW	0x0	hclk_mmc_peri_gate_en arbiter in peri_ahb_mmc module AHB clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
12	RW	0x0	hclk_emem_peri_gate_en arbiter in peri_ahb_emem module AHB clock disable. When HIGH, disable clock
11	RW	0x0	aclk_peri_niu_gate_en NIU in peripheral power domain AXI clock disable. When HIGH, disable clock
10	RW	0x0	hclk_peri_ahb_arbi_gate_en AHB arbiter in peripheral power domain AHB clock disable. When HIGH, disable clock
9	RW	0x0	hclk_usb_peri_gate_en USB arbiter AHB clock disable. When HIGH, disable clock
8	RW	0x0	hclk_hsic_gate_en HSIC AHB clock disable. When HIGH, disable clock
7	RW	0x0	hclk_host1_gate_en HOST1 AHB clock disable. Field0000 Description
6	RW	0x0	hclk_host0_gate_en HOST0 AHB clock disable. Field0000 Description
5	RW	0x0	pmu_hclk_otg0_gate_en USB OTG PMU AHB clock disable. When HIGH, disable clock
4	RW	0x0	hclk_otg0_gate_en USB OTG AHB clock disable. When HIGH, disable clock
3	RW	0x0	pclk_sim_gate_en SIM APB clock disable. When HIGH, disable clock
2	RW	0x0	pclk_tsadc_gate_en TSADC APB clock disable. When HIGH, disable clock
1	RW	0x0	pclk_saradc_gate_en SARADC APB clock disable. When HIGH, disable clock
0	RW	0x0	pclk_i2c5_gate_en I2C5 APB clock disable. When HIGH, disable clock

CRU_CLKGATE8_CON
Address: Operational Base + offset (0x0180)

Internal clock gating control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	aclk_peri_mmu_gate_en PERI_MMU aclk clock disable. When HIGH, disable clock
11	RW	0x0	clk_27m_tsp_gate_en 27M_TSP clock disable. When HIGH, disable clock
10	RW	0x0	clk_hsadc_1_tsp_gate_en HSADC_1_TSP clock disable. When HIGH, disable clock
9	RW	0x0	clk_hsadc_0_tsp_gate_en HSADC_0_TSP clock disable. When HIGH, disable clock
8	RW	0x0	hclk_tsp_gate_en TSP AHB clock disable. When HIGH, disable clock
7	RW	0x0	hclk_hsadc_gate_en HSADC AHB clock disable. When HIGH, disable clock
6	RW	0x0	hclk_emmc_gate_en EMMC AHB clock disable. When HIGH, disable clock
5	RW	0x0	hclk_sdio1_gate_en SDIO1 AHB clock disable. When HIGH, disable clock
4	RW	0x0	hclk_sdio0_gate_en SDIO0 AHB clock disable. When HIGH, disable clock
3	RW	0x0	hclk_sdmmc_gate_en SDMMC AHB clock disable. When HIGH, disable clock
2	RW	0x0	hclk_gps_gate_en GPS hclk clock disable. When HIGH, disable clock
1	RW	0x0	pclk_gmac_gate_en GMAC pclk clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
0	RW	0x0	aclk_gmac_gate_en GMAC aclk clock disable. When HIGH, disable clock

CRU_CLKGATE9_CON
Address: Operational Base + offset (0x0184)
Internal clock gating control register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:2	RO	0x0	reserved
1	RW	0x0	hclk_video_clock_en VIDEO AHB clock disable. When HIGH, disable clock
0	RW	0x0	aclk_video_gate_en VIDEO AXI clock disable. When HIGH, disable clock

CRU_CLKGATE10_CON
Address: Operational Base + offset (0x0188)
Internal clock gating control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_publ0_gate_en DDR0 PUBL apb clock disable When HIGH, disable clock
14	RW	0x0	pclk_ddrupctl0_gate_en DDRUPCTL0 apb clock disable When HIGH, disable clock
13	RW	0x0	aclk_strc_sys_gate_en aclk_strc_sys (CPU Structure system) clock disable. When HIGH, disable clock
12	RW	0x0	aclk_dmac_bus_gate_en DMAC_BUS aclk clock disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
11	RW	0x0	hclk_spdif_8ch_gate_en hclk_spdif_8ch clock disable. When HIGH, disable clock
10	RW	0x0	hclk_spdif_gate_en hclk_spdif clock disable. When HIGH, disable clock
9	RW	0x0	hclk_rom_gate_en hclk_rom clock disable. When HIGH, disable clock
8	RW	0x0	hclk_i2s_8ch_gate_en hclk_i2s_8ch AHB clock disable. When HIGH, disable clock
7	RW	0x0	clk_intmem2_gate_en intmem2 clock disable. When HIGH, disable clock
6	RW	0x0	clk_intmem1_gate_en intmem1 clock disable. When HIGH, disable clock
5	RW	0x0	clk_intmem0_gate_en intmem0 clock disable. When HIGH, disable clock
4	RW	0x0	aclk_intmem_gate_en intmem axi clock disable. When HIGH, disable clock
3	RW	0x0	pclk_i2c1_gate_en pclk_i2c1 disable. When HIGH, disable clock
2	RW	0x0	pclk_i2c0_gate_en pclk_i2c0 disable. When HIGH, disable clock
1	RW	0x0	pclk_timer_gate_en pclk_timer disable. When HIGH, disable clock
0	RW	0x0	pclk_pwm_gate_en pclk_pwm disable. When HIGH, disable clock

CRU_CLKGATE11_CON

Address: Operational Base + offset (0x018c)

Internal clock gating control register11

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	pclk_rkpwm_gate_en pclk_rkpwm disable. When HIGH, disable clock
10	RW	0x0	pclk_efuse_256_gate_en EFUSE256 APB clock disable. When HIGH, disable clock
9	RW	0x0	pclk_uart_dbg_gate_en UART_DBG APB clock disable. When HIGH, disable clock
8	RW	0x0	aclk_ccp_gate_en CCP aclk clock disable. When HIGH, disable clock
7	RW	0x0	hclk_crypto_gate_en CRYPTO sclk clock disable. When HIGH, disable clock
6	RW	0x0	aclk_crypto_gate_en CRYPTO mclk clock disable. When HIGH, disable clock
5	RW	0x0	nclk_ddrupctl1_gate_en DDR Controller PHY clock disable. When HIGH, disable clock
4	RW	0x0	nclk_ddrupctl0_gate_en DDR Controller PHY clock disable. When HIGH, disable clock
3	RW	0x0	pclk_tzpc_gate_en TZPC APB clock disable. When HIGH, disable clock
2	RW	0x0	pclk_efuse_1024_gate_en EFUSE1024 APB clock disable. When HIGH, disable clock
1	RW	0x0	pclk_publ1_gate_en DDR1 PUBL apb clock disable When HIGH, disable clock
0	RW	0x0	pclk_ddrupctl1_gate_en DDRUPCTL1 apb clock disable When HIGH, disable clock

CRU_CLKGATE12_CON

Address: Operational Base + offset (0x0190)
Internal clock gating control register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	pclk_core_niu_gate_en core NIU APB bus clock disable. When HIGH, disable clock
10	RW	0x0	cs_dbg_clk_gate_en coresight debug clock disable. When HIGH, disable clock
9	RW	0x0	dbg_core_clk_gate_en core debug clock disable. When HIGH, disable clock
8	RW	0x0	dbg_src_clk_gate_en Debug source clock disable. When HIGH, disable clock
7	RW	0x0	atclk_core_gate_en core ATB bus clock disable. When HIGH, disable clock
6	RW	0x0	aclk_mp_gate_en core MP AXI bus clock disable. When HIGH, disable clock
5	RW	0x0	aclk_core_m0_gate_en CORE m0 AXI bus clock disable. When HIGH, disable clock
4	RW	0x0	l2_ram_clk_gate_en L2 RAM clock disable. When HIGH, disable clock
3	RW	0x0	core3_clk_gate_en core3 clock disable. When HIGH, disable clock
2	RW	0x0	core2_clk_gate_en core2 clock disable. When HIGH, disable clock
1	RW	0x0	coer1_clk_gate_en core1 clock disable. When HIGH, disable clock
0	RW	0x0	core0_clk_gate_en core0 clock disable. When HIGH, disable clock

CRU_CLKGATE13_CON
Address: Operational Base + offset (0x0194)
Internal clock gating control register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_hevc_core_gate_en HEVC CORE clock disable. When HIGH, disable clock
14	RW	0x0	clk_hevc_cabac_gate_en HEVC cabac clock disable. When HIGH, disable clock
13	RW	0x0	aclk_hevc_gate_en HEVC AXI clock disable. When HIGH, disable clock
12	RW	0x0	clk_wifi_gate_en wifi/gps/bt 3in1 16.384M clock disable. When HIGH, disable clock
11	RW	0x0	clk_lcdc_pwm1_gate_en lcdc_pwm1 clock disable. When HIGH, disable clock
10	RW	0x0	clk_lcdc_pwm0_gate_en lcdc_pwm0 clock disable. When HIGH, disable clock
9	RW	0x0	clk_hsic_12m_gate_en HSIC 12MHz clock disable. When HIGH, disable clock
8	RW	0x0	clk_c2c_host_gate_en C2C HOST clock disable. When HIGH, disable clock
7	RW	0x0	clk_otg_adp_gate_en OTG adp clock disable. When HIGH, disable clock
6	RW	0x0	clk_otgphy2_gate_en OTGPHY2 clock(clk_otgphy2) disable. When HIGH, disable clock

Bit	Attr	Reset Value	Description
5	RW	0x0	clk_otgphy1_gate_en OTGPHY1 clock(clk_otgphy1) disable. When HIGH, disable clock
4	RW	0x0	clk_otgphy0_gate_en OTGPHY0 clock(clk_otgphy0) disable. When HIGH, disable clock
3	RW	0x0	clk_emmc_src_gate_en EMMC source clock disable. When HIGH, disable clock
2	RW	0x0	clk_sdio1_src_gate_en SDIO1 source clock disable. When HIGH, disable clock
1	RW	0x0	clk_sdio0_src_gate_en SDIO0 source clock disable. When HIGH, disable clock
0	RW	0x0	clk_mmc0_src_gate_en SDMMC0 source clock disable. When HIGH, disable clock

CRU_CLKGATE14_CON
Address: Operational Base + offset (0x0198)
Internal clock gating control register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	pclk_alive_niu_gate_en ALIVE_NIU pclk disable When HIGH, disable clock
11	RW	0x0	pclk_grf_gate_en GRF pclk disable When HIGH, disable clock
10:9	RO	0x0	reserved
8	RW	0x0	pclk_gpio8_gate_en GPIO8 pclk disable When HIGH, disable clock
7	RW	0x0	pclk_gpio7_gate_en GPIO7 pclk disable When HIGH, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_gpio6_gate_en GPIO6 pclk disable When HIGH, disable clock
5	RW	0x0	pclk_gpio5_gate_en GPIO5 pclk disable When HIGH, disable clock
4	RW	0x0	pclk_gpio4_gate_en GPIO4 pclk disable When HIGH, disable clock
3	RW	0x0	pclk_gpio3_gate_en GPIO3 pclk disable When HIGH, disable clock
2	RW	0x0	pclk_gpio2_gate_en GPIO2 pclk disable When HIGH, disable clock
1	RW	0x0	pclk_gpio1_gate_en GPIO1 pclk disable When HIGH, disable clock
0	RO	0x0	reserved

CRU_CLKGATE15_CON
Address: Operational Base + offset (0x019c)
Internal clock gating control register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_vip_gate_en VIP hclk disable When HIGH, disable clock
14	RW	0x0	aclk_vip_gate_en VIP aclk disable When HIGH, disable clock
13	RW	0x0	aclk_vio2_noc_gate_en VIO2_NOC aclk disable When HIGH, disable clock
12	RW	0x0	aclk_vio1_noc_gate_en VIO1_NOC aclk disable When HIGH, disable clock
11	RW	0x0	aclk_vio0_noc_gate_en VIO0_NOC aclk disable When HIGH, disable clock

Bit	Attr	Reset Value	Description
10	RW	0x0	hclk_vio_noc_gate_en VIO_NOC hclk disable When HIGH, disable clock
9	RW	0x0	hclk_vio_ahb_arbi_gate_en VIO_AHB_ARBI hclk disable When HIGH, disable clock
8	RW	0x0	hclk_lcdc1_gate_en LCDC1 hclk disable When HIGH, disable clock
7	RW	0x0	aclk_lcdc1_gate_en LCDC1 aclk disable When HIGH, disable clock
6	RW	0x0	hclk_lcdc0_gate_en LCDC0 hclk disable When HIGH, disable clock
5	RW	0x0	aclk_lcdc0_gate_en LCDC0 aclk disable When HIGH, disable clock
4	RW	0x0	aclk_lcdc_iep_gate_en LCDC_IEP aclk disable When HIGH, disable clock
3	RW	0x0	hclk_iep_gate_en IEP hclk disable When HIGH, disable clock
2	RW	0x0	aclk_iep_gate_en IEP aclk disable When HIGH, disable clock
1	RW	0x0	hclk_rga_gate_en RGA hclk disable When HIGH, disable clock
0	RW	0x0	aclk_rga_gate_en RGA aclk disable When HIGH, disable clock

CRU_CLKGATE16_CON

Address: Operational Base + offset (0x01a0)

Internal clock gating control register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	pclk_vio2_h2p_gate_en VIO2_H2P pclk disable When HIGH, disable clock
10	RW	0x0	hclk_vio2_h2p_gate_en VIO2_H2P hclk disable When HIGH, disable clock
9	RW	0x0	pclk_hdmi_ctrl_gate_en HDMI_CTRL pclk disable When HIGH, disable clock
8	RW	0x0	pclk_edp_ctrl_gate_en EDP_CTRL pclk disable When HIGH, disable clock
7	RW	0x0	pclk_lvds_phy_gate_en LVDS_PHY pclk disable When HIGH, disable clock
6	RW	0x0	pclk_mipi_csi_gate_en MIPI_CSI pclk disable When HIGH, disable clock
5	RW	0x0	pclk_mipi_dsi1_gate_en MIPI_DSI1 pclk disable When HIGH, disable clock
4	RW	0x0	pclk_mipi_dsi0_gate_en MIPI_DSI0 pclk disable When HIGH, disable clock
3	RW	0x0	pclkin_isp_gate_en ISP pclkin disable When HIGH, disable clock
2	RW	0x0	aclk_isp_gate_en ISP aclk disable When HIGH, disable clock
1	RW	0x0	hclk_isp_gate_en ISP hclk disable When HIGH, disable clock
0	RW	0x0	pclkin_vip_gate_en VIP pclkin disable When HIGH, disable clock

CRU_CLKGATE17_CON

Address: Operational Base + offset (0x01a4)

Internal clock gating control register17

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:5	RO	0x0	reserved
4	RW	0x0	pclk_gpio0_gate_en GPIO0 pclk disable When HIGH, disable clock
3	RW	0x0	pclk_sgrf_gate_en SGRF pclk disable When HIGH, disable clock
2	RW	0x0	pclk_pmu_noc_gate_en PMU_NOC pclk disable When HIGH, disable clock
1	RW	0x0	pclk_intmem1_gate_en INTMEM1 pclk disable When HIGH, disable clock
0	RW	0x0	pclk_pmu_gate_en PMU pclk disable When HIGH, disable clock

CRU_CLKGATE18_CON
Address: Operational Base + offset (0x01a8)
Internal clock gating control register18

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:1	RO	0x0	reserved
0	RW	0x0	aclk_gpu_gate_en GPU aclk disable When HIGH, disable clock

CRU_GLB_SRST_FST_VALUE
Address: Operational Base + offset (0x01b0)
The first global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	glb_srst_fst_value The first global software reset config value If config 0xfdb9, it will generate first global software reset.

CRU_GLB_SRST_SND_VALUE
Address: Operational Base + offset (0x01b4)
The second global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_snd_value The second global software reset config value If config 0xeca8, it will generate second global software reset.

CRU_SOFTRST0_CON
Address: Operational Base + offset (0x01b8)
Internal software reset control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	core3_dbg_srstn_req Core3 CPU debug software reset request. When HIGH, reset relative logic
14	RW	0x0	core2_dbg_srstn_req Core2 CPU debug software reset request. When HIGH, reset relative logic
13	RW	0x0	core1_dbg_srstn_req Core1 CPU debug software reset request. When HIGH, reset relative logic
12	RW	0x0	core0_dbg_srstn_req Core0 CPU debug software reset request. When HIGH, reset relative logic
11	RW	0x0	topdbg_srstn_req CPU top debug software reset request. When HIGH, reset relative logic
10	RW	0x0	l2c_srstn_req L2 controller software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
9	RW	0x0	pd_bus_str_sys_asrstn_req PD BUS NOC AXI software reset request. When HIGH, reset relative logic
8	RW	0x0	pd_core_str_sys_asrstn_req PD CORE NOC AXI software reset request. When HIGH, reset relative logic
7	RW	0x0	core3_po_srstn_req Core3 CPU PO software reset request. When HIGH, reset relative logic
6	RW	0x0	core2_po_srstn_req Core2 CPU PO software reset request. When HIGH, reset relative logic
5	RW	0x0	core1_po_srstn_req Core1 CPU PO software reset request. When HIGH, reset relative logic
4	R/WSC	0x0	core0_po_srstn_req Core0 CPU PO software reset request. When HIGH, reset relative logic
3	RW	0x0	core3_srstn_req Core3 CPU software reset request. When HIGH, reset relative logic
2	RW	0x0	core2_srstn_req Core2 CPU software reset request. When HIGH, reset relative logic
1	RW	0x0	core1_srstn_req Core1 CPU software reset request. When HIGH, reset relative logic
0	R/WSC	0x0	core0_srstn_req Core0 CPU software reset request. When HIGH, reset relative logic

CRU_SOFTRST1_CON
Address: Operational Base + offset (0x01bc)
Internal software reset control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	efuse_psrstn_req EFUSE APB software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
14	RW	0x0	timer5_srstn_req Timer5 software reset request. When HIGH, reset relative logic
13	RW	0x0	timer4_srstn_req Timer4 software reset request. When HIGH, reset relative logic
12	RW	0x0	timer3_srstn_req Timer3 software reset request. When HIGH, reset relative logic
11	RW	0x0	timer2_srstn_req Timer2 software reset request. When HIGH, reset relative logic
10	RW	0x0	timer1_srstn_req Timer1 software reset request. When HIGH, reset relative logic
9	RW	0x0	timer0_srstn_req Timer0 software reset request. When HIGH, reset relative logic
8	RW	0x0	spdif_srstn_req SPDIF software reset request. When HIGH, reset relative logic
7	RW	0x0	i2s_srstn_req I2S software reset request. When HIGH, reset relative logic
6	RW	0x0	timer_psrstn_req Timer APB software reset request. When HIGH, reset relative logic
5	RW	0x0	spdif_8ch_srstn_req SPDIF 8ch software reset request. When HIGH, reset relative logic
4	RW	0x0	rom_srstn_req ROM software reset request. When HIGH, reset relative logic
3	RW	0x0	intmem_srstn_req Internal memory software reset request. When HIGH, reset relative logic
2	RW	0x0	dma1_srstn_req DMA1 software reset request. When HIGH, reset relative logic
1	RW	0x0	efuse_256bit_psrstn_req 256bit EFUSE APB software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
0	RW	0x0	pd_bus_ahb_arbitor_srstn_req pd_bus ahb arbitor software reset request. pd_cpu AHB arbitor reset control When HIGH, reset relative logic

CRU_SOFTRST2_CON

Address: Operational Base + offset (0x01c0)

Internal software reset control register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	i2c5_srstn_req I2C5 software reset request. When HIGH, reset relative logic
14	RW	0x0	i2c4_srstn_req I2C4 software reset request. When HIGH, reset relative logic
13	RW	0x0	i2c3_srstn_req I2C3 software reset request. When HIGH, reset relative logic
12	RW	0x0	i2c2_srstn_req I2C2 software reset request. When HIGH, reset relative logic
11	RW	0x0	i2c1_srstn_req I2C1 software reset request. When HIGH, reset relative logic
10	RW	0x0	i2c0_srstn_req I2C0 software reset request. When HIGH, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	gpio8_srstn_req GPIO8 software reset request. When HIGH, reset relative logic
7	RW	0x0	gpio7_srstn_req GPIO7 software reset request. When HIGH, reset relative logic
6	RW	0x0	gpio6_srstn_req GPIO6 software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio5_srstn_req GPIO5 software reset request. When HIGH, reset relative logic
4	RW	0x0	gpio4_srstn_req GPIO4 software reset request. When HIGH, reset relative logic
3	RW	0x0	gpio3_srstn_req GPIO3 software reset request. When HIGH, reset relative logic
2	RW	0x0	gpio2_srstn_req GPIO2 software reset request. When HIGH, reset relative logic
1	RW	0x0	gpio1_srstn_req GPIO1 software reset request. When HIGH, reset relative logic
0	RW	0x0	gpio0_srstn_req GPIO0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST3_CON
Address: Operational Base + offset (0x01c4)
Internal software reset control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	usb_peri_srstn_req USB PERIPH software reset request. When HIGH, reset relative logic
14	RW	0x0	emem_peri_srstn_req EMEM ahb bus software reset request. When HIGH, reset relative logic
13	RW	0x0	pd_peri_ahb_arbitor_srstn_req pd_peri ahb arbitor software reset request. cypro, nandc, hsic, otg, uhost AHB arbitor reset control When HIGH, reset relative logic
12	RW	0x0	periph_niu_srstn_req PERIPH NIU software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
11	RW	0x0	periphsys_psrstn_req PERIPH APB software reset request. pd_peri bus matrix apb softreset When HIGH, reset relative logic
10	RW	0x0	periphsys_hsrstn_req PERIPH AHB software reset request. pd_peri bus matrix ahb softreset When HIGH, reset relative logic
9	RW	0x0	periphsys_asrstn_req PERIPH AXI software reset request. pd_peri bus matrix axi softreset When HIGH, reset relative logic
8	RW	0x0	pmu_srstn_req PMU software reset request. When HIGH, reset relative logic
7	RW	0x0	grf_srstn_req GRF software reset request. When HIGH, reset relative logic
6	RW	0x0	pmu_psrstn_req PMU APB bus software reset request. When HIGH, reset relative logic
5	RW	0x0	tpiu_atsrstn_req TPIU ATB software reset request. When HIGH, reset relative logic
4	RW	0x0	dap_sys_srstn_req DAP system software reset request. When HIGH, reset relative logic
3	RW	0x0	dap_srstn_req DAP software reset request. When HIGH, reset relative logic
2	RW	0x0	periph_mmu_srstn_req PERIPH MMU software reset request. When HIGH, reset relative logic
1	RW	0x0	mmc_peri_srstn_req pd_peri mmc AHB bus software reset request. emmc, sdio, sdmmc AHB arbitor reset control When HIGH, reset relative logic
0	RW	0x0	dw_pwm_srstn_req DW_PWM software reset request. When HIGH, reset relative logic

CRU_SOFTRST4_CON

Address: Operational Base + offset (0x01c8)

Internal software reset control register4

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	nandc1_srstn_req NANDC1 software reset request. When HIGH, reset relative logic
13	RW	0x0	nandc0_srstn_req NANDC0 software reset request. When HIGH, reset relative logic
12	RW	0x0	hsadc_srstn_req HSADC software reset request. When HIGH, reset relative logic
11	RW	0x0	hsicphy_srstn_req HSICPHY software reset request. When HIGH, reset relative logic
10	RW	0x0	hsic_aux_srstn_req HSIC AUX AHB software reset request. When HIGH, reset relative logic
9	RW	0x0	hsic_srstn_req HSIC AHB software reset request. When HIGH, reset relative logic
8	RW	0x0	usb_host0_srstn_req USB HOST0 AHB software reset request. When HIGH, reset relative logic
7	RW	0x0	ccp_srstn_req CCP software reset request. When HIGH, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	rk_pwm_srstn_req RK_PWM software reset request. When HIGH, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	gps_srstn_req GPS software reset request. When HIGH, reset relative logic
2	RW	0x0	mac_srstn_req MAC software reset request. When HIGH, reset relative logic
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	dma2_srstn_req DMA2 software reset request. When HIGH, reset relative logic

CRU_SOFTRST5_CON
Address: Operational Base + offset (0x01cc)
Internal software reset control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	security_grf_psrstn_req security GRF APB software reset request. When HIGH, reset relative logic
10	RW	0x0	pd_pmu_niu_psrstn_req pd_pmu niu APB software reset request. When HIGH, reset relative logic
9	RW	0x0	pd_pmu_intmem_psrstn_req pd_pmu internal memory apb software reset request. When HIGH, reset relative logic
8	RW	0x0	pd_alive_niu_psrstn_req pd_alive niu APB software reset request. When HIGH, reset relative logic
7	RW	0x0	saradc_srstn_req SARADC software reset request. When HIGH, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	spi2_srstn_req SPI2 software reset request. When HIGH, reset relative logic
4	RW	0x0	spi1_srstn_req SPI1 software reset request. When HIGH, reset relative logic
3	RW	0x0	spi0_srstn_req SPI0 software reset request. When HIGH, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	tzpc_srstn_req TZPC software reset request. When HIGH, reset relative logic

CRU_SOFTRST6_CON
Address: Operational Base + offset (0x01d0)
Internal software reset control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	edp_srstn_req eDP software reset request. When HIGH, reset relative logic
14	RW	0x0	isp_srstn_req ISP software reset request. When HIGH, reset relative logic
13	RW	0x0	rga_hsrstn_req RGA AHB software reset request. When HIGH, reset relative logic
12	RW	0x0	rga_asrstn_req RGA AXI software reset request. When HIGH, reset relative logic
11	RW	0x0	iep_hsrstn_req IEP AHB software reset request. When HIGH, reset relative logic
10	RW	0x0	iep_asrstn_req IEP AXI software reset request. When HIGH, reset relative logic
9	RW	0x0	rga_core_srstn_req RGA func software reset request. When HIGH, reset relative logic
8	RW	0x0	vip_srstn_req VIP software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
7	RW	0x0	vio1_niu_asrstn_req VIO1 NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
6	RW	0x0	lcdc0_dsrstn_req LCDC0 DCLK software reset request. When HIGH, reset relative logic
5	RW	0x0	lcdc0_hsrstn_req LCDC0 AHB software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
4	RW	0x0	lcdc0_asrstn_req LCDC0 AXI software reset request. When HIGH, reset relative logic
3	RW	0x0	vio_niu_hsrstn_req VIO NIU AHB software reset request. When HIGH, reset relative logic
2	RW	0x0	vio0_niu_asrstn_req VIO0 NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
1	RW	0x0	rga_niu_asrstn_req RGA NIU AXI software reset request. IEP ISP VOP's NIU software reset. When HIGH, reset relative logic
0	RW	0x0	vio_arbi_hsrstn_req VIO arbitor AHB software reset request. When HIGH, reset relative logic

CRU_SOFTRST7_CON

Address: Operational Base + offset (0x01d4)

Internal software reset control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	gpu_pvtm_srstn_req gpu pvtm software reset request. When HIGH, reset relative logic
12	RW	0x0	core_pvtm_srstn_req core pvtm software reset request. When HIGH, reset relative logic
11:10	RO	0x0	reserved
9	RW	0x0	hdmi_srstn_req HDMI software reset request. When HIGH, reset relative logic
8	RW	0x0	gpu_srstn_req GPU core software reset request. When HIGH, reset relative logic
7	RW	0x0	lvds_con_srstn_req LVDS controller software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
6	RW	0x0	lvds_phy_psrstn_req LVDS PHY APB software reset request. When HIGH, reset relative logic
5	RW	0x0	mipicsi_psrstn_req MIPi CSI APB software reset request. When HIGH, reset relative logic
4	RW	0x0	mipidsi1_psrstn_req MIPi DSI1 APB software reset request. When HIGH, reset relative logic
3	RW	0x0	mipidsi0_psrstn_req MIPi DSI0 APB software reset request. When HIGH, reset relative logic
2	RW	0x0	vio_h2p_hsrstn_req VIO ahb to apb bridge AHB software reset request. When HIGH, reset relative logic
1	RW	0x0	vcodec_hsrstn_req VCODEC AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	vcodec_asrstn_req VCODEC AXI software reset request. When HIGH, reset relative logic

CRU_SOFTRST8_CON
Address: Operational Base + offset (0x01d8)
Internal software reset control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	acc_efuse_srstn_req acc efuse software reset request. When HIGH, reset relative logic
13	RW	0x0	usb_adp_srstn_req OTG adp clock software reset request. When HIGH, reset relative logic
12	RW	0x0	usbhost1c_srstn_req USBHOST1 controller software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
11	RW	0x0	usbhost1phy_srstn_req USBHOST1 PHY software reset request. When HIGH, reset relative logic
10	RW	0x0	usbhost1_hsrstn_req USBHOST1 AHB BUS software reset request. When HIGH, reset relative logic
9	RW	0x0	usbhost0c_srstn_req USBHOST0 controller software reset request. When HIGH, reset relative logic
8	RW	0x0	usbhost0phy_srstn_req USBHOST0 PHY software reset request. When HIGH, reset relative logic
7	RW	0x0	usbhost0_hsrstn_req USBHOST0 AHB BUS software reset request. When HIGH, reset relative logic
6	RW	0x0	usbotgc_srstn_req USBOTG controller software reset request. When HIGH, reset relative logic
5	RW	0x0	usbotgphy_srstn_req USBOTG PHY software reset request. When HIGH, reset relative logic
4	RW	0x0	usbotg_hsrstn_req USBOTG AHB BUS software reset request. When HIGH, reset relative logic
3	RW	0x0	emmc_srstn_req EMMC software reset request. When HIGH, reset relative logic
2	RW	0x0	sdio1_srstn_req SDIO1 software reset request. When HIGH, reset relative logic
1	RW	0x0	sdio0_srstn_req SDIO0 software reset request. When HIGH, reset relative logic
0	RW	0x0	mmc0_srstn_req SDMMC0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST9_CON

Address: Operational Base + offset (0x01dc)

Internal software reset control register9

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	tsadc_psrstn_req TSADC APB software reset request. When HIGH, reset relative logic
14:11	RO	0x0	reserved
10	RW	0x0	hevc_srstn_req HEVC software reset request. When HIGH, reset relative logic
9	RW	0x0	rga_h2p_brg_srstn_req RGA AHB to APB bridge software reset request. When HIGH, reset relative logic
8	RW	0x0	vio1_h2p_brg_srstn_req VIO1 AHB to APB bridge software reset request. When HIGH, reset relative logic
7	RW	0x0	vio0_h2p_brg_srstn_req VIO0 AHB to APB bridge software reset request. When HIGH, reset relative logic
6	RW	0x0	lcdcpwm1_srstn_req lcdc_pwm1 software reset request. When HIGH, reset relative logic
5	RW	0x0	lcdcpwm0_srstn_req lcdc_pwm0 software reset request. When HIGH, reset relative logic
4	RW	0x0	gic_srstn_req GIC software reset request. When HIGH, reset relative logic
3	RW	0x0	pd_core_mp_axi_srstn_req pd_croe periph axi software reset request. When HIGH, reset relative logic
2	RW	0x0	pd_core_apb_noc_srstn_req pd_core APB software reset request. When HIGH, reset relative logic
1	RW	0x0	pd_core_ahb_noc_srstn_req PD_CORE AHB software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
0	RW	0x0	coresight_srstn_req coresight software reset request. When HIGH, reset relative logic

CRU_SOFTRST10_CON
Address: Operational Base + offset (0x01e0)
Internal software reset control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	c2c_host_srstn_req c2c host clk domain software reset request. When HIGH, reset relative logic
14	RW	0x0	crypto_srstn_req crypto working clk domain software reset request. When HIGH, reset relative logic
13:12	RO	0x0	reserved
11	RW	0x0	ddrmsch1_srstn_req DDR1 memory scheduler software reset request. When HIGH, reset relative logic
10	RW	0x0	ddrmsch0_srstn_req DDR0 memory scheduler software reset request. When HIGH, reset relative logic
9	RW	0x0	ddrphy1_ctl_srstn_req DDR1 PUB software reset request. When HIGH, reset relative logic
8	RW	0x0	ddrctrl1_psrstn_req DDR controller1 APB software reset request. When HIGH, reset relative logic
7	RW	0x0	ddrctrl1_srstn_req DDR controller1 software reset request. When HIGH, reset relative logic
6	RW	0x0	ddrphy1_psrstn_req DDR PHY1 APB software reset request. When HIGH, reset relative logic
5	RW	0x0	ddrphy1_srstn_req DDR PHY1 software reset request. When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
4	RW	0x0	ddrphy0_ctl_srstn_req DDR0 PUB software reset request. When HIGH, reset relative logic
3	RW	0x0	ddrctrl0_psrstn_req DDR controller0 APB software reset request. When HIGH, reset relative logic
2	RW	0x0	ddrctrl0_srstn_req DDR controller0 software reset request. When HIGH, reset relative logic
1	RW	0x0	ddrphy0_psrstn_req DDR PHY0 APB software reset request. When HIGH, reset relative logic
0	RW	0x0	ddrphy0_srstn_req DDR PHY0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST11_CON
Address: Operational Base + offset (0x01e4)
Internal software reset control register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	tsp_27m_srstn_req TSP 27M lock domain software reset request. When HIGH, reset relative logic
14	RW	0x0	tsp_clkin1_srstn_req TSP clockin1 software reset request. When HIGH, reset relative logic
13	RW	0x0	tsp_clkin0_srstn_req TSP clockin 0 software reset request. When HIGH, reset relative logic
12	RW	0x0	tsp_srstn_req tsp software reset request. When HIGH, reset relative logic
11	RW	0x0	ps2c_srstn_req ps2 controlor software reset request. When HIGH, reset relative logic
10	RW	0x0	simc_srstn_req cim card controlor software reset request. When HIGH, reset relative logic
9:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	uart4_srstn_req UART4 software reset request. When HIGH, reset relative logic
6	RW	0x0	uart3_srstn_req UART3 software reset request. When HIGH, reset relative logic
5	RW	0x0	uart2_srstn_req UART2 software reset request. When HIGH, reset relative logic
4	RW	0x0	uart1_srstn_req UART1 software reset request. When HIGH, reset relative logic
3	RW	0x0	uart0_srstn_req UART0 software reset request. When HIGH, reset relative logic
2	RW	0x0	lcdc1_dsrstn_req LCDC1 DCLK software reset request. When HIGH, reset relative logic
1	RW	0x0	lcdc1_hsrstn_req LCDC1 AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	lcdc1_asrstn_req LCDC1 AXI software reset request. When HIGH, reset relative logic

CRU_MISC_CON
Address: Operational Base + offset (0x01e8)
SCU control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	testclk_sel Output clock selection for test 4'b0000: aclk_periph 4'b0001: clk_core 4'b0010: aclk_vio0 4'b0011: clk_ddrphy 4'b0100: aclk_vcodec 4'b0101: aclk_gpu 4'b0110: clk_rga_core 4'b0111: aclk_cpu 4'b1000: 24MHz 4'b1001: 27MHz 4'b1010: 32KHz 4'b1011: clk_wifi(16.368MHz) 4'b1100: dclk_lcdc0 4'b1101: dclk_lcdc1 4'b1110: clk_isp_jpeg 4'b1111: clk_isp
7:0	RO	0x0	reserved

CRU_GLB_CNT_TH
Address: Operational Base + offset (0x01ec)
global reset wait counter threshold

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x064	glb_rst_cnt_th Global soft reset counter threshold

CRU_GLB_RST_CON
Address: Operational Base + offset (0x01f0)
global reset trigger select

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	pmu_glb_srst_ctrl pmu reset by global soft reset select 2'b00: pmu reset by first global soft reset 2'b01: pmu reset by second global soft reset 2'b10: pmu not reset by any global soft reset
1	RW	0x0	wdt_glb_srst_ctrl watch_dog trigger global soft reset select 1'b0: watch_dog trigger second global reset 1'b1: watch_dog trigger first global reset

Bit	Attr	Reset Value	Description
0	RW	0x0	tsadc_glb_srst_ctrl TSADC trigger global soft reset select 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

CRU_GLB_RST_ST
Address: Operational Base + offset (0x01f8)
global reset status

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	W1C	0x0	snd_glb_wdt_rst_st second global watch_dog triggered reset flag 1'b0: last hot reset is not second global watch_dog triggered reset 1'b1: last hot reset is second global watch_dog triggered reset
4	W1C	0x0	fst_glb_wdt_rst_st first global watch_dog triggered reset flag 1'b0: last hot reset is not first global watch_dog triggered reset 1'b1: last hot reset is first global watch_dog triggered reset
3	W1C	0x0	snd_glb_tsadc_rst_st second global TSADC triggered reset flag 1'b0: last hot reset is not second global TSADC triggered reset 1'b1: last hot reset is second global TSADC triggered reset
2	W1C	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: last hot reset is not first global TSADC triggered reset 1'b1: last hot reset is first global TSADC triggered reset
1	W1C	0x0	snd_glb_rst_st second global rst flag 1'b0: last hot reset is not second global rst 1'b1: last hot reset is second global rst
0	W1C	0x0	fst_glb_rst_st first global rst flag 1'b0: last hot reset is not first global rst 1'b1: last hot reset is first global rst

CRU_SDMMC_CON0*
Address: Operational Base + offset (0x0200)

sdmmc control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdmmc_drv_sel sdmmc drive select sdmmc drive select
10:3	WO	0x00	sdmmc_drv_delaynum sdmmc drive delay number sdmmc drive delay number
2:1	WO	0x1	sdmmc_drv_degree sdmmc drive degree sdmmc drive degree
0	WO	0x0	sdmmc_init_state sdmmc initial state sdmmc initial state

CRU_SDMMC_CON1*

Address: Operational Base + offset (0x0204)

sdmmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdmmc_sample_sel sdmmc sample select sdmmc sample select
9:2	WO	0x00	sdmmc_sample_delaynum sdmmc sample delay number sdmmc sample delay number
1:0	WO	0x0	sdmmc_sample_degree sdmmc sample degree sdmmc sample degree

CRU_SDIO0_CON0*

Address: Operational Base + offset (0x0208)

sdio0 control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdio0_drv_sel sdio0 drive select sdio0 drive select
10:3	WO	0x00	sdio0_drv_delaynum sdio0 drive delay number sdio0 drive delay number
2:1	WO	0x1	sdio0_drv_degree sdio0 drive degree sdio0 drive degree
0	WO	0x0	sdio0_init_state sdio0 initial state sdio0 initial state

CRU_SDIO0_CON1*
Address: Operational Base + offset (0x020c)
sdio0 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdio0_sample_sel sdio0 sample select sdio0 sample select
9:2	WO	0x00	sdio0_sample_delaynum sdio0 sample delay number sdio0 sample delay number
1:0	WO	0x0	sdio0_sample_degree sdio0 sample degree sdio0 sample degree

CRU_SDIO1_CON0*
Address: Operational Base + offset (0x0210)
sdio1 control0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	sdio1_drv_sel sdio1 drive select sdio1 drive select
10:3	WO	0x00	sdio1_drv_delaynum sdio1 drive delay number sdio1 drive delay number
2:1	WO	0x1	sdio1_drv_degree sdio1 drive degree sdio1 drive degree
0	WO	0x0	sdio1_init_state sdio1 initial state sdio1 initial state

CRU_SDIO1_CON1*
Address: Operational Base + offset (0x0214)
sdio1 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	sdio1_sample_sel sdio1 sample select sdio1 sample select
9:2	WO	0x00	sdio1_sample_delaynum sdio1 sample delay number sdio1 sample delay number
1:0	WO	0x0	sdio1_sample_degree sdio1 sample degree sdio1 sample degree

CRU_EMMC_CON0*
Address: Operational Base + offset (0x0218)
emmc control0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	WO	0x0	emmc_drv_sel emmc drive select emmc drive select
10:3	WO	0x00	emmc_drv_delaynum emmc drive delay number emmc drive delay number
2:1	WO	0x1	emmc_drv_degree emmc drive degree emmc drive degree
0	WO	0x0	emmc_init_state emmc initial state emmc initial state

CRU_EMMC_CON1*
Address: Operational Base + offset (0x021c)
emmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	WO	0x0	emmc_sample_sel emmc sample select emmc sample select
9:2	WO	0x00	emmc_sample_delaynum emmc sample delay number emmc sample delay number
1:0	WO	0x0	emmc_sample_degree emmc sample degree emmc sample degree

**Notes: CRU_SDMMC_CON0/1, CRU_SDIO1_CON0/1, CRU_SDIO0_CON0/1, CRU_EMMC_CON0/1, detail description please refer to chapter15 Mobile Storage Host Controller 15.6.10.*

3.8 Timing Diagram

Power on reset timing is shown as follow:

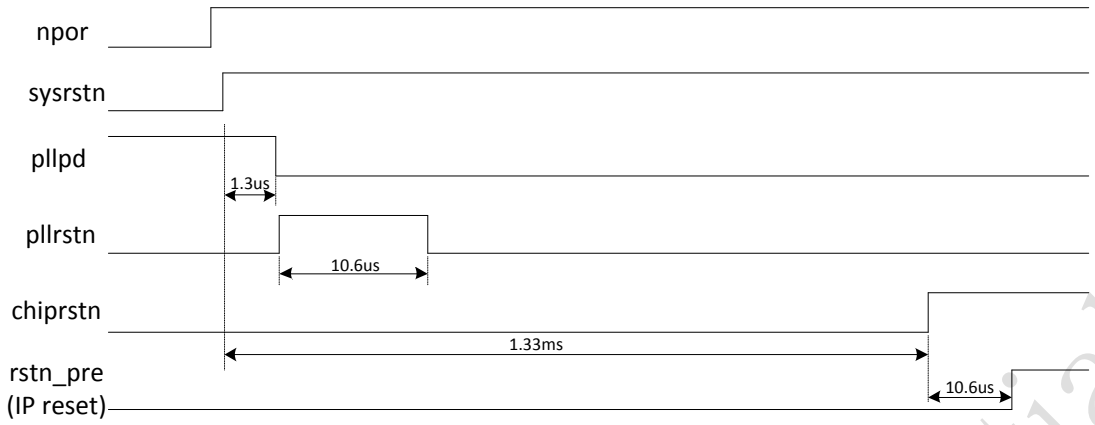

Fig. 3-8 Chip Power On Reset Timing Diagram

Npor is hardware reset signal from out-chip and power-off mode wakeup reset from PMU, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the power down signal (pllpd) must be high when reset, and maintains high for more then 1us when sysrstn de-active. Then PLL reset signals (pllrstn) are asserted for about 10.6us, and PLLs start to lock when pllrstn de-assert, and consume about 1330us to lock. So the system will wait about 1330us, then de-active reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 256 cycles (10.7us) to de-active signal rstn_pre, which is used to generate power on reset of all IP.

3.9 Application Notes

3.9.1 PLL usage

A. PLL output frequency configuration

The output frequency Fout is related to the input frequency Fin by:

Fout = ((Fin /NR) * NF)/ NO

Fout is clock output of PLL, and Fin is clock input of PLL from external oscillators (24MHz). Another, other factors such as NF, NR, NO can be configured by programming CRU_APLL_CONi, CRU_DPLL_CONi, CRU_CPLL_CONi and CRU_GPLL_CONi registers (i=0,1,2), and their value will affect Fout as follows.

(1) CLKR: A 6-bit bus that selects the values 1-64 for the reference divider (NR)

NR = CLKR[5:0] + 1
Example:
/1 pgm 000000
/4 pgm 000011
/8 pgm 000111

(2) CLKF: A 13-bit bus that selects the values 1-4096 for the PLL multiplication factor (NF)

NF = CLKF[12:0] + 1
Example:
X1 pgm 0000000000000
X2 pgm 0000000000001

X4096 pgm 0111111111111

(3) CLKOD: A 4-bit bus that selects the value1,2-16(even only) for the PLL post VCO divider (NO)

NO = CLKOD[3:0] + 1
Example:
/1 pgm 0000
/2 pgm 0001
/4 pgm 0011
/8 pgm 0111

(4) BWADJ: A 12-bit bus that selects the values 1-4096 for the bandwidth divider (NB)

NB = BWADJ[11:0] + 1
Example:
/1 pgm 000000000000
/4 pgm 000000000011
/8 pgm 000000000111

The recommended setting of NB: NB = NF / 2.

B. PLL frequency range requirement

If different CLKR, CLKF and CLKOD configuration value cause internal out of range, unpredicted result will be caused.

Fin value range requirement: 269kHz – 2200MHz
Fref = Fin/NR value range requirement: 269kHz – 2200MHz
Fvco = (Fin/NR)*NF value range requirement: 440MHz – 2200MHz
Fout = ((Fin/NR)*NF)/NO value range requirement: 27.5MHz – 2200MHz

C. PLL setting consideration

Optimization of the PLL settings for jitter < +/- 2.5% of the output period/sq rt(NO) require running the VCO at maximum frequency and dividing down using the NO divider to get the required Fout, i.e. maximum NO.

Optimization for minimum power (Fvco/1100MHz * 3.3 mA) requires setting the VCO frequency at the minimum frequency and using the lowest NO setting.

These two values, minimum jitter or minimum power will determine your choice of settings.

A larger value of input divider NR gives a longer lock time, and higher long term as well as period jitter. It is better to use a lower value of NR where possible.

3.9.2 PLL frequency change method

When the PLL settings are changed, it has to reset PLL by programming registers CRU_APLL_CON3, CRU_DPLL_CON3, CRU_CPLL_CON3, CRU_GPLL_CON3, CRU_NPLL_CON3, and reserve at least 5us after valid settings, referring to the following figure.

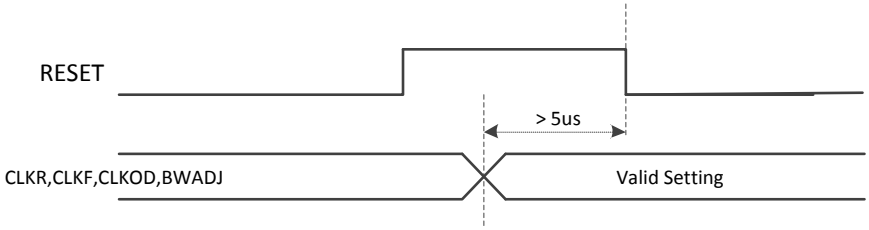

Fig. 3-9 PLL setting change timing

Before set some factors such as NR/NF/NO/BS to change PLL output frequency, you must change chip from normal to slow mode by programming CRU_MODE_CON. Then until PLL is lock state by checking GRF_SOC_STATUS0[8:5] register, or after delay about (NR * 500) / Fin, you can change PLL into normal mode.

3.9.3 Fractional divider usage

To get specific frequency, clocks of I2S, SPDIF, UART, HSADC can be generated by fractional divider. Generally you must set that denominator is 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock like I2S, UART and HSADC.

All the fractional divider has auto-gating control. When fractional divider is not selected, the divider clock is gated. So fractional divider must be selected before changing configuration.

3.9.4 Global software reset

Two global software resets are designed in this chip, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-deasserted by hardware.

TSADC, WDT and PMU also can trigger glb_srstn_1 or glb_srstn_2.

CRU_GLB_RST_CON controls which global soft-reset will be triggered.

After global reset, the reset trigger source can be check in CRU_GLB_RST_ST.

glb_srstn_1 resets almost all chip logic except PMU_SYS_REG0~3, which can be used to store something when reset.

glb_srstn_2 resets almost all chip logic except PMU_SYS_REG0~3, GRF and GPIOs.

3.9.5 Pre-shift for test

Pre-shift registers is designed in this chip for flexible test.

The key configuration registers can be shifted with a initial value in testmode. The pre-shift registers including 191 bit pre_shift_test_reg.

The following table describes the pre-shift registers of the design.

Name	Bit number	Default value	Description
armpll_clkr	pre_shift_test_reg[5:0]	6'd0	armpll_clkr control

armpll_clkf	pre_shift_test_reg[18:6]	13'd199	armpll_clkf control
armpll_bwadj	pre_shift_test_reg[30:19]	12'd49	armpll_bwadj control
armpll_clkod	pre_shift_test_reg[35:31]	5'd1	armpll_clkod control
ddrpll_clkr	pre_shift_test_reg[41:36]	6'd1	ddrpll_clkr control
ddrpll_clkf	pre_shift_test_reg[54:42]	13'd99	ddrpll_clkf control
ddrpll_bwadj	pre_shift_test_reg[66:55]	12'd49	ddrpll_bwadj control
ddrpll_clkod	pre_shift_test_reg[71:67]	5'd5	ddrpll_clkod control
codecpll_clkr	pre_shift_test_reg[77:72]	6'd1	codecpll_clkr control
codecpll_clkf	pre_shift_test_reg[90:78]	13'd99	codecpll_clkf control
codecpll_bwadj	pre_shift_test_reg[102:91]	12'd49	codecpll_bwadj control
codecpll_clkod	pre_shift_test_reg[107:103]	5'd5	codecpll_clkod control
generalpll_clkr	pre_shift_test_reg[113:108]	6'd1	generalpll_clkr control
generalpll_clkf	pre_shift_test_reg[126:114]	13'd99	generalpll_clkf control
generalpll_bwadj	pre_shift_test_reg[138:127]	12'd49	generalpll_bwadj control
generalpll_clkod	pre_shift_test_reg[143:139]	5'd5	generalpll_clkod control
newpll_clkr	pre_shift_test_reg[149:144]	6'd1	newpll_clkr control
newpll_clkf	pre_shift_test_reg[162:150]	13'd99	newpll_clkf control
newpll_bwadj	pre_shift_test_reg[174:163]	12'd49	newpll_bwadj control
newpll_clkod	pre_shift_test_reg[179:175]	5'd5	newpll_clkod control
testclk_sel	pre_shift_test_reg[182:180]	3'd0	testclk_out select in testmode
aclk_core_m_div_con	pre_shift_test_reg[185:183]	3'd1	Aclk_m divider configuration in testmode
Io_sr	pre_shift_test_reg[186]	1'd1	IO slew rate
io_drive	pre_shift_test_reg[188:187]	2'b10	IO drive configuration
Io_vsel	pre_shift_test_reg[189]	1'd0	IO voltage select
Io_smt	pre_shift_test_reg[190]	1'd0	IO smt control

Pre-shift relative controls IO are as follow.

Name	IO	description
Pre_shift_datain	IO_UART3GPSsout_GPSsig_HSADCT1data1_GPIO30gpio7b0	Pre-shift data in
Pre_shift_en	IO_UART3GPSctsn_GPSrfclk_GPST1clk_GPIO30gpio7b1	Pre-shift enable
Pre_shift_clk	IO_UART3GPSrtsn_USBdrvvbus0_GPIO30gpio7b2	Pre-shift clock
Pre-shift_default_select	IO_USBdrvvbus1_EDPhotplug_GPIO30gpio7b3	1'b0: pre_shift use default value; 1'b1: pre_shift use shift in value;

Pre-shift_select	IO_ISPshutteren_SPI1clk_GPIO30gpio7b4	1’b0: disable, testmode do not use pre-shift config value; use internal 6 configs. 1’b1: enable, testmode use pre-shift config value;