

Chapter 4 Power Management Unit (PMU)

4.1 Overview

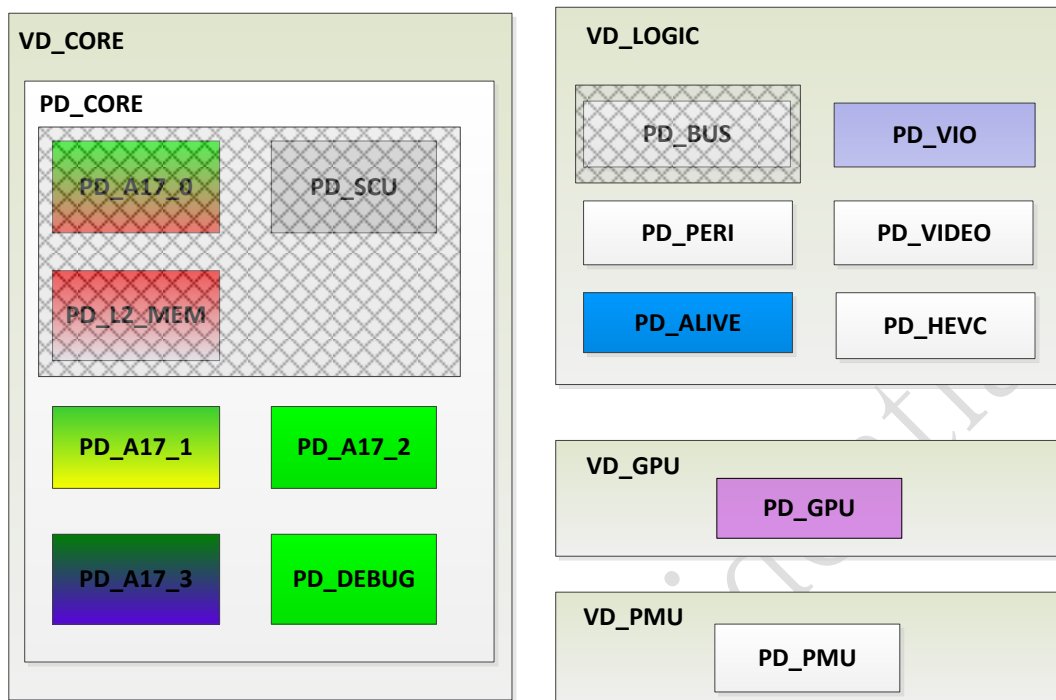
In order to meet high performance and low power requirements, a power management unit is designed for saving power when RK3288 in low power mode. The RK3288 PMU is dedicated for managing the power of the whole chip.

4.1.1 Features

- Support 4 voltage domains including VD_CORE, VD_LOGIC, VD_GPU and VD_PMU
- Support 15 separate power domains in the whole chip, which can be power up/down by software based on different application scenes
- In low power mode, the pmu could power up/down pd_A17_0, pd_scu, vd_core, and pd_bus by hardware
- Support CORTEX-A17 core source clock gating in low power mode
- Support global interrupt disable in low power mode
- Support PLLs power down/up in low power mode
- Support VD_CORE/VD_LOGIC power down/up in low power mode
- Support pd_alive clock switch to 32KHz in low power mode
- Support pd_pmu clock switch to 32KHz request in low power mode
- Support OSC enable/disable request in low power mode
- Support to clamp all VD_LOGIC output before power off it in low power mode
- Support wakeup reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR IO retention in low power mode
- Support DDR IO power off in low power mode
- Support DDR controller clock auto gating in low power mode
- Support to send idle requests to all NIU in the SoC (details will be described later)
- A group of configurable counter in PMU for HW control (such as PLL, PMIC, DDRIO and so on)
- Support varies configurable wakeup source for low power mode

4.2 Block Diagram

4.2.1 power domain partition



Note:
VD_* : voltage domain
PD_* : power domain

Fig. 4-1 Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists all the power domains.

Table 4-1 RK3288 Power Domain and Voltage Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE (PD_CORE system)	PD_A17_0	A17 primary core logic, L1C and noen
	PD_A17_1	A17 slave core 1 logic, L1C and noen
	PD_A17_2	A17 slave core 2 logic, L1C and noen
	PD_A17_3	A17 slave core 3 logic, L1C and noen
	PD_SCU	SCU RAM, SCU, GIC, Periphral, L2 controller
	PD_DEBUG	A17 Debug
	PD_MEM	L2 Cache
VD_LOGIC	PD_BUS	Soc architecture subsystem, include soc architecture (NOC) , eFuse, TZPC, ROM, DMAC_BUS, Crypto, Host, Timer(6ch), PWM(0~3), UART_DBG, I2C, DDR_PCTL, I2S, Spdif, Internal Memory(96K)
	PD_PERI	Peripheral subsystem , include DMAC_PERI, GMAC, NANDC0/1, HSIC/USB Host0/USB Host1/ USB OTG, SDMMC/SDIO0/SDIO1/eMMC, HSADC, PS2C, TSADC, UART, I2C, SPI, GPS, TSP
	PD_VIO	Video input/output system, include VOPBIG,

		VOPLIT, ISP, IEP, RGA, MIPI-CSI, MIPI-DSI, LVDS, HDMI, eDP
	PD_ALIVE	CRU, GRF, GPIO 1~8, TIMER, WDT
	PD_HEVC	HEVC
	PD_VIDEO	Video Encode&Decode , include VEPU, VDPU
VD_GPU	PD_GPU	GPU
VD_PMU	PD_PMU	PMU, SRAM(4K), Secure GRF, GPIO0

Notes: "Always on" means that their power supply can be switched off only by external PMIC module. Only one "always on" power domain is in a voltage domain.

4.2.2 PMU block diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB interface and register, which can accept the system configuration
- Low Power State Control, which generate low power control signals.
- Power Switch Control, which control all power domain switch

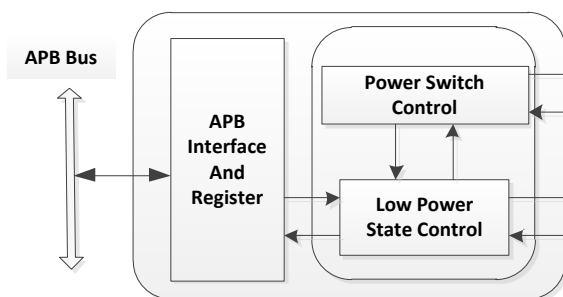


Fig. 4-2 PMU Bock Diagram

4.3 Power Switch Timing Requirement

The following table describe the switch time for power down and power up progress of each power domain. This table gives the time range, and each power domain switch time will be more than the min time and less than the max time.

Table 4-2 Power Switch Timing

Power domain	type	Power down Switch Timing① (ns)	Power up Switch Timing① (ns)
PD_A17_0	min	170.3	132.4
	max	306.7	237.5
PD_A17_1	min	170.3	132.4
	max	306.7	237.5
PD_A17_2	min	181.5	140.7
	max	326.2	251.9
PD_A17_3	min	181.5	140.7
	max	326.2	251.9
PD_DEBUG	min	169.4	131.7
	max	77.3	60
PD_BUS	min	169.4	131.7
	max	313.6	247
PD_PERI	min	103.7	80.5
	max	199.0	156.1

PD_VIO	min	280.6	217.5
	max	518.5	407.8
PD_VIDEO	min	315.4	244.2
	max	586.2	460.4
PD_GPU	min	470.2	364
	max	871.4	684.1
PD_HEVC	min	33.4	25.9
	max	62.4	49
	max	65.6	51.5

Notes: the power switch timing is just the chip power electrical parameter, this is not the parameter for the software to determine the power domain status. The software need to check each power domain status register to determine the power status.

4.4 Function Description

4.4.1 Normal Mode

First of all, we define two modes of power for chip, normal mode and low power mode.

In normal mode, the PMU can power off/on all power domain (except pd_A17_0 and pd_bus) by setting PMU_PWRDN_CON register. At same, pmu can send idle request for every power domain by setting PMU_IDLE_REQ register.

Don't set pd_A17_0 and pd_bus power off or send idle_req_core and idle_req_bus in normal mode. This will cause the system to not work properly.

Basically, there are 2 configurations that software can do in normal mode to save power.

- Configure DDR to self-refresh, DDR IO retention and DDR IO power off
- Power down power domains

The first one will save power consumption of using DDR controller and DDR IO. For avoiding confliction, the software must make sure the execution code of this step is not in DDR.

The second one will save power of the power domain which software is shutting down.

4.4.2 Low Power Mode

PMU can work in the Low Power Mode by setting bit[0] of PMU_PWRMODE_CON register. After setting the register, PMU would enter the Low Power mode. In the low power mode, pmu will auto power on/off the specified power domain, send idle req to specified power domain, shut down/up pll and so on. All of above are configurable by setting corresponding registers.

Table 4-3 Low Power State

Num	Hardware Flow	Description of Flow	Corresponding Register
0	NORMAL	in normal	
1	L2FLUSH_REQ	send L2 cache flush request	bit[3] of PMU_PWRMODE_CON
2	STANDBYL2	wait L2 cache standby	
3	A17_CLK_DIS	close A17 clock	bit[1] of PMU_PWRMODE_CON
4	TRANS_NO_FIN	wait the corresponding noc interface end the transaction	PMU_PMRMODE_CON1
5	SREF_ENTER	enter DDR self-refresh	bit[16:15] of PMU_PWRMODE_CON
6	DDR_IO_RET	ddr io retention	bit[18:17] of PMU_PWRMODE_CON
7	DDR_IO_PWROFF	ddr io power off	bit[20:19] of PMU_PWRMODE_CON
8	BUS_PWRDN	pd_bus power down	bit[4] of PMU_PWRMODE_CON
9	A17_0_PWRDN	pd_a17_0 power down	bit[5] of PMU_PWRMODE_CON
10	L2MEM_PWRDN	pd_l2mem power down (vd_core power down)	bit[6] of PMU_PWRMODE_CON
11	ALIVE_PMU_LF	pd_alive& pd_pmu switch to 32KHz clock	bit[11:10] of PMU_PWRMODE_CON
12	PLL_PWRDN	pll power down	bit[7] of PMU_PWRMODE_CON
13	INPUT_CLAMP	isolation cell input clamp	bit[13] of PMU_PWRMODE_CON
14	POWEROFF	chip power off	bit[8] of PMU_PWRMODE_CON
15	24M_OSC_DIS	close 24MHz OSC	bit[12] of PMU_PWRMODE_CON
16	WAIT_WAKEUP	wait wakeup source	PMU_WAKEUP_CFG0/1
17	WAKEUP_RESET	send reset after wakeup	
18	EXT_PWRUP	pmic power up whole chip	
19	RELEASE_CLAMP	release isolation cell clamp	
20	24M_OSC_EN	open 24MHz OSC	
21	ALIVE_PMU_HF	switch pd_alive and pd_pmu back to 24MHz	
22	WAKEUP_RESET_CLR	release wakeup reset	
23	PLL_PWRUP	PLL power up	
24	BUS_PWRUP	PD_BUS power up	
25	DDR_IO_PWRUP	ddr io power up	
26	SREF_EXIT	exit ddr self-refresh	
27	L2MEM_PWRUP	pd_l2mem power up	
28	A17_0_PWRUP	pd_a17_0 power up	
29	TRANS_RESTORE	restore the transaction	
30	A17_CLK_EN	enable a17 clock	

The Low Power mode have three steps:

- Enter Low Power mode, there are some sub-steps in the enter step, every sub-step can be enable/disable by setting the corresponding register.
- Wait wakeup, you can select the wakeup source by setting PMU_WAKEUP_CFG0/1 register
- Exit Low Power mode, the sub-step are executed depend on whether they were executed in enter low power step.

4.4.3 Wakeup source of AP

The wakeup source is a group of signals which can trigger PMU from power mode to normal mode, such as SDMMC detect, core interrupt, GPIO0, and gpio interrupt.

Table 4-4 Wakeup Source

Num	Wakeup Source	Description
1	software control	software control (in normal mode)
2	arm interrupt	a17 interrupt
3	pmu_gpio	gpio0, in pd_pmu
4	sdmmc0	detect_n of sdmmc0
5	gpio int	gpio interrupt outside of pd_pmu

If software expect PMU be woken up from power mode by a wake up source, it should be enabled by write 1 to the corresponding bit of PMU_WAKEUP_CFG0/1 register before entering into power mode.

Technically, wakeup source can be used in every power mode if only the path from wakeup source to PMU is not shut down.

4.5 Register Description

4.5.1 Register Summary

Name	Offset	Size	Reset Value	Description
PMU_WAKEUP_CFG0	0x0000	W	0x00000000	PMU wake-up source configuration register0
PMU_WAKEUP_CFG1	0x0004	W	0x00000000	PMU wake-up source configuration register1
PMU_PWRDN_CON	0x0008	W	0x00000000	System power gating configuration register
PMU_PWRDN_ST	0x000c	W	0x00000000	System power gating status register
PMU_IDLE_REQ	0x0010	W	0x00000000	PMU Noc idle req control
PMU_IDLE_ST	0x0014	W	0x00000000	PMU Noc idle status
PMU_PWRMODE_CON	0x0018	W	0x00000000	PMU configuration register in power mode flow
PMU_PWR_STATE	0x001c	W	0x00000000	PMU Low power mode state
PMU_OSC_CNT	0x0020	W	0x00005dc0	24MHz OSC stabilization counter threshold
PMU_PLL_CNT	0x0024	W	0x10004000	PLL lock counter threshold
PMU_STABL_CNT	0x0028	W	0x00005dc0	External PMU stabilization counter threshold
PMU_DDR0IO_PWRON_CNT	0x002c	W	0x00005dc0	DDR0 IO power on counter threshold
PMU_DDR1IO_PWRON_CNT	0x0030	W	0x00005dc0	DDR1 IO power on counter threshold
PMU_CORE_PWRDOWN_CNT	0x0034	W	0x00005dc0	CORE domain power down waiting counter in sleep mode
PMU_CORE_PWRUP_CNT	0x0038	W	0x00005dc0	CORE domain power up waiting counter in sleep mode
PMU_GPU_PWRDOWN_CNT	0x003c	W	0x00005dc0	GPU domain power down waiting counter in sleep mode
PMU_GPU_PWRUP_CNT	0x0040	W	0x00005dc0	GPU domain power up waiting counter in sleep mode
PMU_WAKEUP_RST_CLR_CNT	0x0044	W	0x00005dc0	Wakeup reset deassert state wait counter in power off mode
PMU_SFT_CON	0x0048	W	0x00000000	PMU Software control in normal mode
PMU_DDR_SREF_ST	0x004c	W	0x00000000	PMU DDR self refresh status
PMU_INT_CON	0x0050	W	0x00000000	PMU interrupt configuration register
PMU_INT_ST	0x0054	W	0x00000000	PMU interrupt status register

Name	Offset	Size	Reset Value	Description
PMU_BOOT_ADDR_SEL	0x0058	W	0x00005dc0	boot_addr_sel in power mode
PMU_GRF_CON	0x005c	W	0x00000008	grf control register
PMU_GPIO_SR	0x0060	W	0x00020000	GPIO slew rate control
PMU_GPIO0_A_PULL	0x0064	W	0x0000555a	GPIO0A input to PU/PD programming section
PMU_GPIO0_B_PULL	0x0068	W	0x00005555	GPIO0B input to PU/PD programming section
PMU_GPIO0_C_PULL	0x006c	W	0x00000015	GPIO0C input to PU/PD programming section
PMU_GPIO0_A_DRV	0x0070	W	0x0000555a	GPIO0A Drive strength selector
PMU_GPIO0_B_DRV	0x0074	W	0x00005555	GPIO0B Drive strength selector
PMU_GPIO0_C_DRV	0x0078	W	0x00000015	GPIO0C Drive strength selector
PMU_GPIO_OP	0x007c	W	0x00000000	GPIO0 output value
PMU_GPIO0_SEL18	0x0080	W	0x00000006	gpio0 1.8v/3.3v sel
PMU_GPIO0_A_IOMUX	0x0084	W	0x00000000	GPIO0A iomux sel
PMU_GPIO0_B_IOMUX	0x0088	W	0x00000000	GPIO0B iomux sel
PMU_GPIO0_C_IOMUX	0x008c	W	0x00000000	GPIO0C iomux sel
PMU_PWRMODE_CON1	0x0090	W	0x00000000	PMU power mode controll1
PMU_SYS_REG0	0x0094	W	0x00000000	PMU system register0
PMU_SYS_REG1	0x0098	W	0x00000000	PMU system register1
PMU_SYS_REG2	0x009c	W	0x00000000	PMU system register2
PMU_SYS_REG3	0x00a0	W	0x00000000	PMU system register3

4.5.2 Detail Register Description

PMU_WAKEUP_CFG0

Address: Operational Base + offset (0x0000)

PMU wake-up source configuration register0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0c_2_wakeup_en GPIO0c bit2 wakeup enable 1'b0: disable 1'b1: enable
17	RW	0x0	gpio0c_1_wakeup_en GPIO0c bit1 wakeup enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
16	RW	0x0	gpio0c_0_wakeup_en GPIO0c bit0 wakeup enable 1'b0: disable 1'b1: enable
15	RW	0x0	gpio0b_7_wakeup_en GPIO0b bit7 wakeup enable 1'b0: disable 1'b1: enable
14	RW	0x0	gpio0b_6_wakeup_en GPIO0b bit6 wakeup enable 1'b0: disable 1'b1: enable
13	RW	0x0	gpio0b_5_wakeup_en GPIO0b bit5 wakeup enable 1'b0: disable 1'b1: enable
12	RW	0x0	gpio0b_4_wakeup_en GPIO0 bit12 wakeup enable 1'b0: disable 1'b1: enable
11	RW	0x0	gpio0b_3_wakeup_en GPIO0b bit3 wakeup enable 1'b0: disable 1'b1: enable
10	RW	0x0	gpio0b_2_wakeup_en GPIO0b bit2 wakeup enable 1'b0: disable 1'b1: enable
9	RW	0x0	gpio0b_1_wakeup_en GPIO0b bit1 wakeup enable 1'b0: disable 1'b1: enable
8	RW	0x0	gpio0b_0_wakeup_en GPIO0b bit0 wakeup enable 1'b0: disable 1'b1: enable
7	RW	0x0	gpio0a_7_wakeup_en GPIO0a bit7 wakeup enable 1'b0: disable 1'b1: enable
6	RW	0x0	gpio0a_6_wakeup_en GPIO0a bit6 wakeup enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0a_5_wakeup_en GPIO0a bit5 wakeup enable 1'b0: disable 1'b1: enable
4	RW	0x0	gpio0a_4_wakeup_en GPIO0a bit4 wakeup enable 1'b0: disable 1'b1: enable
3	RW	0x0	gpio0a_3_wakeup_en GPIO0a bit3 wakeup enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio0a_2_wakeup_en GPIO0a bit2 wakeup enable 1'b0: disable 1'b1: enable
1	RW	0x0	gpio0a_1_wakeup_en GPIO0a bit1 wakeup enable 1'b0: disable 1'b1: enable
0	RW	0x0	gpio0a_0_wakeup_en GPIO0a bit0 wakeup enable 1'b0: disable 1'b1: enable

PMU_WAKEUP_CFG1

Address: Operational Base + offset (0x0004)

PMU wake-up source configuration register1

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	gpoint_wakeup_en GPIO Interrupt wake enable 1'b0: disable 1'b1: enable
2	RW	0x0	sdmmc0_wakeup_en SDMMC0 wake-up enable 1'b0: disable 1'b1: enable
1	RW	0x0	pmu_gpio_wakeup_type GPIO in pmu wakeup type 1'b0: posedge 1'b1: negedge
0	RW	0x0	armint_wakeup_en ARM interrupt wake-up enable 1'b0: disable 1'b1: enable

PMU_PWRDN_CON

Address: Operational Base + offset (0x0008)

System power gating configuration register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	PD_HEVC_DWN_EN Power domain HEVC power down enable 1'b0: power on 1'b1: power off
13	RW	0x0	CHIP_PWROFF_EN software conifg power off chip logic 1'b1: power off 1'b0: not power off
12	RW	0x0	CORE_PWROFF_EN software conifg power off pd_core 1'b1: power off 1'b0: not power off
11	RW	0x0	PD_SCU_DWN_EN Power domain SCU power down enable 1'b0: power on 1'b1: power off
10	RO	0x0	reserved
9	RW	0x0	PD_GPU_DWN_EN Power domain GPU power down enable 1'b0: power on 1'b1: power off
8	RW	0x0	PD_VIDEO_DWN_EN Power domain VIDEO power down enable 1'b0: power on 1'b1: power off
7	RW	0x0	PD_VIO_DWN_EN Power domain VIO power down enable 1'b0: power on 1'b1: power off
6	RW	0x0	PD_PERI_DWN_EN Power domain PERI power down enable 1'b0: power on 1'b1: power off
5	RW	0x0	PD_BUS_DWN_EN Power domain BUS power down enable 1'b0: power on 1'b1: power off
4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	PD_A17_3_DWN_EN Power Domain A17 slave core 3 power down enable 1'b0: power on 1'b1: power off
2	RW	0x0	PD_A17_2_DWN_EN Power Domain A17 slave core 2 power down enable 1'b0: power on 1'b1: power off
1	RW	0x0	PD_A17_1_DWN_EN Power domain A17 slave core 1 power down enable 1'b0: power on 1'b1: power off
0	RW	0x0	PD_A17_0_DWN_EN Power Domain A17 primary core power down enable 1'b0: power on 1'b1: power off

PMU_PWRDN_ST

Address: Operational Base + offset (0x000c)

System power gating status register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	l2_standbywfi
12	RW	0x0	l2_flush_done
11	RO	0x0	pd_scu_pwr_st Power domain SCU power status 1'b0: power on 1'b1: power off
10	RO	0x0	pd_hevc_pwr_st Power domain HEVC power status 1'b0: power on 1'b1: power off
9	RO	0x0	pd_gpu_pwr_st Power domain GPU power status 1'b0: power on 1'b1: power off
8	RO	0x0	pd_video_pwr_st Power domain VIDEO power status 1'b0: power on 1'b1: power off

Bit	Attr	Reset Value	Description
7	RO	0x0	pd_vio_pwr_st Power domain VIO power status 1'b0: power on 1'b1: power off
6	RO	0x0	pd_peri_pwr_st Power domain PERI power status 1'b0: power on 1'b1: power off
5	RO	0x0	pd_bus_pwr_st Power domain BUS power status 1'b0: power on 1'b1: power off
4	RO	0x0	reserved
3	RW	0x0	pd_A17_3_pwr_st Power domain A17 slave core 3 power status 1'b0: power on 1'b1: power off
2	RW	0x0	pd_A17_2_pwr_st Power domain A17 slave core 2 power status 1'b0: power on 1'b1: power off
1	RW	0x0	pd_A17_1_pwr_st Power domain A17 slave core 1 power status 1'b0: power on 1'b1: power off
0	RW	0x0	pd_A17_0_pwr_st Power domain A17 primary core power status 1'b0: power on 1'b1: power off

PMU_IDLE_REQ

Address: Operational Base + offset (0x0010)

PMU Noc idle req control

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	idle_req_hevc_cfg software config HEVC domain flush trasaction request 1'b1: idle req 1'b0: not idle req
8	RW	0x0	idle_req_cpup_cfg software config CPUP domain flush trasaction request 1'b1: idle req 1'b0: not idle req

Bit	Attr	Reset Value	Description
7	RW	0x0	idle_req_dma_cfg software config DMA domain flush transaction request 1'b1: idle req 1'b0: not idle req
6	RW	0x0	idle_req_alive_cfg software config ALIVE domain flush transaction request 1'b1: idle req 1'b0: not idle req
5	RW	0x0	idle_req_core_cfg software config CORE domain flush transaction request 1'b1: idle req 1'b0: not idle req
4	RW	0x0	idle_req_vio_cfg software config VIO domain flush transaction request 1'b1: idle req 1'b0: not idle req
3	RW	0x0	idle_req_video_cfg software config VIDEO domain flush transaction request 1'b1: idle req 1'b0: not idle req
2	RW	0x0	idle_req_gpu_cfg software config GPU domain flush transaction request 1'b1: idle req 1'b0: not idle req
1	RW	0x0	idle_req_peri_cfg software config PERI domain flush transaction request 1'b1: idle req 1'b0: not idle req
0	RW	0x0	idle_req_bus_cfg software config BUS domain flush transaction request 1'b1: idle req 1'b0: not idle req

PMU_IDLE_ST

Address: Operational Base + offset (0x0014)

PMU Noc idle status

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25	RW	0x0	idle_ack_hevc hevc domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
24	RW	0x0	idle_ack_cpup cpup domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
23	RW	0x0	idle_ack_dma dma domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
22	RW	0x0	idle_ack_alive ALIVE domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
21	RW	0x0	idle_ack_core core domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
20	RW	0x0	idle_ack_vio VIO domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
19	RW	0x0	idle_ack_video VIDEO domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
18	RW	0x0	idle_ack_gpu GPU domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
17	RW	0x0	idle_ack_peri PERI domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
16	RW	0x0	idle_ack_bus BUS domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
15:10	RO	0x0	reserved
9	RW	0x0	IDLE_HEVC HEVC domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish

Bit	Attr	Reset Value	Description
8	RW	0x0	IDLE_CPUP CPUP domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
7	RW	0x0	IDLE_DMA DMA domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
6	RW	0x0	IDLE_ALIVE ALIVE domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
5	RW	0x0	IDLE_CORE CORE domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
4	RW	0x0	IDLE_VIO VIO domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
3	RW	0x0	IDLE_VIDEO VIDEO domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
2	RW	0x0	IDLE_GPU GPU domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
1	RW	0x0	IDLE_PERI PERI domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
0	RW	0x0	IDLE_BUS BUS domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish

PMU_PWRMODE_CON

Address: Operational Base + offset (0x0018)

PMU configuration register in power mode flow

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	ddr1io_ret_de_req ddr1io retention de-assert request 1'b0: de-assert request 1'b1: not de-assert request

Bit	Attr	Reset Value	Description
21	RW	0x0	ddr0io_ret_de_req ddr0io retention de-assert request 1'b0: de-assert request 1'b1: not de-assert request
20	RW	0x0	ddrc1_gating_en ddrc1 clock auto gating after self-refresh in low power mode 1'b1: auto gating 1'b0: not auto gating
19	RW	0x0	ddr0_gating_en ddrc0 auto gating in low power mode 1'b0: disable 1'b1: enable
18	RW	0x0	ddr1io_ret_en ddr1 io ret enable in low power mode 1'b1: enable 1'b0: disable
17	RW	0x0	ddr0io_ret_en DDR0 IO retention function enable or not 1'b0: DDR0 IO retention disable 1'b1: DDR0 IO retention enable
16	RW	0x0	sref1_enter_en ddr1 enter self-refresh in low power mode 1'b1: enable 1'b0: disable
15	RW	0x0	sref0_enter_en DDR0 enter self-refresh enable in low power mode 1'b0: disable DDR0 enter self-refresh 1'b1: enable DDR0 enter self-refresh
14	RW	0x0	wakeup_reset_en wakeup reset enable if power up 1'b0: diable 1'b1: enable
13	RW	0x0	input_clamp_en input clamp enable if power off input clamp for PD_PMU enable if power off 1'b0: disable 1'b1: enable
12	RW	0x0	osc_24m_dis 24MHz OSC disable in low power mode 1'b0: 24MHz OSC enable 1'b1: 24MHz OSC disable

Bit	Attr	Reset Value	Description
11	RW	0x0	pmu_use_lf pmu domain clock switch to 32.768kHz enable 1'b0: not switch to 32.768kHz 1'b1: switch to 32.768kHz
10	RW	0x0	alive_use_lf ALIVE domain clock switch to 32.768kHz enable 1'b0: not switch to 32.768kHz 1'b1: switch to 32.768kHz
9	RW	0x0	pwroff_comb three power off signal combination 1'b0: not combine 1'b1: combine enable
8	RW	0x0	chip_pd_en chip power down enable in power mode flow 1'b0: chip power on 1'b1: chip power off
7	RW	0x0	pll_pd_en pll power down enable in power mode flow 1'b0: pll power on 1'b1: pll power off
6	RW	0x0	scu_en scu power down enable in power mode flow 1'b0: scu power on 1'b1: scu power off
5	RW	0x0	A17_0_pd_en A17_0 power down in power mode flow 1'b0: A17_0 power on 1'b1: A17_0 power off
4	RW	0x0	bus_pd_en bus power off enable in low power mode 1'b0: bus power on 1'b1: bus power off
3	RW	0x0	l2flush_en l2 flush enable 1'b1: l2 flush enable 1'b0: l2 flush disable
2	RW	0x0	global_int_disable Global interrupt disable 1'b0: enable global interrupt 1'b1: disable global interrupt

Bit	Attr	Reset Value	Description
1	RW	0x0	clk_core_src_gate_en A17 core clock source gating enable in idle mode 1'b0: enable 1'b1: disable
0	RW	0x0	power_mode_en power mode flow enable 1'b0: disable 1'b1: enable

PMU_PWR_STATE

Address: Operational Base + offset (0x001c)

PMU Low power mode state

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	A17_CLK_EN A17 source clock enable 1'b0: state not happened 1'b1: state happened
29	RW	0x0	TRANS_RESTORE noc trans restore 1'b0: state not happened 1'b1: state happened
28	RW	0x0	A17_0_PWRUP A17 core0 power up state 1'b0: state not happened 1'b1: state happened
27	RW	0x0	L2MEM_PWRUP pd_l2mem powerup state 1'b0: state not happened 1'b1: state happened
26	RW	0x0	SREF_EXIT ddr exit self-refresh 1'b0: state not happened 1'b1: state happened
25	RW	0x0	DDR_IO_PWRUP ddr io powerup state 1'b0: state not happened 1'b1: state happened
24	RW	0x0	BUS_PWRUP pd_bus powerup state 1'b0: state not happened 1'b1: state happened

Bit	Attr	Reset Value	Description
23	RW	0x0	PLL_PWRUP pll power up state 1'b0: state not happened 1'b1: state happened
22	RW	0x0	WAKEUP_RESET_CLR deassert wakeup reset 1'b0: state not happened 1'b1: state happened
21	RW	0x0	ALIVE_PMU_HF pd_alive & pd_pmu switch to normal clock 1'b0: state not happened 1'b1: state happened
20	RW	0x0	X24M_OSC_EN 24MHz OSC enable 1'b0: state not happened 1'b1: state happened
19	RW	0x0	RELEASE_CLAMP release pd_pmu input clamp 1'b0: state not happened 1'b1: state happened
18	RW	0x0	EXT_PWRUP ext pmic power up 1'b0: state not happened 1'b1: state happened
17	RW	0x0	WAKEUP_RESET wakeup reset 1'b0: state not happened 1'b1: state happened
16	RW	0x0	WAIT_WAKEUP wati wakeup state 1'b0: state not happened 1'b1: state happened
15	RW	0x0	X24M_OSC_DIS 24MHz soc diable state 1'b0: state not happened 1'b1: state happened
14	RW	0x0	POWEROFF chip power off state 1'b0: state not happened 1'b1: state happened
13	RW	0x0	INPUT_CLAMP pd_pmu input clamp 1'b0: state not happened 1'b1: state happened

Bit	Attr	Reset Value	Description
12	RW	0x0	PLL_PWRDN pll power down state 1'b0: state not happened 1'b1: state happened
11	RW	0x0	ALIVE_PMU_LF pd_alive&pd_pmu switch to 32khz 1'b0: state not happened 1'b1: state happened
10	RW	0x0	L2MEM_PWRDN l2 mem power down state 1'b0: state not happened 1'b1: state happened
9	RW	0x0	A17_0_PWRDN A17 core0 power down state 1'b0: state not happened 1'b1: state happened
8	RW	0x0	BUS_PWRDN pd_bus power down state 1'b0: A17_0 power on 1'b1: A17_0 power off
7	RW	0x0	DDR_IO_PWROFF ddr io power off 1'b0: state not happened 1'b1: state happened
6	RW	0x0	DDR_IO_RET DDR io retention 1'b0: state not happened 1'b1: state happened
5	RW	0x0	SREF_ENTER ddr selfrefresh enter 1'b0: state not happened 1'b1: state happened
4	RW	0x0	TRANS_NO_FIN transfer no finish 1'b0: state not happened 1'b1: state happened
3	RW	0x0	A17_CLK_DIS A17 clock disable 1'b0: state not happened 1'b1: state happened
2	RW	0x0	STANDBYL2 L2 Standby 1'b0: state not happened 1'b1: state happened

Bit	Attr	Reset Value	Description
1	RW	0x0	L2FLUSH_REQ L2 Flush req 1'b0: state not happened 1'b1: state happened
0	RW	0x0	NORMAL normal state 1'b0: state not happened 1'b1: state happened

PMU_OSC_CNT

Address: Operational Base + offset (0x0020)
24MHz OSC stabilization counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	osc_stabl_cnt_thresh 24MHz OSC stabilization counter threshold

PMU_PLL_CNT

Address: Operational Base + offset (0x0024)
PLL lock counter threshold

Bit	Attr	Reset Value	Description
31:20	RW	0x100	pllrst_cnt_thresh PLL reset wait counter threshold
19:0	RW	0x04000	plllock_cnt_thresh PLL lock wait counter threshold

PMU_STABL_CNT

Address: Operational Base + offset (0x0028)
External PMU stabilization counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_stabl_cnt_thresh External PMU stabilization counter threshold

PMU_DDR0IO_PWRON_CNT

Address: Operational Base + offset (0x002c)
DDR0 IO power on counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	ddr0io_pwrn_cnt_thresh DDR0 IO power on counter threshold

PMU_DDR1IO_PWRON_CNT

Address: Operational Base + offset (0x0030)
DDR1 IO power on counter threshold

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:0	RW	0x05dc0	ddr1io_pwrn_cnt_thresh DDR1 IO power on counter threshold

PMU_CORE_PWRDWN_CNT

Address: Operational Base + offset (0x0034)

CORE domain power down waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	core_pwrn_cnt_thresh CORE domain power down waiting counter threshold

PMU_CORE_PWRUP_CNT

Address: Operational Base + offset (0x0038)

CORE domain power up waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	core_pwrup_cnt_thresh CORE domain power up waiting counter threshold

PMU_GPU_PWRDWN_CNT

Address: Operational Base + offset (0x003c)

GPU domain power down waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	gpu_pwrn_cnt_thresh GPU domain power down waiting counter threshold

PMU_GPU_PWRUP_CNT

Address: Operational Base + offset (0x0040)

GPU domain power up waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	gpu_pwrup_cnt_thresh GPU domain power up waiting counter threshold

PMU_WAKEUP_RST_CLR_CNT

Address: Operational Base + offset (0x0044)

Wakeup reset deassert state wait counter in power off mode

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	wakeup_rst_clr_cnt_thresh Power off mode wakeup reset clear counter threshold

PMU_SFT_CON

Address: Operational Base + offset (0x0048)

PMU Software control in normal mode

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	l2flush_cfg l2 flush config in normal mode 1'b1: l2 flush req 1'b0: l2 flush disable
14	RW	0x0	osc_disable_cfg software config OSC disable 1'b1: OSC disable 1'b0: OSC enable
13	RW	0x0	osc_bypass osc bypass control 1'b0: disable 1'b1: enable
12	RW	0x0	alive_lf_ena_cfg software config ALIVE domain clock switch to 32.768kHz 1'b1: switch to 32.768kHz 1'b0: not switch
11	RW	0x0	pmu_lf_ena_cfg software config PMU domain clock switch to 32.768kHz 1'b1: switch to 32.768kHz 1'b0: not switch
10	RW	0x0	power_off_ddr1io_cfg software config power off DDR1 IO 1'b1: power off 1'b0: not power off
9	RW	0x0	ddr1_io_ret_cfg software config DDR1 IO retention 1'b1: retention 1'b0: not retention
8	RW	0x0	upctl1_c_sysreq_cfg software config enter DDR1 self-refresh by lowpower interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh
7	RW	0x0	power_off_ddr0io_cfg software config power off DDR0 IO 1'b1: power off 1'b0: not power off
6	RW	0x0	ddr0_io_ret_cfg software config DDR0 IO retention 1'b1: retention 1'b0: not retention

Bit	Attr	Reset Value	Description
5	RW	0x0	upctl0_c_sysreq_cfg software config enter DDR0 self-refresh by lowpower interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh
4	RW	0x0	clk_core_src_gating_cfg software config A17 core clock source gating 1'b1: gating 1'b0: not gating
3	RW	0x0	dbgnopwrdsn3_enable ARM CORE3 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
2	RW	0x0	dbgnopwrdsn2_enable ARM CORE2 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
1	RW	0x0	dbgnopwrdsn1_enable ARM CORE1 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support
0	RW	0x0	dbgnopwrdsn0_enable ARM CORE0 DBGNOPWRDWN function support enable 1'b0: not support 1'b1: support

PMU_DDR_SREF_ST

Address: Operational Base + offset (0x004c)

PMU DDR self refresh status

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	upctl0_c_sysack DDR0 enter self-refresh acknowledge 1'b0: no ack 1'b1: ack
2	RW	0x0	upctl0_c_active DDR0 enter self-refresh 1'b0: no active 1'b1: active

Bit	Attr	Reset Value	Description
1	RW	0x0	upctl1_c_sysack DDR1 enter self-refresh acknowledge 1'b0: no ack 1'b1: ack
0	RW	0x0	upctl1_c_active DDR1 enter self-refresh 1'b0: no active 1'b1: active

PMU_INT_CON

Address: Operational Base + offset (0x0050)

PMU interrupt configuration register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	pd_mem_int_en Power domain L2 MEM power switch interrupt enable 1'b0: disable 1'b1: enable
26	RW	0x0	pd_hevc_int_en Power domain hevc power switch interrupt enable 1'b0: disable 1'b1: enable
25	RW	0x0	pd_gpu_int_en Power domain GPU power switch interrupt enable 1'b0: disable 1'b1: enable
24	RW	0x0	pd_video_int_en Power domain VIDEO power switch interrupt enable 1'b0: disable 1'b1: enable
23	RW	0x0	pd_vio_int_en Power domain VIO power switch interrupt enable 1'b0: disable 1'b1: enable
22	RW	0x0	pd_peri_int_en Power domain PERI power switch interrupt enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
21	RW	0x0	pd_bus_int_en Power domain BUS power switch interrupt enable 1'b0: disable 1'b1: enable
20	RO	0x0	reserved
19	RW	0x0	pd_a2_3_int_en Power domain A17 slave core 3 power switch interrupt enable 1'b0: disable 1'b1: enable
18	RW	0x0	pd_A17_2_int_en Power domain A17 slave core 2 power switch interrupt enable 1'b0: disable 1'b1: enable
17	RW	0x0	pd_A17_1_int_en Power domain A17 slave core 1 power switch interrupt enable 1'b0: disable 1'b1: enable
16	RW	0x0	pd_A17_0_int_en Power domain A17 primary core power switch interrupt enable 1'b0: disable 1'b1: enable
15:6	RO	0x0	reserved
5	RW	0x0	pwrmode_wakeup_int_en wakeup interrupt enable in power mode 1'b0: disable 1'b1: enable
4	RW	0x0	gpioint_wakeup_int_en gpio interrupt wakeup interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	sdmmc0_wakeup_int_en SDMMC0 wakeup status interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	gpio_wakeup_int_en GPIO0 wakeup status interrupt enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
1	RW	0x0	armint_wakeup_int_en ARM interrupt wakeup status interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	pmu_int_en PMU interrupt enable 1'b0: disable 1'b1: enable

PMU_INT_ST

Address: Operational Base + offset (0x0054)

PMU interrupt status register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	pd_mem_int_st Power domain I2 mem power switch status 1'b0: no power switch happen 1'b1: power switch happen
26	RW	0x0	pd_hevc_int_st Power domain HEVC power switch status 1'b0: no power switch happen 1'b1: power switch happen
25	W1C	0x0	pd_gpu_int_st Power domain GPU power switch status 1'b0: no power switch happen 1'b1: power switch happen
24	W1C	0x0	pd_video_int_st Power domain VIDEO power switch status 1'b0: no power switch happen 1'b1: power switch happen
23	W1C	0x0	pd_vio_int_st Power domain VIO power switch status 1'b0: no power switch happen 1'b1: power switch happen
22	W1C	0x0	pd_peri_int_st Power domain PERI power switch status 1'b0: no power switch happen 1'b1: power switch happen
21	W1C	0x0	pd_bus_int_st Power domain BUS power switch status 1'b0: no power switch happen 1'b1: power switch happen
20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RW	0x0	pd_A17_3_int_st Power domain A17 slave core 3 power switch status 1'b0: no power switch happen 1'b1: power switch happen
18	RW	0x0	pd_A17_2_int_st Power domain A17 slave core 2 power switch status 1'b0: no power switch happen 1'b1: power switch happen
17	RW	0x0	pd_A17_1_int_st Power domain A17 slave core 1 power switch status 1'b0: no power switch happen 1'b1: power switch happen
16	RW	0x0	pd_A17_0_int_st Power domain A17 primary core power switch status 1'b0: no power switch happen 1'b1: power switch happen
15:5	RO	0x0	reserved
4	RW	0x0	pwrmode_wakeup_event_trig power mode flow wakeup 1'b0: no wakeup 1'b1: wakeup
3	RW	0x0	gpoint_wakeup_event_trig ARM interrupt wake-up event trigger 1'b0: no wakeup 1'b1: wakeup
2	W1C	0x0	sdmmc0_wakeup_event_trig SDMMC0 wake-up event trigger 1'b0: no wakeup 1'b1: wakeup
1	W1C	0x0	gpio_wakeup_event_trig GPIO0 wake-up event trigger 1'b0: no wakeup 1'b1: wakeup
0	RW	0x0	armint_wakeup_event_trig ARM interrupt wake-up event trigger 1'b0: no wakeup 1'b1: wakeup

PMU_BOOT_ADDR_SEL

Address: Operational Base + offset (0x0058)

boot_addr_sel in power mode

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	boot_addr_sel boot addr sel when wakeup from power mode

PMU_GRF_CON

Address: Operational Base + offset (0x005c)

grf control register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:10	RW	0x00	GRF_NPOR_CRNT_CTRL Npor signal crnt control register
9:4	RW	0x00	GRF_TEST_CRNT_CTRL Test signal crnt control register
3:2	RW	0x2	GRF_X32K_CRNT_CTRL X32K signal crnt control register
1:0	RW	0x0	GRF_X24M_CRNT_CTRL X24M signal crnt control register

PMU_GPIO_SR

Address: Operational Base + offset (0x0060)

GPIO slew rate control

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0_c2_sr gpio0_c2 slew rate control 1'b0: slow (half frequency) 1'b1: fast
17	RW	0x1	gpio0_c1_sr gpio0_c1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
16	RW	0x0	gpio0_c0_sr gpio0_c0 slew rate control 1'b0: slow (half frequency) 1'b1: fast
15	RW	0x0	gpio0_b7_sr gpio0_b7 slew rate control 1'b0: slow (half frequency) 1'b1: fast
14	RW	0x0	gpio0_b6_sr gpio0_b6 slew rate control 1'b0: slow (half frequency) 1'b1: fast
13	RW	0x0	gpio0_b5_sr gpio0_b5 slew rate control 1'b0: slow (half frequency) 1'b1: fast

Bit	Attr	Reset Value	Description
12	RW	0x0	gpio0_b4_sr gpio0_b4 slew rate control 1'b0: slow (half frequency) 1'b1: fast
11	RW	0x0	gpio0_b3_sr gpio0_b3 slew rate control 1'b0: slow (half frequency) 1'b1: fast
10	RW	0x0	gpio0_b2_sr gpio0_b2 slew rate control 1'b0: slow (half frequency) 1'b1: fast
9	RW	0x0	gpio0_b1_sr gpio0_b1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
8	RW	0x0	gpio0_b0_sr gpio0_b0 slew rate control 1'b0: slow (half frequency) 1'b1: fast
7	RW	0x0	gpio0_a7_sr gpio0_a7 slew rate control 1'b0: slow (half frequency) 1'b1: fastll
6	RW	0x0	gpio0_a6_sr gpio0_a6 slew rate control 1'b0: slow (half frequency) 1'b1: fast
5	RW	0x0	gpio0_a5_sr gpio0_a5 slew rate control 1'b0: slow (half frequency) 1'b1: fast
4	RW	0x0	gpio0_a4_sr gpio0_a4 slew rate control 1'b0: slow (half frequency) 1'b1: fast
3	RW	0x0	gpio0_a3_sr gpio0_a3 slew rate control 1'b0: slow (half frequency) 1'b1: fast
2	RW	0x0	gpio0_a2_sr gpio0_a2 slew rate control 1'b0: slow (half frequency) 1'b1: fast

Bit	Attr	Reset Value	Description
1	RW	0x0	gpio0_a1_sr gpio0_a1 slew rate control 1'b0: slow (half frequency) 1'b1: fast
0	RW	0x0	gpio0_a0_sr gpio0_a0 slew rate control 1'b0: slow (half frequency) 1'b1: fast

PMU_GPIO0_A_PULL

Address: Operational Base + offset (0x0064)

GPIO0A input to PU/PD programming section

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_a7_pull gpio0_a7 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
13:12	RW	0x1	gpio0_a6_pull gpio0_a6 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
11:10	RW	0x1	gpio0_a5_pull gpio0_a5 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
9:8	RW	0x1	gpio0_a4_pull gpio0_a4 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	gpio0_a3_pull gpio0_a3 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
5:4	RW	0x1	gpio0_a2_pull gpio0_a2 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
3:2	RW	0x2	gpio0_a1_pull gpio0_a1 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
1:0	RW	0x2	gpio0_a0_pull gpio0_a0 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_B_PULL

Address: Operational Base + offset (0x0068)

GPIO0B input to PU/PD programming section

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_b7_pull gpio0_b7 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio0_b6_pull gpio0_b6 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
11:10	RW	0x1	gpio0_b5_pull gpio0_b5 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
9:8	RW	0x1	gpio0_b4_pull gpio0_b4 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
7:6	RW	0x1	gpio0_b3_pull gpio0_b3 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
5:4	RW	0x1	gpio0_b2_pull gpio0_b2 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
3:2	RW	0x1	gpio0_b1_pull gpio0_b1 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio0_b0_pull gpio0_b0 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_C_PULL

Address: Operational Base + offset (0x006c)
GPIO0C input to PU/PD programming section

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x1	gpio0_c2_pull gpio0_c2 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
3:2	RW	0x1	gpio0_c1_pull gpio0_c1 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)
1:0	RW	0x1	gpio0_c0_pull gpio0_c0 pu/pd programming section [p2:p1] 2'b00: Z(Normal operation) 2'b01: weak 1 (pull-up) 2'b10: weak 0 (pull-down) 2'b11: repeater (bus keeper)

PMU_GPIO0_A_DRV

Address: Operational Base + offset (0x0070)
GPIO0A Drive strength selector

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_a7_e gpio0_a7 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

Bit	Attr	Reset Value	Description
13:12	RW	0x1	gpio0_a6_e gpio0_a6 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
11:10	RW	0x1	gpio0_a5_e gpio0_a5 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
9:8	RW	0x1	gpio0_a4_e gpio0_a4 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
7:6	RW	0x1	gpio0_a3_e gpio0_a3 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
5:4	RW	0x1	gpio0_a2_e gpio0_a2 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
3:2	RW	0x2	gpio0_a1_e gpio0_a1 drive strength slector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

Bit	Attr	Reset Value	Description
1:0	RW	0x2	gpio0_a0_e gpio0_a0 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO0_B_DRV

Address: Operational Base + offset (0x0074)

GPIO0B Drive strength selector

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:14	RW	0x1	gpio0_b7_e gpio0_b7 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
13:12	RW	0x1	gpio0_b6_e gpio0_b6 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
11:10	RW	0x1	gpio0_b5_e gpio0_b5 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
9:8	RW	0x1	gpio0_b4_e gpio0_b4 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

Bit	Attr	Reset Value	Description
7:6	RW	0x1	gpio0_b3_e gpio0_b3 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
5:4	RW	0x1	gpio0_b2_e gpio0_b2 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
3:2	RW	0x1	gpio0_b1_e gpio0_b1 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x1	gpio0_b0_e gpio0_b0 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO0_C_DRV

Address: Operational Base + offset (0x0078)

GPIO0C Drive strength selector

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x1	gpio0_c2_e gpio0_c2 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio0_c1_e gpio0_c1 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x1	gpio0_c0_e gpio0_c0 drive strength selector [e2:e1] 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMU_GPIO_OP

Address: Operational Base + offset (0x007c)

GPIO0 output value

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	gpio0_c2_op gpio0_c2 output value
17	RW	0x0	gpio0_c1_op gpio0_c1 output value
16	RW	0x0	gpio0_c0_op gpio0_c0 output value
15	RW	0x0	gpio0_b7_op gpio0_b7 output value
14	RW	0x0	gpio0_b6_op gpio0_b6 output value
13	RW	0x0	gpio0_b5_op gpio0_b5 output value
12	RW	0x0	gpio0_b4_op gpio0_b4 output value
11	RW	0x0	gpio0_b3_op gpio0_b3 output value
10	RW	0x0	gpio0_b2_op gpio0_b2 output value
9	RW	0x0	gpio0_b1_op gpio0_b1 output value
8	RW	0x0	gpio0_b0_op gpio0_b0 output value
7	RW	0x0	gpio0_a7_op gpio0_a7 output value
6	RW	0x0	gpio0_a6_op gpio0_a6 output value

Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0_a5_op gpio0_a5 output value
4	RW	0x0	gpio0_a4_op gpio0_a4 output value
3	RW	0x0	gpio0_a3_op gpio0_a3 output value
2	RW	0x0	gpio0_a2_op gpio0_a2 output value
1	RW	0x0	gpio0_a1_op gpio0_a1 output value
0	RW	0x0	gpio0_a0_op gpio0_a0 output value

PMU_GPIO0_SEL18

Address: Operational Base + offset (0x0080)

gpio0 1.8v/3.3v sel

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x1	gpio0_c0_smt
1	RW	0x1	gpio0_b7_smt gpio0_a0 output value
0	RW	0x0	gpio0_a0_op gpio0_a0 output value 1'b0: >=2.5v 1'b1: <=1.8v

PMU_GPIO0_A_IOMUX

Address: Operational Base + offset (0x0084)

GPIO0A iomux sel

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RW	0x0	gpio0_a3 iomux 1'b0: gpioa3 1'b1: ddr1_retention
5	RO	0x0	reserved
4	RW	0x0	gpio0_a2 iomux 1'b0: gpioa2 1'b1: ddr0_retention
3	RO	0x0	reserved
2	RW	0x0	gpio0_a1 iomux 1'b0: gpioa1 1'b1: ddrio_pwroff
1	RO	0x0	reserved
0	RW	0x0	gpio0_a0 iomux 1'b0: gpioa0 1'b1: global_pwroff

PMU_GPIO0_B_IOMUX

Address: Operational Base + offset (0x0088)

GPIO0B iomux sel

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	gpio0_b7 iomux 1'b0: gpiob7 1'b1: i2c0pmu_sda
13:11	RO	0x0	reserved
10	RW	0x0	gpio0_b5 iomux 1'b0: gpiob5 1'b1: CLK_27M
9:5	RO	0x0	reserved
4	RW	0x0	gpio0_b2 iomux 1'b0: gpiob2 1'b1: tsadc_int
3:0	RO	0x0	reserved

PMU_GPIO0_C_IOMUX

Address: Operational Base + offset (0x008c)

GPIO0C iomux sel

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x0	gpio0_c1 iomux 2'b00: gpioc1 2'b01: test_clkout 2'b10: clkt1_27m 2'b11: reserved
1	RO	0x0	reserved
0	RW	0x0	gpio0_c0 iomux 1'b0: gpioc0 1'b1: i2c0pmu_scl

PMU_PWRMODE_CON1

Address: Operational Base + offset (0x0090)

PMU PowerMode CON1

Bit	Attr	Reset Value	Description
31:10	-	0x0	reserved
9	RW	0x0	clr_vio issue idle_req_vio in low power mode 1'b0: not issue 1'b1: issue
8	RW	0x0	clr_hevc issue idle_req_hevc in low power mode 1'b0: not issue 1'b1: issue

Bit	Attr	Reset Value	Description
7	RW	0x0	clr_video issue idle_req_video in low power mode 1'b0: not issue 1'b1: issue
6	RW	0x0	clr_gpu issue idle_req_gpu in low power mode 1'b0: not issue 1'b1: issue
5	RW	0x0	clr_peri issue idle_req_peri in low power mode 1'b0: not issue 1'b1: issue
4	RW	0x0	clr_dma issue idle_req_dma in low power mode 1'b0: not issue 1'b1: issue
3	RW	0x0	clr_alive issue idle_req_alive in low power mode 1'b0: not issue 1'b1: issue
2	RW	0x0	clr_cpup issue idle_req_cpup in low power mode 1'b0: not issue 1'b1: issue
1	RW	0x0	clr_core issue idle_req_core in low power mode 1'b0: not issue 1'b1: issue
0	RW	0x0	clr_bus issue idle_req_bus in low power mode 1'b0: not issue 1'b1: issue

PMU_SYS_REG0

Address: Operational Base + offset (0x0094)

PMU system register0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg0 PMU system register0

PMU_SYS_REG1

Address: Operational Base + offset (0x0098)

PMU system register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg1 PMU system register1

PMU_SYS_REG2

Address: Operational Base + offset (0x009c)

PMU system register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg2 PMU system register2

PMU_SYS_REG3

Address: Operational Base + offset (0x00a0)

PMU system register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg3 PMU system register3

4.6 Timing Diagram

4.6.1 Each domain power switch timing

The following figure is the each domain power down and power up timing.

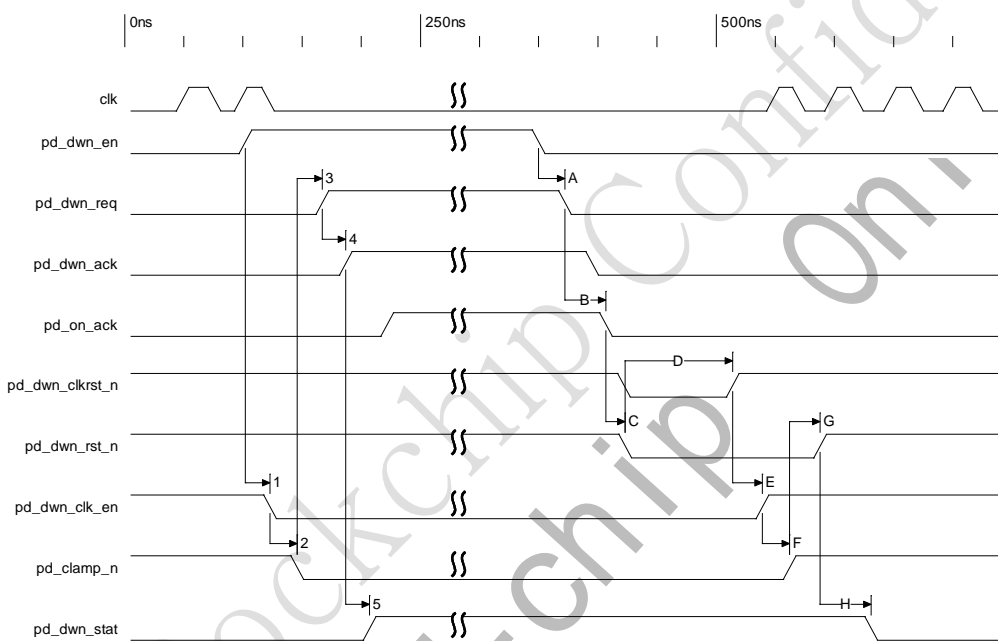


Fig. 4-3 Each Domain Power Switch Timing

4.6.2 External wakeup PAD timing

The PMU supports a lot of external wakeup sources, such as SD/MMDC, USBDEV, SIM0/1 detect wakeup, GPIO0 wakeup source and so on. All these external wakeup sources must meet the timing requirement (at least 200us) when the wakeup event is asserted. The following figure gives the timing information.

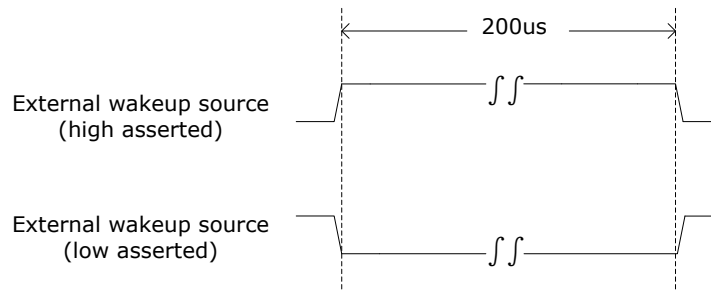


Fig. 4-4 External Wakeup Source PAD Timing

4.7 Application Notes

4.7.1 Recommend configurations for power mode.

The PMU is a design with great flexibilities, but just for facilities and inheritances, a group of recommend configurations will be shown below for software. And for convenience, we will define several modes.

The RK3288 can support following 5 recommended power modes:

- normal
- idle mode
- deep idle mode
- sleep mode
- power off mode

The following table lists the detailed description of the modes.

Table 4-5 Power Domain Status Summary in all Work Mode

Power Domain		Power Mode				
		Mode0(normal)	Mode1(idle)	Mode2(didle)	Mode3(sleep)	Mode4(poweroff)
VD_CORE	PD_A17_0	Running	Standby	Power off	Power off	Power off
	PD_A17_1	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_A17_2	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_A17_3	Running/Standby/Power off	Running/Standby/Power off	Power off	Power off	Power off
	PD_SCU	Running	Running	Running	Power off	Power off
	PD_CS	Power on	Power off	Running	Power off	Power off
	PD_MEM	Running	Running	Running	Power off	Power off
	PD_BUS	Power on	Power on	Running	Power off	Power off
	PD_PERI	Power on	Power on/off	Power on/off	Power off	Power off
	PD_VIO	Power on	Power on/off	Power on/off	Power off	Power off
PD_VIDEO	Power on	Power on/off	Power on/off	Power off	Power off	
PD_HEVC	Power on	Power on/off	Power on/off	Power off	Power off	
PD_GPU	Power on	Power on/off	Power on/off	Power off	Power off	
PD_ALIVE	Power on	Power on	Power on	Power on. Clocked by 24MHz or 32KHz	Power off	
PD_PMU	Power on	Power on	Power on	Power on. Clocked by 24MHz or 32KHz	Power on. Clocked by 32KHz	
PLL	All PLLs on	All PLLs on	All PLLs on	ALL PLLs off	ALL PLLs off	
OSC_24MHz	OSC enable	OSC enable	OSC enable	OSC enable/disable	OSC disable	
DDR	Running	Running	Self refresh	Self refresh	Self refresh	
Wakeup Sources	Software control to wake up all the module in power off or clock off states	1. all arm interrupts (include EVENTI input) 2. sdmmc0 detect_n 3. gpio int(not gpio0) 4. gpio0 io	1. all arm interrupts (include EVENTI input) 2. sdmmc0 detect_n 3. gpio int(not gpio0) 4. gpio0 io	1. sdmmc0 detect_n 2. gpio io int(not gpio0) 3. gpio0 io		GPI00 IO

Normal mode

In this mode, you can power off/on or enable/disable the following power domain to save power: PD_PERI/PD_VIO/PD_VIDEO/PD_HEVC/PD_GPU

Idle mode

This mode is used when the core do not have load for a shot while such as waiting for interrupt and the software want to save power by gating Cortex-A17 source clock.

In idle mode, core1/2/3 of Cortex-A17 should be either power off or in WFI/WFE state. The

core0 of A17 should be in WFI/WFE state. The configurations of core clock source gating and disable global interrupt are presented. The Cortex-A17 can waked up by an interrupt.

Deep idle mode

Deep idle mode is used in the scenario of audio player. In deep idle mode, powering off Cortex-A17 cores or VD_CORE voltage domain is operational, and others are same as normal mode.

In deep idle mode, you can set ddr enter the self-refresh, and power off DDRIO and enable DDR retention function in this mode, but it will takes a longer time for the recovery of DDR IO.

Sleep mode

The sleep mode can power off all power domains except PD_ALIVE. The VD_CORE is turned off externally, PD_BUS power off by hardware, and other domains power off by software.

In sleep mode the clock of PD_ALIVE can be switched from 24MHz to 32.768kHz optionally by hardware.

In sleep mode all PLLs power down mandatorily to save power by hardware.

In sleep mode OSC can be disabled optionally by hardware.

In sleep mode DDR self-refresh can be issued by hardware mandatorily.

In sleep mode DDR IO can power off and enter retention optionally by hardware.

Power off mode

The power off mode turns off the power of all VD_LOGIC externally.

In power off mode all PLLs power down mandatorily to save power by hardware.

In power off mode OSC disable request should be send by hardware.

In power off mode DDR self-refresh should be issued mandatorily by hardware.

In power off mode DDR IO can power off and enter retention optionally by hardware.

4.7.2 System Register

PMU support 4 words register: PMU_SYS_REG0, PMU_SYS_REG1, PMU_SYS_REG2, PMU_SYS_REG3. These registers are always on no matter what low power mode. So software can use these registers to retain some information which is useful after wakeup from any mode.

4.7.3 Configuration Constraint

In order to shut down the power domains correctly, the software must obey the rules bellow:

- Send NIU request to the NIU in power domain that you want to shut down.
- Querying PMU_NOC_ST register to get the information until the pacific NIU is in idle state.
- Send power request to the power domain through PMU_PWRDN_CON register.
- Querying PMU_PWRDN_ST register to make sure the pacific power domain is power down.

The power domains controlled only by software are showing below:

PD_VIO, PD_PERI, PD_GPU, PD_VIDEO, PD_HEVC, and PD_A17_1 and PD_A17_2 to PD_A17_3.

So you must power off these power domains before enter low power mode if you need.

4.7.4 Poweroff Request Combine

There is only two poweroff request, one is for VD_CORE and VD_LOGIC (power_off_req),

another is for DDRIO (power_off_ddrio).

POWER_OFF_REQ

In normal mode, If you set the chip power down (bit[13] of PMU_PWRDN_CON), or set core power down (bit[12] of PMU_PWRDN_CON), the power_off_req will be set to 1 immediate.

In Low Power mode, if you set the chip power down (bit[8] of PMU_PWRMODE_CON) or set core power down (bit[6] of PMU_PWRMODE_CON), the power_off_req will be set to 1 at the sub-step POWEROFF.

POWER_OFF_DDRIO

In normal mode, If you set the power_off_ddr0io_cfg (bit[7] of PMU_SFT_CON), or set power_off_ddr1io_cfg (bit[10] of PMU_SFT_CON), the power_off_ddrio will be set to 1 immediate.

In Low Power mode, if you set the ddr0io_ret_en (bit[17] of PMU_PWRMODE_CON) or set ddr1io_ret_en (bit[18] of PMU_PWRMODE_CON), the power_off_ddrio will be set to 1 at the sub-step DDR_IO_POWEROFF.

In Low Power mode, if you set pwroff_comb (bit[9] of PMU_PWRMODE_CON) at same time, the power_off_ddrio would not be set to 1, and the power_off_req would be set to 1 at the sub-step DDR_IO_POWEROFF.

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