Chapter 7 General Register Files (GRF)

7.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control. The GRF is divided into two sections, one is GRF for non-secure system, the other is SGRF for secure system.

7.2 Function Description

The function of general register file is：

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

7.3 GRF Register Description

7.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO1D_IOMUX	0x000c	W	0x00000000	GPIO1D iomux control
GRF_GPIO2A_IOMUX	0x0010	W	0x00000000	GPIO2A iomux control
GRF_GPIO2B_IOMUX	0x0014	W	0x00000000	GPIO2B iomux control
GRF_GPIO2C_IOMUX	0x0018	W	0x00000000	GPIO2C iomux control
GRF_GPIO3A_IOMUX	0x0020	W	0x00000000	GPIO3A iomux control
GRF_GPIO3B_IOMUX	0x0024	W	0x00000000	GPIO3B iomux control
GRF_GPIO3C_IOMUX	0x0028	W	0x00000000	GPIO3C iomux control
GRF_GPIO3DL_IOMUX	0x002c	W	0x00000000	GPIO3D iomux control
GRF_GPIO3DH_IOMUX	0x0030	W	0x00000000	GPIO3D iomux control
GRF_GPIO4AL_IOMUX	0x0034	W	0x00000000	GPIO4A iomux control
GRF_GPIO4AH_IOMUX	0x0038	W	0x00000000	GPIO4A iomux control
GRF_GPIO4BL_IOMUX	0x003c	W	0x00000000	GPIO4B iomux control
GRF_GPIO4C_IOMUX	0x0044	W	0x00000000	GPIO4C iomux control
GRF_GPIO4D_IOMUX	0x0048	W	0x00000000	GPIO4D iomux control
GRF_GPIO5B_IOMUX	0x0050	W	0x00000000	GPIO5B iomux control
GRF_GPIO5C_IOMUX	0x0054	W	0x00000000	GPIO5C iomux control
GRF_GPIO6A_IOMUX	0x005c	W	0x00000000	GPIO6A iomux control
GRF_GPIO6B_IOMUX	0x0060	W	0x00000000	GPIO6B iomux control
GRF_GPIO6C_IOMUX	0x0064	W	0x00001555	GPIO6C iomux control
GRF_GPIO7A_IOMUX	0x006c	W	0x00000000	GPIO7A iomux control
GRF_GPIO7B_IOMUX	0x0070	W	0x00000000	GPIO7B iomux control
GRF_GPIO7CL_IOMUX	0x0074	W	0x00000000	GPIO7CL iomux control
GRF_GPIO7CH_IOMUX	0x0078	W	0x00000000	GPIO7CH iomux control

Name	Offset	Size	Reset Value	Description
GRF_GPIO8A_IOMUX	0x0080	W	0x00000000	GPIO8A iomux control
GRF_GPIO8B_IOMUX	0x0084	W	0x00000000	GPIO8B iomux control
GRF_GPIO1H_SR	0x0104	W	0x00000f00	GPIO1C/D SR control
GRF_GPIO2L_SR	0x0108	W	0x00000000	GPIO2A/B SR control
GRF_GPIO2H_SR	0x010c	W	0x00000000	GPIO2C/D SR control
GRF_GPIO3L_SR	0x0110	W	0x000020ff	GPIO3A/B SR control
GRF_GPIO3H_SR	0x0114	W	0x0000ff04	GPIO3C/D SR control
GRF_GPIO4L_SR	0x0118	W	0x00000120	GPIO4A/B SR control
GRF_GPIO4H_SR	0x011c	W	0x00000000	GPIO4C/D SR control
GRF_GPIO5L_SR	0x0120	W	0x00000000	GPIO5A/B SR control
GRF_GPIO5H_SR	0x0124	W	0x00000000	GPIO5C/D SR control
GRF_GPIO6L_SR	0x0128	W	0x00000100	GPIO6A/B SR control
GRF_GPIO6H_SR	0x012c	W	0x00000010	GPIO6C/D SR control
GRF_GPIO7L_SR	0x0130	W	0x00000000	GPIO7A/B SR control
GRF_GPIO7H_SR	0x0134	W	0x00000000	GPIO7C/D SR control
GRF_GPIO8L_SR	0x0138	W	0x00000000	GPIO8A/B SR control
GRF_GPIO1D_P	0x014c	W	0x0000aaaa	GPIO1D PU/PD control
GRF_GPIO2A_P	0x0150	W	0x0000aaaa	GPIO2A PU/PD control
GRF_GPIO2B_P	0x0154	W	0x0000aaaa	GPIO2B PU/PD control
GRF_GPIO2C_P	0x0158	W	0x0000aaa5	GPIO2C PU/PD control
GRF_GPIO3A_P	0x0160	W	0x00005555	GPIO3A PU/PD control
GRF_GPIO3B_P	0x0164	W	0x00005699	GPIO3B PU/PD control
GRF_GPIO3C_P	0x0168	W	0x0000aaa5	GPIO3C PU/PD control
GRF_GPIO3D_P	0x016c	W	0x00005555	GPIO3D PU/PD control
GRF_GPIO4A_P	0x0170	W	0x00005555	GPIO4A PU/PD control
GRF_GPIO4B_P	0x0174	W	0x0000aaa5	GPIO4B PU/PD control
GRF_GPIO4C_P	0x0178	W	0x00005559	GPIO4C PU/PD control
GRF_GPIO4D_P	0x017c	W	0x00005a99	GPIO4D PU/PD control
GRF_GPIO5B_P	0x0184	W	0x00006559	GPIO5B PU/PD control
GRF_GPIO5C_P	0x0188	W	0x0000aaa9	GPIO5C PU/PD control
GRF_GPIO6A_P	0x0190	W	0x0000aaaa	GPIO6A PU/PD control
GRF_GPIO6B_P	0x0194	W	0x0000aa96	GPIO6B PU/PD control
GRF_GPIO6C_P	0x0198	W	0x00005655	GPIO6C PU/PD control
GRF_GPIO7A_P	0x01a0	W	0x000059aa	GPIO7A PU/PD control
GRF_GPIO7B_P	0x01a4	W	0x0000a696	GPIO7B PU/PD control
GRF_GPIO7C_P	0x01a8	W	0x00005955	GPIO7C PU/PD control
GRF_GPIO8A_P	0x01b0	W	0x00006555	GPIO8A PU/PD control
GRF_GPIO8B_P	0x01b4	W	0x0000aaaa	GPIO8B PU/PD control
GRF_GPIO1D_E	0x01cc	W	0x000055aa	GPIO1D drive strength control
GRF_GPIO2A_E	0x01d0	W	0x0000aaaa	GPIO2A drive strength control
GRF_GPIO2B_E	0x01d4	W	0x0000aaaa	GPIO2B drive strength control
GRF_GPIO2C_E	0x01d8	W	0x00005555	GPIO2C drive strength control
GRF_GPIO3A_E	0x01e0	W	0x0000aaaa	GPIO3A drive strength control

Name	Offset	Size	Reset Value	Description
GRF_GPIO3B_E	0x01e4	W	0x00005955	GPIO3B drive strength control
GRF_GPIO3C_E	0x01e8	W	0x00005565	GPIO3C drive strength control
GRF_GPIO3D_E	0x01ec	W	0x0000aaaa	GPIO3D drive strength control
GRF_GPIO4A_E	0x01f0	W	0x00005955	GPIO4A drive strength control
GRF_GPIO4B_E	0x01f4	W	0x00005556	GPIO4B drive strength control
GRF_GPIO4C_E	0x01f8	W	0x00005555	GPIO4C drive strength control
GRF_GPIO4D_E	0x01fc	W	0x00005555	GPIO4D drive strength control
GRF_GPIO5B_E	0x0204	W	0x00005555	GPIO5B drive strength control
GRF_GPIO5C_E	0x0208	W	0x00005555	GPIO5C drive strength control
GRF_GPIO6A_E	0x0210	W	0x00005555	GPIO6A drive strength control
GRF_GPIO6B_E	0x0214	W	0x00005555	GPIO6B drive strength control
GRF_GPIO6C_E	0x0218	W	0x00005555	GPIO6C drive strength control
GRF_GPIO7A_E	0x0220	W	0x00005555	GPIO7A drive strength control
GRF_GPIO7B_E	0x0224	W	0x00005555	GPIO7B drive strength control
GRF_GPIO7C_E	0x0228	W	0x00005555	GPIO7C drive strength control
GRF_GPIO8A_E	0x0230	W	0x00005555	GPIO8A drive strength control
GRF_GPIO8B_E	0x0234	W	0x00005555	GPIO8B drive strength control
GRF_GPIO_SMT	0x0240	W	0x00000fff	GPIO smitter control register
GRF_SOC_CON0	0x0244	W	0x00001c18	SoC control register 0
GRF_SOC_CON1	0x0248	W	0x00004040	SoC control register 1
GRF_SOC_CON2	0x024c	W	0x00000002	SoC control register 2
GRF_SOC_CON3	0x0250	W	0x00000810	SoC control register 3
GRF_SOC_CON4	0x0254	W	0x00000607	SoC control register 4
GRF_SOC_CON5	0x0258	W	0x00008c87	SoC control register 5
GRF_SOC_CON6	0x025c	W	0x00008000	SoC control register 6
GRF_SOC_CON7	0x0260	W	0x00000000	SoC control register 7
GRF_SOC_CON8	0x0264	W	0x0000000e	SoC control register 8
GRF_SOC_CON9	0x0268	W	0x0000000e	SoC control register 9
GRF_SOC_CON10	0x026c	W	0x0000000f	SoC control register 10
GRF_SOC_CON11	0x0270	W	0x00000000	SoC control register 11
GRF_SOC_CON12	0x0274	W	0x00000013	SoC control register 12
GRF_SOC_CON13	0x0278	W	0x00000000	SoC control register 13
GRF_SOC_CON14	0x027c	W	0x00000000	SoC control register 14
GRF_SOC_STATUS0	0x0280	W	0x00000000	SoC status register 0
GRF_SOC_STATUS1	0x0284	W	0x00000000	SoC status register 1
GRF_SOC_STATUS2	0x0288	W	0x00000000	SoC status register 2
GRF_SOC_STATUS3	0x028c	W	0x00000000	SoC status register 3
GRF_SOC_STATUS4	0x0290	W	0x00000000	SoC status register 4
GRF_SOC_STATUS5	0x0294	W	0x00000000	SoC status register 5
GRF_SOC_STATUS6	0x0298	W	0x00000000	SoC status register 6
GRF_SOC_STATUS7	0x029c	W	0x00000000	SoC status register 7
GRF_SOC_STATUS8	0x02a0	W	0x00000000	SoC status register 8
GRF_SOC_STATUS9	0x02a4	W	0x00000000	SoC status register 9

Name	Offset	Size	Reset Value	Description
GRF_SOC_STATUS10	0x02a8	W	0x00000000	SoC status register 10
GRF_SOC_STATUS11	0x02ac	W	0x00000000	SoC status register 11
GRF_SOC_STATUS12	0x02b0	W	0x00000000	SoC status register 12
GRF_SOC_STATUS13	0x02b4	W	0x00000000	SoC status register 13
GRF_SOC_STATUS14	0x02b8	W	0x00000000	SoC status register 14
GRF_SOC_STATUS15	0x02bc	W	0x00000000	SoC status register 15
GRF_SOC_STATUS16	0x02c0	W	0x00000000	SoC status register 16
GRF_SOC_STATUS17	0x02c4	W	0x00000000	SoC status register 17
GRF_SOC_STATUS18	0x02c8	W	0x00000000	SoC status register 18
GRF_SOC_STATUS19	0x02cc	W	0x00000000	SoC status register 19
GRF_SOC_STATUS20	0x02d0	W	0x00000000	SoC status register 20
GRF_SOC_STATUS21	0x02d4	W	0x00000000	SoC status register 21
GRF_PERIDMAC_CON0	0x02e0	W	0x000000fa	PERI DMAC control register 0
GRF_PERIDMAC_CON1	0x02e4	W	0x00000000	PERI DMAC control register 1
GRF_PERIDMAC_CON2	0x02e8	W	0x0000ffff	PERI DMAC control register 2
GRF_PERIDMAC_CON3	0x02ec	W	0x0000ffff	PERI DMAC control register 3
GRF_DDRC0_CON0	0x02f0	W	0x00000000	DDRC0 control register 0
GRF_DDRC1_CON0	0x02f4	W	0x00000000	DDRC1 control register 0
GRF_CPU_CON0	0x02f8	W	0x00008220	CPU control register 0
GRF_CPU_CON1	0x02fc	W	0x00000ff0	CPU control register 1
GRF_CPU_CON2	0x0300	W	0x00000fff	CPU control register 2
GRF_CPU_CON3	0x0304	W	0x00000000	CPU control register 3
GRF_CPU_CON4	0x0308	W	0x00002400	CPU control register 4
GRF_CPU_STATUS0	0x0318	W	0x00000000	CPU status register 0
GRF_UOC0_CON0	0x0320	W	0x00000089	UOC0 control register 0
GRF_UOC0_CON1	0x0324	W	0x00007333	UOC0 control register 1
GRF_UOC0_CON2	0x0328	W	0x00000d08	UOC0 control register 2
GRF_UOC0_CON3	0x032c	W	0x00000001	UOC0 control register 3
GRF_UOC0_CON4	0x0330	W	0x00000003	UOC0 control register 4
GRF_UOC1_CON0	0x0334	W	0x00000b89	UOC1 control register 0
GRF_UOC1_CON1	0x0338	W	0x00007333	UOC1 control register 1
GRF_UOC1_CON2	0x033c	W	0x00000d08	UOC1 control register 2
GRF_UOC1_CON3	0x0340	W	0x00001c41	UOC1 control register 3
GRF_UOC1_CON4	0x0344	W	0x0000c820	UOC1 control register 4
GRF_UOC2_CON0	0x0348	W	0x00000089	UOC2 control register 0
GRF_UOC2_CON1	0x034c	W	0x00007333	UOC2 control register 1
GRF_UOC2_CON2	0x0350	W	0x00000d08	UOC2 control register 2
GRF_UOC2_CON3	0x0354	W	0x00001c01	UOC2 control register 3
GRF_UOC3_CON0	0x0358	W	0x000030eb	UOC3 control register 0
GRF_UOC3_CON1	0x035c	W	0x00000003	UOC3 control register 1
GRF_UOC4_CON0	0x0360	W	0x00001080	UOC4 control register 0
GRF_UOC4_CON1	0x0364	W	0x00000820	UOC4 control register 1
GRF_PVTM_CON0	0x0368	W	0x00000000	PVT monitor control register 0

Name	Offset	Size	Reset Value	Description
GRF_PVTM_CON1	0x036c	W	0x016e3600	PVT monitor control register 1
GRF_PVTM_CON2	0x0370	W	0x016e3600	PVT monitor control register 2
GRF_PVTM_STATUS0	0x0374	W	0x00000000	PVT monitor status register 0
GRF_PVTM_STATUS1	0x0378	W	0x00000000	PVT monitor status register 1
GRF_PVTM_STATUS2	0x037c	W	0x00000000	PVT monitor status register 2
GRF_IO_VSEL	0x0380	W	0x00000004	IO voltage select
GRF_SARADC_TESTBIT	0x0384	W	0x00000000	SARADC Test bit register
GRF_TSADC_TESTBIT_L	0x0388	W	0x00000000	TSADC Test bit low register
GRF_TSADC_TESTBIT_H	0x038c	W	0x00000000	TSADC Test bit high register
GRF_OS_REG0	0x0390	W	0x00000000	OS register 0
GRF_OS_REG1	0x0394	W	0x00000000	OS register 1
GRF_OS_REG2	0x0398	W	0x00000000	OS register 2
GRF_OS_REG3	0x039c	W	0x00000000	OS register 3
GRF_SOC_CON15	0x03a4	W	0x00000000	SoC control register 15
GRF_SOC_CON16	0x03a8	W	0x00000000	SoC control register 16

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

7.3.2 Detail Register Description

GRF_GPIO1D_IOMUX
Address: Operational Base + offset (0x000c)
GPIO1D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio1d3_sel GPIO1D[3] iomux select 1'b0: gpio 1'b1: lcdc0_dclk
5	RO	0x0	reserved
4	RW	0x0	gpio1d2_sel GPIO1D[2] iomux select 1'b0: gpio 1'b1: lcdc0_den
3	RO	0x0	reserved
2	RW	0x0	gpio1d1_sel GPIO1D[1] iomux select 1'b0: gpio 1'b1: lcdc0_vsync

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	gpio1d0_sel GPIO1D[0] iomux select 1'b0: gpio 1'b1: lcdc0_hsync

GRF_GPIO2A_IOMUX
Address: Operational Base + offset (0x0010)
GPIO2A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio2a7_sel GPIO2A[7] iomux select 2'b00: gpio 2'b01: cif_data9 2'b10: host_din5 2'b11: hsadc_data7
13:12	RW	0x0	gpio2a6_sel GPIO2A[6] iomux select 2'b00: gpio 2'b01: cif_data8 2'b10: host_din4 2'b11: hsadc_data6
11:10	RW	0x0	gpio2a5_sel GPIO2A[5] iomux select 2'b00: gpio 2'b01: cif_data7 2'b10: host_ckinn 2'b11: hsadc_data5
9:8	RW	0x0	gpio2a4_sel GPIO2A[4] iomux select 2'b00: gpio 2'b01: cif_data6 2'b10: host_ckinp 2'b11: hsadc_data4

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] iomux select 2'b00: gpio 2'b01: cif_data5 2'b10: host_din3 2'b11: hsadc_data3
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] iomux select 2'b00: gpio 2'b01: cif_data4 2'b10: host_din2 2'b11: hsadc_data2
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] iomux select 2'b00: gpio 2'b01: cif_data3 2'b10: host_din1 2'b11: hsadc_data1
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] iomux select 2'b00: gpio 2'b01: cif_data2 2'b10: host_din0 2'b11: hsadc_data0

GRF_GPIO2B_IOMUX
Address: Operational Base + offset (0x0014)
GPIO2B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	gpio2b7_sel GPIO2B[7] iomux select 1'b0: gpio 1'b1: cif_data11
13	RO	0x0	reserved
12	RW	0x0	gpio2b6_sel GPIO2B[6] iomux select 1'b0: gpio 1'b1: cif_data10
11	RO	0x0	reserved
10	RW	0x0	gpio2b5_sel GPIO2B[5] iomux select 1'b0: gpio 1'b1: cif_data1
9	RO	0x0	reserved
8	RW	0x0	gpio2b4_sel GPIO2B[4] iomux select 1'b0: gpio 1'b1: cif_data0
7:6	RW	0x0	gpio2b3_sel GPIO2B[3] iomux select 2'b00: gpio 2'b01: cif_clkout 2'b10: host_wkreq 2'b11: hsadcts_fail
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] iomux select 2'b00: gpio 2'b01: cif_clkin 2'b10: host_wkack 2'b11: gps_clk (when hsadc_clkout_en==0) hsadc_clkout (when hsadc_clkout_en==1)
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] iomux select 2'b00: gpio 2'b01: cif_href 2'b10: host_din7 2'b11: hsadcts_valid
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] iomux select 2'b00: gpio 2'b01: cif_vsync 2'b10: host_din6 2'b11: hsadcts_sync

GRF_GPIO2C_IOMUX
Address: Operational Base + offset (0x0018)
GPIO2C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:3	RO	0x0	reserved
2	RW	0x0	gpio2c1_sel GPIO2C[1] iomux select 1'b0: gpio 1'b1: i2c3cam_sda
1	RO	0x0	reserved
0	RW	0x0	gpio2c0_sel GPIO2C[0] iomux select 1'b0: gpio 1'b1: i2c3cam_scl

GRF_GPIO3A_IOMUX
Address: Operational Base + offset (0x0020)
GPIO3A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio3a7_sel GPIO3A[7] iomux select 2'b00: gpio 2'b01: flash0_data7 2'b10: emmc_data7 2'b11: reserved
13:12	RW	0x0	gpio3a6_sel GPIO3A[6] iomux select 2'b00: gpio 2'b01: flash0_data6 2'b10: emmc_data6 2'b11: reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio3a5_sel GPIO3A[5] iomux select 2'b00: gpio 2'b01: flash0_data5 2'b10: emmc_data5 2'b11: reserved
9:8	RW	0x0	gpio3a4_sel GPIO3A[4] iomux select 2'b00: gpio 2'b01: flash0_data4 2'b10: emmc_data4 2'b11: reserved
7:6	RW	0x0	gpio3a3_sel GPIO3A[3] iomux select 2'b00: gpio 2'b01: flash0_data3 2'b10: emmc_data3 2'b11: reserved
5:4	RW	0x0	gpio3a2_sel GPIO3A[2] iomux select 2'b00: gpio 2'b01: flash0_data2 2'b10: emmc_data2 2'b11: reserved
3:2	RW	0x0	gpio3a1_sel GPIO3A[1] iomux select 2'b00: gpio 2'b01: flash0_data1 2'b10: emmc_data1 2'b11: reserved
1:0	RW	0x0	gpio3a0_sel GPIO3A[0] iomux select 2'b00: gpio 2'b01: flash0_data0 2'b10: emmc_data0 2'b11: reserved

GRF_GPIO3B_IOMUX
Address: Operational Base + offset (0x0024)
GPIO3B iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio3b7_sel GPIO3B[7] iomux select 1'b0: gpio 1'b1: flash0_csn1
13	RO	0x0	reserved
12	RW	0x0	gpio3b6_sel GPIO3B[6] iomux select 1'b0: gpio 1'b1: flash0_csn0
11	RO	0x0	reserved
10	RW	0x0	gpio3b5_sel GPIO3B[5] iomux select 1'b0: gpio 1'b1: flash0_wrn
9	RO	0x0	reserved
8	RW	0x0	gpio3b4_sel GPIO3B[4] iomux select 1'b0: gpio 1'b1: flash0_cle
7	RO	0x0	reserved
6	RW	0x0	gpio3b3_sel GPIO3B[3] iomux select 1'b0: gpio 1'b1: flash0_ale
5	RO	0x0	reserved
4	RW	0x0	gpio3b2_sel GPIO3B[2] iomux select 1'b0: gpio 1'b1: flash0_rdn
3:2	RW	0x0	gpio3b1_sel GPIO3B[1] iomux select 2'b00: gpio 2'b01: flash0_wp 2'b10: emmc_pwren 2'b11: reserved
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio3b0_sel GPIO3B[0] iomux select 1'b0: gpio 1'b1: flash0_rdy

GRF_GPIO3C_IOMUX
Address: Operational Base + offset (0x0028)
GPIO3C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5:4	RW	0x0	gpio3c2_sel GPIO3C[2] iomux select 2'b00: gpio 2'b01: flash0_dqs 2'b10: emmc_clkout 2'b11: reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] iomux select 2'b00: gpio 2'b01: flash0_csn3 2'b10: emmc_rstnout 2'b11: reserved
1:0	RW	0x0	gpio3c0_sel GPIO3C[0] iomux select 2'b00: gpio 2'b01: flash0_csn2 2'b10: emmc_cmd 2'b11: reserved

GRF_GPIO3DL_IOMUX
Address: Operational Base + offset (0x002c)
GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d3_sel GPIO3D[3] iomux select 3'b000: gpio 3'b001: flash1_data3 3'b010: host_dout3 3'b011: mac_rxd3 3'b100: sdio1_data3 other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d2_sel GPIO3D[2] iomux select 3'b000: gpio 3'b001: flash1_data2 3'b010: host_dout2 3'b011: mac_rxd2 3'b100: sdio1_data2 other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d1_sel GPIO3D[1] iomux select 3'b000: gpio 3'b001: flash1_data1 3'b010: host_dout1 3'b011: mac_txd3 3'b100: sdio1_data1 other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d0_sel GPIO3D[0] iomux select 3'b000: gpio 3'b001: flash1_data0 3'b010: host_dout0 3'b011: mac_txd2 3'b100: sdio1_data0 other: reserved

GRF_GPIO3DH_IOMUX
Address: Operational Base + offset (0x0030)
GPIO3D iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d7_sel GPIO3D[7] iomux select 3'b000: gpio 3'b001: flash1_data7 3'b010: host_dout7 3'b011: mac_rxd1 3'b100: sdio1_intn other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d6_sel GPIO3D[6] iomux select 3'b000: gpio 3'b001: flash1_data6 3'b010: host_dout6 3'b011: mac_rxd0 3'b100: sdio1_bkpwr other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d5_sel GPIO3D[5] iomux select 3'b000: gpio 3'b001: flash1_data5 3'b010: host_dout5 3'b011: mac_txd1 3'b100: sdio1_wrprt other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d4_sel GPIO3D[4] iomux select 3'b000: gpio 3'b001: flash1_data4 3'b010: host_dout4 3'b011: mac_txd0 3'b100: sdio1_detectn other: reserved

GRF_GPIO4AL_IOMUX
Address: Operational Base + offset (0x0034)

GPIO4A iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a3_sel GPIO4A[3] iomux select 3'b001: flash1_ale 3'b010: host_dout9 3'b011: mac_clk 3'b100: flash0_csn6 other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a2_sel GPIO4A[2] iomux select 3'b000: gpio 3'b001: flash1_rdn 3'b010: host_dout8 3'b011: mac_rxer 3'b100: flash0_csn5 other: reserved
7	RO	0x0	reserved
6:4	RW	0x0	gpio4a1_sel GPIO4A[1] iomux select 3'b000: gpio 3'b001: flash1_wp 3'b010: host_ckoutn 3'b011: mac_rxdv 3'b100: flash0_csn4 other: reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	gpio4a0_sel GPIO4A[0] iomux select 2'b00: gpio 2'b01: flash1_rdy 2'b10: host_ckoutp 2'b11: mac_mdc

GRF_GPIO4AH_IOMUX

Address: Operational Base + offset (0x0038)

GPIO4A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a7_sel GPIO4A[7] iomux select 3'b000: gpio 3'b001: flash1_csn1 3'b010: host_dout13 3'b011: mac_crs 3'b100: sdio1_clkout other: reserved
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a6_sel GPIO4A[6] iomux select 3'b000: gpio 3'b001: flash1_csn0 3'b010: host_dout12 3'b011: mac_rxclk 3'b100: sdio1_cmd other: reserved
7:6	RO	0x0	reserved
5:4	RW	0x0	gpio4a5_sel GPIO4A[5] iomux select 2'b00: gpio 2'b01: flash1_wrn 2'b10: host_dout11 2'b11: mac_mdio
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a4_sel GPIO4A[4] iomux select 3'b000: gpio 3'b001: flash1_cle 3'b010: host_dout10 3'b011: mac_txen 3'b100: flash0_csn7 other: reserved

GRF_GPIO4BL_IOMUX
Address: Operational Base + offset (0x003c)
GPIO4B iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6:4	RW	0x0	gpio4b1_sel GPIO4B[1] iomux select 3'b000: gpio 3'b001: flash1_csn2 3'b010: host_dout15 3'b011: mac_txclk 3'b100: sdio1_pwren other: reserved
3	RO	0x0	reserved
2:0	RW	0x0	gpio4b0_sel GPIO4B[0] iomux select 3'b000: gpio 3'b001: flash1_dqs 3'b010: host_dout14 3'b011: mac_col 3'b100: flash1_csn3 other: reserved

GRF_GPIO4C_IOMUX
Address: Operational Base + offset (0x0044)
GPIO4C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio4c7_sel GPIO4C[7] iomux select 1'b0: gpio 1'b1: sdio0_data3
13	RO	0x0	reserved
12	RW	0x0	gpio4c6_sel GPIO4C[6] iomux select 1'b0: gpio 1'b1: sdio0_data2

Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10	RW	0x0	gpio4c5_sel GPIO4C[5] iomux select 1'b0: gpio 1'b1: sdio0_data1
9	RO	0x0	reserved
8	RW	0x0	gpio4c4_sel GPIO4C[4] iomux select 1'b0: gpio 1'b1: sdio0_data0
7	RO	0x0	reserved
6	RW	0x0	gpio4c3_sel GPIO4C[3] iomux select 1'b0: gpio 1'b1: uart0bt_rtsn
5	RO	0x0	reserved
4	RW	0x0	gpio4c2_sel GPIO4C[2] iomux select 1'b0: gpio 1'b1: uart0bt_ctsn
3	RO	0x0	reserved
2	RW	0x0	gpio4c1_sel GPIO4C[1] iomux select 1'b0: gpio 1'b1: uart0bt_sout
1	RO	0x0	reserved
0	RW	0x0	gpio4c0_sel GPIO4C[0] iomux select 1'b0: gpio 1'b1: uart0bt_sin

GRF_GPIO4D_IOMUX
Address: Operational Base + offset (0x0048)
GPIO4D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x0	gpio4d6_sel GPIO4D[6] iomux select 1'b0: gpio 1'b1: sdio0_intn
11	RO	0x0	reserved
10	RW	0x0	gpio4d5_sel GPIO4D[5] iomux select 1'b0: gpio 1'b1: sdio0_bkpwr
9	RO	0x0	reserved
8	RW	0x0	gpio4d4_sel GPIO4D[4] iomux select 1'b0: gpio 1'b1: sdio0_pwren
7	RO	0x0	reserved
6	RW	0x0	gpio4d3_sel GPIO4D[3] iomux select 1'b0: gpio 1'b1: sdio0_wrprt
5	RO	0x0	reserved
4	RW	0x0	gpio4d2_sel GPIO4D[2] iomux select 1'b0: gpio 1'b1: sdio0_detectn
3	RO	0x0	reserved
2	RW	0x0	gpio4d1_sel GPIO4D[1] iomux select 1'b0: gpio 1'b1: sdio0_clkout
1	RO	0x0	reserved
0	RW	0x0	gpio4d0_sel GPIO4D[0] iomux select 1'b0: gpio 1'b1: sdio0_cmd

GRF_GPIO5B_IOMUX
Address: Operational Base + offset (0x0050)
GPIO5B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio5b7_sel GPIO5B[7] iomux select 2'b00: gpio 2'b01: spi0_rxd 2'b10: ts0_data7 2'b11: uart4exp_sin
13:12	RW	0x0	gpio5b6_sel GPIO5B[6] iomux select 2'b00: gpio 2'b01: spi0_txd 2'b10: ts0_data6 2'b11: uart4exp_sout
11:10	RW	0x0	gpio5b5_sel GPIO5B[5] iomux select 2'b00: gpio 2'b01: spi0_csn0 2'b10: ts0_data5 2'b11: uart4exp_rtsn
9:8	RW	0x0	gpio5b4_sel GPIO5B[4] iomux select 2'b00: gpio 2'b01: spi0_clk 2'b10: ts0_data4 2'b11: uart4exp_ctsn
7:6	RW	0x0	gpio5b3_sel GPIO5B[3] iomux select 2'b00: gpio 2'b01: uart1bb_rtsn 2'b10: ts0_data3 2'b11: reserved
5:4	RW	0x0	gpio5b2_sel GPIO5B[2] iomux select 2'b00: gpio 2'b01: uart1bb_ctsn 2'b10: ts0_data2 2'b11: reserved
3:2	RW	0x0	gpio5b1_sel GPIO5B[1] iomux select 2'b00: gpio 2'b01: uart1bb_sout 2'b10: ts0_data1 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio5b0_sel GPIO5B[0] iomux select 2'b00: gpio 2'b01: uart1bb_sin 2'b10: ts0_data0 2'b11: reserved

GRF_GPIO5C_IOMUX
Address: Operational Base + offset (0x0054)
GPIO5C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio5c3_sel GPIO5C[3] iomux select 1'b0: gpio 1'b1: ts0_err
5	RO	0x0	reserved
4	RW	0x0	gpio5c2_sel GPIO5C[2] iomux select 1'b0: gpio 1'b1: ts0_clk
3	RO	0x0	reserved
2	RW	0x0	gpio5c1_sel GPIO5C[1] iomux select 1'b0: gpio 1'b1: ts0_valid
1:0	RW	0x0	gpio5c0_sel GPIO5C[0] iomux select 2'b00: gpio 2'b01: spi0_csn1 2'b10: ts0_sync 2'b11: reserved

GRF_GPIO6A_IOMUX
Address: Operational Base + offset (0x005c)
GPIO6A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio6a7_sel GPIO6A[7] iomux select 1'b0: gpio 1'b1: i2s_sdo3
13	RO	0x0	reserved
12	RW	0x0	gpio6a6_sel GPIO6A[6] iomux select 1'b0: gpio 1'b1: i2s_sdo2
11	RO	0x0	reserved
10	RW	0x0	gpio6a5_sel GPIO6A[5] iomux select 1'b0: gpio 1'b1: i2s_sdo1
9	RO	0x0	reserved
8	RW	0x0	gpio6a4_sel GPIO6A[4] iomux select 1'b0: gpio 1'b1: i2s_sdo0
7	RO	0x0	reserved
6	RW	0x0	gpio6a3_sel GPIO6A[3] iomux select 1'b0: gpio 1'b1: i2s_sdi
5	RO	0x0	reserved
4	RW	0x0	gpio6a2_sel GPIO6A[2] iomux select 1'b0: gpio 1'b1: i2s_lrcktx
3	RO	0x0	reserved
2	RW	0x0	gpio6a1_sel GPIO6A[1] iomux select 1'b0: gpio 1'b1: i2s_lrckrx
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	gpio6a0_sel GPIO6A[0] iomux select 1'b0: gpio 1'b1: i2s_sclk

GRF_GPIO6B_IOMUX
Address: Operational Base + offset (0x0060)
GPIO6B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio6b3_sel GPIO6B[3] iomux select 1'b0: gpio 1'b1: spdif_tx
5	RO	0x0	reserved
4	RW	0x0	gpio6b2_sel GPIO6B[2] iomux select 1'b0: gpio 1'b1: i2c1audio_scl
3	RO	0x0	reserved
2	RW	0x0	gpio6b1_sel GPIO6B[1] iomux select 1'b0: gpio 1'b1: i2c1audio_sda
1	RO	0x0	reserved
0	RW	0x0	gpio6b0_sel GPIO6B[0] iomux select 1'b0: gpio 1'b1: i2s_clk

GRF_GPIO6C_IOMUX
Address: Operational Base + offset (0x0064)
GPIO6C iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x1	gpio6c6_sel GPIO6C[6] iomux select 1'b0: gpio 1'b1: sdmmc0_dectn
11	RO	0x0	reserved
10	RW	0x1	gpio6c5_sel GPIO6C[5] iomux select 1'b0: gpio 1'b1: sdmmc0_cmd
9:8	RW	0x1	gpio6c4_sel GPIO6C[4] iomux select 2'b00: gpio 2'b01: sdmmc0_clkout 2'b10: jtag_tdo 2'b11: reserved
7:6	RW	0x1	gpio6c3_sel GPIO6C[3] iomux select 2'b00: gpio 2'b01: sdmmc0_data3 2'b10: jtag_tck 2'b11: reserved
5:4	RW	0x1	gpio6c2_sel GPIO6C[2] iomux select 2'b00: gpio 2'b01: sdmmc0_data2 2'b10: jtag_tdi 2'b11: reserved
3:2	RW	0x1	gpio6c1_sel GPIO6C[1] iomux select 2'b00: gpio 2'b01: sdmmc0_data1 2'b10: jtag_trstn 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio6c0_sel GPIO6C[0] iomux select 2'b00: gpio 2'b01: sdmmc0_data0 2'b10: jtag_tms 2'b11: reserved

GRF_GPIO7A_IOMUX
Address: Operational Base + offset (0x006c)
GPIO7A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio7a7_sel GPIO7A[7] iomux select 2'b00: gpio 2'b01: uart3gps_sin 2'b10: gps_mag 2'b11: hsadct1_data0
13:3	RO	0x0	reserved
2	RW	0x0	gpio7a1_sel GPIO7A[1] iomux select 1'b0: gpio 1'b1: pwm_1
1:0	RW	0x0	gpio7a0_sel GPIO7A[0] iomux select 2'b00: gpio 2'b01: pwm_0 2'b10: vop0_pwm 2'b11: vop1_pwm

GRF_GPIO7B_IOMUX
Address: Operational Base + offset (0x0070)
GPIO7B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio7b7_sel GPIO7B[7] iomux select 2'b00: gpio 2'b01: isp_shuttertrig 2'b10: spi1_txd 2'b11: reserved
13:12	RW	0x0	gpio7b6_sel GPIO7B[6] iomux select 2'b00: gpio 2'b01: isp_prelighttrig 2'b10: spi1_rxd 2'b11: reserved
11:10	RW	0x0	gpio7b5_sel GPIO7B[5] iomux select 2'b00: gpio 2'b01: isp_flashtrigout 2'b10: spi1_csn0 2'b11: reserved
9:8	RW	0x0	gpio7b4_sel GPIO7B[4] iomux select 2'b00: gpio 2'b01: isp_shutteren 2'b10: spi1_clk 2'b11: reserved
7:6	RW	0x0	gpio7b3_sel GPIO7B[3] iomux select 2'b00: gpio 2'b01: usb_drvvbus1 2'b10: edp_hotplug 2'b11: reserved
5:4	RW	0x0	gpio7b2_sel GPIO7B[2] iomux select 2'b00: gpio 2'b01: uart3gps_rtsn 2'b10: usb_drvvbus0 2'b11: reserved
3:2	RW	0x0	gpio7b1_sel GPIO7B[1] iomux select 2'b00: gpio 2'b01: uart3gps_ctsn 2'b10: gps_rfclk 2'b11: gpst1_clk

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio7b0_sel GPIO7B[0] iomux select 2'b00: gpio 2'b01: uart3gps_sout 2'b10: gps_sig 2'b11: hsadct1_data1

GRF_GPIO7CL_IOMUX
Address: Operational Base + offset (0x0074)
GPIO7CL iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:12	RW	0x0	gpio7c3_sel GPIO7C[3] iomux select 2'b00: gpio 2'b01: i2c5hdmi_sda 2'b10: edphdmii2c_sda 2'b11: reserved
11:9	RO	0x0	reserved
8	RW	0x0	gpio7c2_sel GPIO7C[2] iomux select 1'b0: gpio 1'b1: i2c4tp_scl
7:5	RO	0x0	reserved
4	RW	0x0	gpio7c1_sel GPIO7C[1] iomux select 1'b0: gpio 1'b1: i2c4tp_sda
3:2	RO	0x0	reserved
1:0	RW	0x0	gpio7c0_sel GPIO7C[0] iomux select 2'b00: gpio 2'b01: isp_flashtrigin 2'b10: edphdmi_cecinoutt1 2'b11: reserved

GRF_GPIO7CH_IOMUX
Address: Operational Base + offset (0x0078)
GPIO7CH iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio7c7_sel GPIO7C[7] iomux select 3'b000: gpio 3'b001: uart2dbg_sout 3'b010: uart2dbg_sirout 3'b011: pwm_3 3'b100: edphdmi_cecinout other: reserved
11:10	RO	0x0	reserved
9:8	RW	0x0	gpio7c6_sel GPIO7C[6] iomux select 2'b00: gpio 2'b01: uart2dbg_sin 2'b10: uart2dbg_sirin 2'b11: pwm_2
7:2	RO	0x0	reserved
1:0	RW	0x0	gpio7c4_sel GPIO7C[4] iomux select 2'b00: gpio 2'b01: i2c5hdmi_scl 2'b10: edphdmii2c_scl 2'b11: reserved

GRF_GPIO8A_IOMUX
Address: Operational Base + offset (0x0080)
GPIO8A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio8a7_sel GPIO8A[7] iomux select 2'b00: gpio 2'b01: spi2_csn0 2'b10: sc_detect 2'b11: reserve
13:12	RW	0x0	gpio8a6_sel GPIO8A[6] iomux select 2'b00: gpio 2'b01: spi2_clk 2'b10: sc_io 2'b11: reserve
11:10	RW	0x0	gpio8a5_sel GPIO8A[5] iomux select 2'b00: gpio 2'b01: i2c2sensor_scl 2'b10: sc_clk 2'b11: reserved
9:8	RW	0x0	gpio8a4_sel GPIO8A[4] iomux select 2'b00: gpio 2'b01: i2c2sensor_sda 2'b10: sc_rst 2'b11: reserved
7:6	RW	0x0	gpio8a3_sel GPIO8A[3] iomux select 2'b00: gpio 2'b01: spi2_csn1 2'b10: sc_iot1 2'b11: reserved
5	RO	0x0	reserved
4	RW	0x0	gpio8a2_sel GPIO8A[2] iomux select 1'b0: gpio 1'b1: sc_detectt1
3:2	RW	0x0	gpio8a1_sel GPIO8A[1] iomux select 2'b00: gpio 2'b01: ps2_data 2'b10: sc_vcc33v 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio8a0_sel GPIO8A[0] iomux select 2'b00: gpio 2'b01: ps2_clk 2'b10: sc_vcc18v 2'b11: reserved

GRF_GPIO8B_IOMUX
Address: Operational Base + offset (0x0084)
GPIO8B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio8b1_sel GPIO8B[1] iomux select 2'b00: gpio 2'b01: spi2_txd 2'b10: sc_clk 2'b11: reserve
1:0	RW	0x0	gpio8b0_sel GPIO8B[0] iomux select 2'b00: gpio 2'b01: spi2_rxd 2'b10: sc_rst 2'b11: reserve

GRF_GPIO1H_SR
Address: Operational Base + offset (0x0104)
GPIO1C/D SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x0f	gpio1d_sr GPIO1D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RO	0x0	reserved

GRF_GPIO2L_SR
Address: Operational Base + offset (0x0108)
GPIO2A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio2b_sr GPIO2B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio2a_sr GPIO2A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO2H_SR
Address: Operational Base + offset (0x010c)
GPIO2C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2c_sr GPIO2C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO3L_SR
Address: Operational Base + offset (0x0110)
GPIO3A/B SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x20	gpio3b_sr GPIO3B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0xff	gpio3a_sr GPIO3A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO3H_SR
Address: Operational Base + offset (0x0114)
GPIO3C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:8	RW	0xff	gpio3d_sr GPIO3D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x04	gpio3c_sr GPIO3C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO4L_SR
Address: Operational Base + offset (0x0118)
GPIO4A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x01	gpio4b_sr GPIO4B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x20	gpio4a_sr GPIO4A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO4H_SR
Address: Operational Base + offset (0x011c)
GPIO4C/D SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio4d_sr GPIO4D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio4c_sr GPIO4C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO5L_SR
Address: Operational Base + offset (0x0120)
GPIO5A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio5b_sr GPIO5B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RO	0x0	reserved

GRF_GPIO5H_SR
Address: Operational Base + offset (0x0124)
GPIO5C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio5c_sr GPIO5C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO6L_SR
Address: Operational Base + offset (0x0128)
GPIO6A/B SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x01	gpio6b_sr GPIO6B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio6a_sr GPIO6A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO6H_SR
Address: Operational Base + offset (0x012c)
GPIO6C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x10	gpio6c_sr GPIO6C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO7L_SR
Address: Operational Base + offset (0x0130)
GPIO7A/B SR control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio7b_sr GPIO7B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio7a_sr GPIO7A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO7H_SR
Address: Operational Base + offset (0x0134)
GPIO7C/D SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio7c_sr GPIO7C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO8L_SR
Address: Operational Base + offset (0x0138)
GPIO8A/B SR control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio8b_sr GPIO8B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio8a_sr GPIO8A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

GRF_GPIO1D_P
Address: Operational Base + offset (0x014c)
GPIO1D PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio1d_p GPIO1D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2A_P
Address: Operational Base + offset (0x0150)
GPIO2A PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio2a_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2B_P
Address: Operational Base + offset (0x0154)
GPIO2B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio2b_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2C_P
Address: Operational Base + offset (0x0158)
GPIO2C PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio2c_p GPIO2C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3A_P
Address: Operational Base + offset (0x0160)
GPIO3A PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio3a_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3B_P
Address: Operational Base + offset (0x0164)
GPIO3B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5699	gpio3b_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3C_P
Address: Operational Base + offset (0x0168)
GPIO3C PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio3c_p GPIO3C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3D_P
Address: Operational Base + offset (0x016c)
GPIO3D PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio3d_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4A_P
Address: Operational Base + offset (0x0170)
GPIO4A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio4a_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4B_P
Address: Operational Base + offset (0x0174)
GPIO4B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa5	gpio4b_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4C_P
Address: Operational Base + offset (0x0178)
GPIO4C PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5559	gpio4c_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4D_P
Address: Operational Base + offset (0x017c)
GPIO4D PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5a99	gpio4d_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO5B_P
Address: Operational Base + offset (0x0184)
GPIO5B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x6559	gpio5b_p GPIO5B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO5C_P
Address: Operational Base + offset (0x0188)
GPIO5C PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaa9	gpio5c_p GPIO5C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6A_P
Address: Operational Base + offset (0x0190)
GPIO6A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio6a_p GPIO6A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6B_P
Address: Operational Base + offset (0x0194)
GPIO6B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaa96	gpio6b_p GPIO6B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO6C_P
Address: Operational Base + offset (0x0198)
GPIO6C PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5655	gpio6c_p GPIO6C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7A_P

Address: Operational Base + offset (0x01a0)

GPIO7A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x59aa	gpio7a_p GPIO7A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7B_P
Address: Operational Base + offset (0x01a4)
GPIO7B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xa696	gpio7b_p GPIO7B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO7C_P
Address: Operational Base + offset (0x01a8)
GPIO7C PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio7c_p GPIO7C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO8A_P
Address: Operational Base + offset (0x01b0)
GPIO8A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x6555	gpio8a_p GPIO8A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO8B_P
Address: Operational Base + offset (0x01b4)
GPIO8B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio8b_p GPIO8B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO1D_E
Address: Operational Base + offset (0x01cc)
GPIO1D drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x55aa	gpio1d_e GPIO1D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2A_E
Address: Operational Base + offset (0x01d0)
GPIO2A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio2a_e GPIO2A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2B_E
Address: Operational Base + offset (0x01d4)
GPIO2B drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio2b_e GPIO2B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO2C_E
Address: Operational Base + offset (0x01d8)
GPIO2C drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio2c_e GPIO2C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3A_E
Address: Operational Base + offset (0x01e0)
GPIO3A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio3a_e GPIO3A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3B_E
Address: Operational Base + offset (0x01e4)
GPIO3B drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio3b_e GPIO3B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3C_E
Address: Operational Base + offset (0x01e8)
GPIO3C drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5565	gpio3c_e GPIO3C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO3D_E
Address: Operational Base + offset (0x01ec)
GPIO3D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xaaaa	gpio3d_e GPIO3D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4A_E
Address: Operational Base + offset (0x01f0)
GPIO4A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5955	gpio4a_e GPIO4A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4B_E
Address: Operational Base + offset (0x01f4)
GPIO4B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5556	gpio4b_e GPIO4B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4C_E
Address: Operational Base + offset (0x01f8)
GPIO4C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio4c_e GPIO4C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO4D_E
Address: Operational Base + offset (0x01fc)
GPIO4D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio4d_e GPIO4D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO5B_E
Address: Operational Base + offset (0x0204)
GPIO5B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio5b_e GPIO5B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO5C_E
Address: Operational Base + offset (0x0208)
GPIO5C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio5c_e GPIO5C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6A_E
Address: Operational Base + offset (0x0210)
GPIO6A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio6a_e GPIO6A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6B_E
Address: Operational Base + offset (0x0214)
GPIO6B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio6b_e GPIO6B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO6C_E
Address: Operational Base + offset (0x0218)
GPIO6C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio6c_e GPIO6C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7A_E
Address: Operational Base + offset (0x0220)
GPIO7A drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio7a_e GPIO7A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7B_E
Address: Operational Base + offset (0x0224)
GPIO7B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio7b_e GPIO7B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO7C_E
Address: Operational Base + offset (0x0228)
GPIO7C drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio7c_e GPIO7C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO8A_E
Address: Operational Base + offset (0x0230)
GPIO8A drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio8a_e GPIO8A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO8B_E
Address: Operational Base + offset (0x0234)
GPIO8B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio8b_e GPIO8B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

GRF_GPIO_SMT
Address: Operational Base + offset (0x0240)
GPIO smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x1	gpio8a1_smt GPIO8A_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
10	RW	0x1	gpio8a0_smt GPIO8A_0 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
9	RW	0x1	gpio7c4_smt GPIO7C_4 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
8	RW	0x1	gpio7c3_smt GPIO7C_3 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
7	RW	0x1	gpio7c2_smt GPIO7C_2 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
6	RW	0x1	gpio7c1_smt GPIO7C_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
5	RW	0x1	gpio2c1_smt GPIO2C_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
4	RW	0x1	gpio2c0_smt GPIO2C_0 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
3	RW	0x1	gpio6b2_smt GPIO6B_2 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
2	RW	0x1	gpio6b1_smt GPIO6B_1 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled
1	RW	0x1	gpio8a5_smt GPIO8A_5 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

Bit	Attr	Reset Value	Description
0	RW	0x1	gpio8a4_smt GPIO8A_4 SMT control 1'b0: No hysteresis 1'b1: Schmitt trigger enabled

GRF_SOC_CON0

Address: Operational Base + offset (0x0244)

SoC control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	pause_mmc_peri PERI MMC AHB bus arbiter pause control
14	RW	0x0	pause_emem_peri PERI EMEM AHB bus arbiter pause control
13	RW	0x0	pause_usb_peri PERI USB AHB bus arbiter pause control
12	RW	0x1	grf_force_jtag Force select jtag function from sdmmc0 IO
11	RW	0x1	grf_core_idle_req_mode_sel1 core idle request mode selection 1
10	RW	0x1	grf_core_idle_req_mode_sel0 core idle request mode selection 0
9	RW	0x0	ddr1_16bit_en DDR Channel 1 interface 16bit enable
8	RW	0x0	ddr0_16bit_en DDR Channel 0 interface 16bit enable

Bit	Attr	Reset Value	Description
7	RW	0x0	vcodec_sel vdpu vepu clock select 1'b0: select vepu aclk as vcodec main clock 1'b1: select vdpu aclk as vcodec main clock
6	RW	0x0	upctl1_c_active_in Channel 1 DDR clock active in External signal from system that flags if a hardware low power request can be accepted or should always be denied. 1'b0: may be accepted 1'b1: will be denied
5	RW	0x0	upctl0_c_active_in Channel 0 DDR clock active in External signal from system that flags if a hardware low power request can be accepted or should always be denied. 1'b0: may be accepted 1'b1: will be denied
4	RW	0x1	msch1_mainddr3 Channel 1 DDR3 mode control 1'b1: DDR3 mode
3	RW	0x1	msch0_mainddr3 Channel 0 DDR3 mode control 1'b1: DDR3 mode
2	RW	0x0	msch1_mainpartialpop msch1_mainpartialpop bit control
1	RW	0x0	msch0_mainpartialpop msch0_mainpartialpop bit control
0	RO	0x0	reserved

GRF_SOC_CON1
Address: Operational Base + offset (0x0248)
SoC control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x1	rmii_mode RMII mode selection 1'b1: RMII mode
13:12	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
11	RW	0x0	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
10	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
9	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
8:6	RW	0x1	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	host_remap Host interface remap control
4:0	RO	0x0	reserved

GRF_SOC_CON2
Address: Operational Base + offset (0x024c)
SoC control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13	RW	0x0	upctl1_lpddr3_odt_en Channel 1 DDR odt enable in LPDDR3 mode 1'b1: ODT enable 1'b0: ODT disable
12	RW	0x0	upctl1_bst_diable Channel 1 DDR controller burst termination disable control 1'b1: disable 1'b0: enable
11	RW	0x0	lpddr3_en1 Channel 1 LPDDR3 mode control 1'b1: LPDDR3 mode
10	RW	0x0	upctl0_lpddr3_odt_en Channel 0 DDR odt enable in LPDDR3 mode 1'b1: ODT enable 1'b0: ODT disable
9	RW	0x0	upctl0_bst_diable Channel 0 DDR controller burst termination disable control 1'b1: disable 1'b0: enable

Bit	Attr	Reset Value	Description
8	RW	0x0	lpddr3_en0 Channel 0 LPDDR3 mode control 1'b1: LPDDR3 mode
7	RW	0x0	grf_poc_flash0_ctrl Flash0 IO domain 1.8V selection source 1'b0: GPIO3C_3 to decide the flash0 IO domain voltage, when GPIO3C_3 high, the voltage is 1.8V 1'b1: grf_io_vsel[2] to decide the flash0 IO domain voltage, when grf_io_vsel[2] high, the voltage is 1.8V
6	RW	0x0	simcard_mux_sel sim card iomux solution selection 1'b1: use GPIO8A[5:2] 1'b0: use GPIO8A[7:6] and GPIO8B[1:0]
5:2	RO	0x0	reserved
1	RW	0x1	grf_spdif_2ch_en SPDIF solution selection 1'b0: 8CH SPDIF 1'b1: 2CH SPDIF
0	RW	0x0	pwm_sel PWM solution selection 1'b1: RK PWM 1'b0: PWM(old)

GRF_SOC_CON3
Address: Operational Base + offset (0x0250)
SoC control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15	RW	0x0	rxclk_dly_ena_gmac RGMII RX clock delayline enable 1'b1: enable 1'b0: disable
14	RW	0x0	txclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
13:7	RW	0x10	clk_rx_dl_cfg_gmac RGMII RX clock delayline value
6:0	RW	0x10	clk_tx_dl_cfg_gmac RGMII TX clock delayline value

GRF_SOC_CON4
Address: Operational Base + offset (0x0254)
SoC control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	dfi_eff_stat_en1 Channel 1 DFI monitor efficiency statistics enable
14	RW	0x0	dfi_eff_stat_en0 Channel 0 DFI monitor efficiency statistics enable
13	RW	0x0	mobile_ddr_sel Mobile DDR selection in DFI monitor 1'b1: mobile DDR(LPDDR2/LPDDR3) 1'b0: DDR3
12:10	RW	0x1	host_l3_ocp_sconnect_grf Host interface l3_ocp_sconnect signal control

Bit	Attr	Reset Value	Description
9:8	RW	0x2	host_txport_rst_val_grf Host interface txport_rst_val signal control
7:6	RW	0x0	host_rxport_rst_val_grf Host interface rxport_rst_val signal control
5	RW	0x0	host_wakereq_grf Host interface wakereq signal control
4:3	RW	0x0	host_eoi_in_grf Host interface eoi_in signal control
2	RW	0x1	host_mstandy_in_grf Host interface mstandy_in signal control
1	RW	0x1	host_mwait_grf Host interface mwait signal control
0	RW	0x1	host_sidle_req_grf Host interface sidle_req signal control

GRF_SOC_CON5
Address: Operational Base + offset (0x0258)
SoC control register 5

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	host_mux_sel Host interface mux selection 1'b1: 8bits input, 16bits output 1'b0: 8bits output, 16bits input
14	RW	0x0	tsp0_inout_sel TSP0 input/output selection 1'b1: output 1'b0: input

Bit	Attr	Reset Value	Description
13	RW	0x0	hsadc_clkout_en hsadc clkout enable 1'b1: hsadc_clkout 1'b0: gps_clk
12:3	RW	0x190	host_fclk_freq_rst_val_grf Host interface fclk_freq_rst_val signal control
2:1	RW	0x3	host_l3_iocp_mconnect_grf Host interface l3_iocp_mconnect signal control
0	RW	0x1	host_l3_ocp_mdiscbehave_grf Host interface l3_ocp_mdiscbehave signal control

GRF_SOC_CON6
Address: Operational Base + offset (0x025c)
SoC control register 6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	grf_hdmi_edp_sel HDMI source selection 1'b1: from HDMI controller 1'b0: from eDP controller
14	RW	0x0	dsi_csi_testbus_sel MIPI PHY TX1RX1 test bus source selection 1'b1: CSI host 1'b0: DSI host1
13	RW	0x0	hsadc_extclk_mux_sel HSADC external clock source selection 1'b1: GPIO7B[1] 1'b0: GPIO2B[2]

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_27m_mux_sel 27M clock input source selection 1'b1: GPIO0C[1] 1'b0: GPIO0B[5]
11	RW	0x0	grf_con_dsi1_dpicolorm DSI host1 dpicolorm bit control
10	RW	0x0	grf_con_dsi1_dpishutdn DSI host1 dpishutdn bit control
9	RW	0x0	grf_con_dsi1_lcdc_sel DSI host1 data from VOP selection 1'b1: VOP LIT output to DSI host1 1'b0: VOP BIG output to DSI host1
8	RW	0x0	grf_con_dsi0_dpicolorm DSI host0 dpicolorm bit control
7	RW	0x0	grf_con_dsi0_dpishutdn DSI host0 dpishutdn bit control
6	RW	0x0	grf_con_dsi0_lcdc_sel DSI host0 data from VOP selection 1'b1: VOP LIT output to DSI host0 1'b0: VOP BIG output to DSI host0
5	RW	0x0	grf_con_edp_lcdc_sel eDP data from VOP selection 1'b1: VOP LIT output to eDP 1'b0: VOP BIG output to eDP
4	RW	0x0	grf_con_hdmi_lcdc_sel HDMI data from VOP selection 1'b1: VOP LIT output to HDMI 1'b0: VOP BIG output to HDMI
3	RW	0x0	grf_con_lvds_lcdc_sel LVDS data from VOP selection 1'b1: VOP LIT output to LVDS 1'b0: VOP BIG output to LVDS
2	RW	0x0	grf_con_iep_vop_sel IEP connect to VOP selection 1'b1: IEP connect to VOP LIT 1'b0: IEP connect to VOP BIG
1	RW	0x0	grf_con_isp_dphy_sel ISP connect to MIPI PHY selection 1'b1: MIPI PHY TX1RX1 1'b0: MIPI PHY RX0
0	RW	0x0	grf_con_disable_isp Disable ISP control

GRF_SOC_CON7
Address: Operational Base + offset (0x0260)

SoC control register 7

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_lvds_pwrdwn LVDS PHY power down control 1'b1: power down 1'b0: power up
14	RO	0x0	reserved
13	RW	0x0	grf_lvds_lcdc_trace_sel LVDS IO used as trace bus enable 1'b1: used as trace bus 1'b0: used as LVDS IO or LCDC RGB output port
12	RW	0x0	grf_lvds_con_enable_2 LVDS controller enable_2 signal control
11	RW	0x0	grf_lvds_con_enable_1 LVDS controller enable_1 signal control
10	RW	0x0	grf_lvds_con_den_polarity LVDS controller den_polarity signal control
9	RW	0x0	grf_lvds_con_hs_polarity LVDS controller hs_polarity signal control
8	RW	0x0	grf_lvds_con_clkinv LVDS controller clkinv signal control
7	RW	0x0	grf_lvds_con_startphase LVDS controller startphase signal control
6	RW	0x0	grf_lvds_con_ttl_en LVDS controller ttl_en signal control
5	RW	0x0	grf_lvds_con_startsel LVDS controller startsel signal control
4	RW	0x0	grf_lvds_con_chasel LVDS controller chasel signal control

Bit	Attr	Reset Value	Description
3	RW	0x0	grf_lvds_con_msbsel LVDS controller msbsel signal control
2:0	RW	0x0	grf_lvds_con_select LVDS controller select signal control

GRF_SOC_CON8
Address: Operational Base + offset (0x0264)
SoC control register 8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_edp_hdcp_protect eDP HDCP function protection 1'b1: protect 1'b0: not protect
14	RW	0x0	grf_edp_bist_en eDP PHY BIST function enabled 1'b1: enable 1'b0: disable
13	RW	0x0	grf_edp_mem_ctrl_sel eDP memory control selection 1'b1: controlled by eDP controller internal logic 1'b0: controlled by APB BUS
12	RW	0x0	grf_hdmi_cec_mux_sel HDMI cec source selection 1'b1: from GPIO7C[0] 1'b0: from GPIO7C[7]

Bit	Attr	Reset Value	Description
11:8	RW	0x0	grf_dphy_tx0_forcetxstopmode MIPI DPHY TX0 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
7:4	RW	0x0	grf_dphy_tx0_forcerxmode MIPI DPHY TX0 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0xe	grf_dphy_tx0_turndisable MIPI DPHY TX0 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON9
Address: Operational Base + offset (0x0268)
SoC control register 9

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_dphy_tx1rx1_enable MIPI DPHY TX1RX1 enable lane N module(N=0~3). Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
11:8	RW	0x0	grf_dphy_tx1rx1_forcetxstopmode MIPI DPHY TX1RX1 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

Bit	Attr	Reset Value	Description
7:4	RW	0x0	grf_dphy_tx1rx1_forcerxmode MIPI DPHY TX1RX1 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0xe	grf_dphy_tx1rx1_turndisable MIPI DPHY TX1RX1 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON10
Address: Operational Base + offset (0x026c)
SoC control register 10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_dphy_rx0_enable MIPI DPHY RX0 enable lane N module(N=0~3). Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
11:8	RW	0x0	grf_dphy_rx0_forcetxstopmode MIPI DPHY RX0 force lane into transmit mode and generate stop sate. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
7:4	RW	0x0	grf_dphy_rx0_forcerxmode MIPI DPHY RX0 force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

Bit	Attr	Reset Value	Description
3:0	RW	0xf	grf_dphy_rx0_turndisable MIPI DPHY RX0 disable turn around control Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON11
Address: Operational Base + offset (0x0270)
SoC control register 11

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio8_a2_fall_edge_irq_pd GIIO8A[2] fall edge interrupt pending status 1'b1: enable 1'b0: disable
14	RW	0x0	gpio8_a2_fall_edge_irq_en GIIO8A[2] fall edge interrupt enable 1'b1: enable 1'b0: disable
13	RW	0x0	gpio8_a2_rise_edge_irq_pd GIIO8A[2] rise edge interrupt pending status 1'b1: enable 1'b0: disable
12	RW	0x0	gpio8_a2_rise_edge_irq_en GIIO8A[2] rise edge interrupt enable 1'b1: enable 1'b0: disable
11	RW	0x0	gpio7_c6_fall_edge_irq_pd GIIO7C[6] fall edge interrupt pending status 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
10	RW	0x0	gpio7_c6_fall_edge_irq_en GIIO7C[6] fall edge interrupt enable 1'b1: enable 1'b0: disable
9	RW	0x0	gpio7_c6_rise_edge_irq_pd GIIO7C[6] rise edge interrupt pending status 1'b1: enable 1'b0: disable
8	RW	0x0	gpio7_c6_rise_edge_irq_en GIIO7C[6] rise edge interrupt enable 1'b1: enable 1'b0: disable
7	RW	0x0	gpio7_b3_fall_edge_irq_pd GIIO7B[3] fall edge interrupt pending status 1'b1: enable 1'b0: disable
6	RW	0x0	gpio7_b3_fall_edge_irq_en GIIO7B[3] fall edge interrupt enable 1'b1: enable 1'b0: disable
5	RW	0x0	gpio7_b3_rise_edge_irq_pd GIIO7B[3] rise edge interrupt pending status 1'b1: enable 1'b0: disable
4	RW	0x0	gpio7_b3_rise_edge_irq_en GIIO7B[3] rise edge interrupt enable 1'b1: enable 1'b0: disable
3	RW	0x0	sd_detectn_fall_edge_irq_pd sdmmc detect_n fall edge interrupt pending status 1'b1: enable 1'b0: disable
2	RW	0x0	sd_detectn_fall_edge_irq_en sdmmc0 detect_n signal fall edge interrupt enable 1'b1: enable 1'b0: disable
1	RW	0x0	sd_detectn_rise_edge_irq_pd sdmmc detect_n rise edge interrupt pending status 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
0	RW	0x0	sd_detectn_rise_edge_irq_en sdmmc0 detect_n signal rise edge interrupt enable 1'b1: enable 1'b0: disable

GRF_SOC_CON12
Address: Operational Base + offset (0x0274)
SoC control register 12

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RW	0x000	grf_edp_frq_vid_ck_in eDP PHY frequency information of vid_ck_in frq_vid_ck_in<8:0>/8 = freq(vid_ck_in)/10
6	RW	0x0	grf_edp_vid_lock eDP PHY input video PLL stable indicator 1'b1: stable 1'b0: unstable
5	RW	0x0	grf_edp_iddq_en eDP PHY IDDQ enable 1'b0: disable 1'b1: enable, all circuits are power down, all IO are high-z
4	RW	0x1	grf_edp_ref_clk_sel eDP PHY reference clock source selection 1'b0: from PAD(IO_EDP_OSC_CLK_24M) 1'b1: from internal 24MHz or 27MHz clock
3	RW	0x0	grf_edp_dc_tp_i eDP PHY analog DC test point input
2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x3	grf_filter_cnt_sel the counter select for sd card detect filter 2'b00: 5ms 2'b01: 15ms 2'b10: 35ms 2'b11: 50ms

GRF_SOC_CON13

Address: Operational Base + offset (0x0278)

SoC control register 13

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	grf_edp_tx_bscan_data eDP TX boundary data bit0: boundary data to ch0 bit1: boundary data to ch1 bit2: boundary data to ch2 bit3: boundary data to ch3
11	RW	0x0	grf_edp_tx_bscan_en eDP TX boundary enable 1'b0: disable 1'b1: enable
10	RO	0x0	reserved
9:5	RW	0x00	grf_uart_rts_sel UART polarity selection for rts port Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT. 1'b1: high asserted 1'b0: low asserted

Bit	Attr	Reset Value	Description
4:0	RW	0x00	grf_uart_cts_sel UART polarity selection for cts port Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT. 1'b1: high asserted 1'b0: low asserted

GRF_SOC_CON14

Address: Operational Base + offset (0x027c)

SoC control register 14

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_dphy_tx1rx1_basedir MIPI DPHY TX1RX1 base direction control
14	RW	0x0	grf_dphy_tx1rx1_masterslavez MIPI DPHY TX1RX1 master/slave control
13	RW	0x0	dphy_rx1_src_sel MIPI DPHY RX1 source selection 1'b1: isp 1'b0: csi host
12	RW	0x0	dphy_tx1rx1_enableclk MIPI DPHY TX1RX1 enable clock Lane module
11	RO	0x0	reserved
10:3	RW	0x00	dphy_rx0_testdin MIPI DPHY RX0 test bus input data
2	RW	0x0	dphy_rx0_testen MIPI DPHY RX0 test bus enable
1	RW	0x0	dphy_rx0_testclk MIPI DPHY RX0 test bus clock

Bit	Attr	Reset Value	Description
0	RW	0x0	dphy_rx0_testclr MIPI DPHY RX0 test bus clear control

GRF_SOC_STATUS0
Address: Operational Base + offset (0x0280)
SoC status register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ddrupctl1_bbflags DDR channel 1 NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.
15:0	RW	0x0000	ddrupctl0_bbflags DDR channel 0 NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when precharge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.

GRF_SOC_STATUS1
Address: Operational Base + offset (0x0284)
SoC status register 1

Bit	Attr	Reset Value	Description
31	RW	0x0	gmac_portselect MAC Port Select A high indicates an MII interface, and a low a GMII interface.
30:26	RO	0x0	reserved
25:22	RW	0x0	hsic_stat_ehci_lpsmc_state HSIC ehci_lpsmc_state bit status
21:16	RW	0x00	hsic_stat_ehci_usbsts HSIC ehci_usbsts bit status

Bit	Attr	Reset Value	Description
15:13	RW	0x0	ddrupctl1_stat 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req
12:10	RW	0x0	ddrupctl0_stat 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req
9	RW	0x0	newpll_lock NEW PLL lock status
8	RW	0x0	generalpll_lock GENERAL PLL lock status
7	RW	0x0	codecpll_lock CODEC PLL lock status
6	RW	0x0	armpll_lock ARM PLL lock status
5	RW	0x0	ddrpll_lock DDR PLL lock status
4	RW	0x0	newpll_clk NEW PLL clock output
3	RW	0x0	generalpll_clk GENERAL PLL clock output
2	RW	0x0	codecpll_clk CODEC PLL clock output
1	RW	0x0	armpll_clk ARM PLL clock output
0	RW	0x0	ddrpll_clk DDR PLL clock output

GRF_SOC_STATUS2

Address: Operational Base + offset (0x0288)

SoC status register 2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RW	0x0	usbhost0_stat_ohci_bufacc USB HOST0 ohci_bufacc signal status
29	RW	0x0	usbhost0_stat_ohci_rmtwkp USB HOST0 ohci_rmtwkp signal status
28:27	RW	0x0	usbhost0_utmi_linestate USB HOST0 utmi_linestate signal status
26	RW	0x0	usbhost0_stat_ohci_drwe USB HOST0 ohci_drwe signal status
25	RW	0x0	usbhost0_stat_ohci_rwe USB HOST0 ohci_rwe signal status
24	RW	0x0	usbhost0_stat_ohci_ccs USB HOST0 ohci_ccs signal status
23	RW	0x0	usbhost1_utmiotg_iddig USB HOST1 utmiotg_iddig signal status
22:21	RW	0x0	usbhost1_utmi_linestate USB HOST1 utmi_linestate signal status
20	RW	0x0	usbhost1_utmisrp_bvalid USB HOST1 utmisrp_bvalid signal status
19	RW	0x0	usbhost1_utmiotg_vbusvalid USB HOST1 utmiotg_vbusvalid signal status
18	RW	0x0	usbhost1_chirp_on USB HOST1 chirp_on signal status
17	RW	0x0	usbotg_utmiotg_iddiq USB OTG utmiotg_iddig signal status
16:15	RW	0x0	usbotg_utmi_linestate USB OTG utmi_linestate signal status
14	RW	0x0	usbotg_utmisrp_bvalid USB OTG utmisrp_bvalid
13	RW	0x0	usbotg_utmiotg_vbusvalid USB OTG utmiotg_vbusvalid signal status
12	RO	0x0	reserved
11	RW	0x0	hsic_stat_ehci_xfer_prdc HSIC ehci_xfer_prdc signal status
10:0	RW	0x000	hsic_stat_ehci_xfer_cnt HSIC ehci_xfer_cnt signal status

GRF_SOC_STATUS3
Address: Operational Base + offset (0x028c)
SoC status register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo0 DDR channel0 NIF interface FIFO0 status

GRF_SOC_STATUS4

Address: Operational Base + offset (0x0290)
SoC status register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo1 DDR channel0 NIF interface FIFO1 status

GRF_SOC_STATUS5
Address: Operational Base + offset (0x0294)
SoC status register 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo2 DDR channel0 NIF interface FIFO2 status

GRF_SOC_STATUS6
Address: Operational Base + offset (0x0298)
SoC status register 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo3 DDR channel0 NIF interface FIFO3 status

GRF_SOC_STATUS7
Address: Operational Base + offset (0x029c)
SoC status register 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo0 DDR channel1 NIF interface FIFO0 status

GRF_SOC_STATUS8
Address: Operational Base + offset (0x02a0)
SoC status register 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo1 DDR channel1 NIF interface FIFO1 status

GRF_SOC_STATUS9
Address: Operational Base + offset (0x02a4)
SoC status register 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo2 DDR channel1 NIF interface FIFO2 status

GRF_SOC_STATUS10
Address: Operational Base + offset (0x02a8)
SoC status register 10

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif1_fifo3 DDR channel1 NIF interface FIFO3 status

GRF_SOC_STATUS11
Address: Operational Base + offset (0x02ac)
SoC status register 11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_wr_num DDR channel0 DFI interface write command number

GRF_SOC_STATUS12
Address: Operational Base + offset (0x02b0)
SoC status register 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_rd_num DDR channel0 DFI interface read command number

GRF_SOC_STATUS13
Address: Operational Base + offset (0x02b4)
SoC status register 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_eff_act_num DDR channel0 DFI interface active command number

GRF_SOC_STATUS14
Address: Operational Base + offset (0x02b8)
SoC status register 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi0_timer_val DDR channel0 DFI interface statistics timer value

GRF_SOC_STATUS15
Address: Operational Base + offset (0x02bc)
SoC status register 15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_wr_num DDR channel1 DFI interface write command number

GRF_SOC_STATUS16

Address: Operational Base + offset (0x02c0)
SoC status register 16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_rd_num DDR channel1 DFI interface read command number

GRF_SOC_STATUS17
Address: Operational Base + offset (0x02c4)
SoC status register 17

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_eff_act_num DDR channel1 DFI interface active command number

GRF_SOC_STATUS18
Address: Operational Base + offset (0x02c8)
SoC status register 18

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi1_timer_val DDR channel1 DFI interface statistics timer value

GRF_SOC_STATUS19
Address: Operational Base + offset (0x02cc)
SoC status register 19

Bit	Attr	Reset Value	Description
31	RW	0x0	usbhost1_fsvminus USB HOST1 PHY fsvminus bit status
30	RW	0x0	usbhost1_fsvplus USB HOST1 PHY fsvplus bit status
29	RW	0x0	usbhost1_chgdet USB HOST1 PHY charge detect status
28	RW	0x0	usbhost0_fsvminus USB HOST0 PHY fsvminus bit status
27	RW	0x0	usbhost0_fsvplus USB HOST0 PHY fsvplus bit status
26	RW	0x0	usbhost0_chgdet USB HOST0 PHY charge detect status
25	RW	0x0	usbotg_fsvminus USB OTG PHY fsvminus bit status
24	RW	0x0	usbotg_fsvplus USB OTG PHY fsvplus bit status
23	RW	0x0	usbotg_chgdet USB OTG PHY charge detect status
22:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:11	RW	0x0	host_l3_ocp_sconnect Host interface L3 OCP sconnect status
10	RW	0x0	host_l3_ocp_tactive Host interface L3 OCP tactive status
9:8	RW	0x0	host_l3_ocp_mconnect Host interface L3 OCP mconnect status
7	RW	0x0	host_wakeack Host interface wakeack status
6:5	RW	0x0	host_eoi_out Host interface eoi_out status
4	RW	0x0	host_mwait_out Host interface mwait_out status
3	RW	0x0	host_mwakeup Host interface mwakeup status
2	RW	0x0	host_mstandby Host interface mstandby status
1:0	RW	0x0	host_sidle_ack Host interface sidle ack

GRF_SOC_STATUS20
Address: Operational Base + offset (0x02d0)
SoC status register 20

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	host_geno Host interface geno bit stauts The GENI GENO is a mechanism that allows the 2 chip to exchange flags (interupts), up to 32 independent flags are available.

GRF_SOC_STATUS21
Address: Operational Base + offset (0x02d4)
SoC status register 21

Bit	Attr	Reset Value	Description
31:26	RW	0x00	usbhost0_stat_ehci_usbsts USB host0 ehci_usbsts bit status
25:15	RW	0x000	usbhost0_stat_ehci_xfer_cnt USB host0 ehci_xfer counter status
14	RW	0x0	usbhost0_stat_ehci_xfer_prdc USB host0 ehci_xfer_prdc bit status
13:10	RW	0x0	usbhost0_stat_ehci_lpsmc_state USB host0 ehci_lpsmc_state bit status
9	RW	0x0	usbhost0_stat_ehci_bufacc USB host0 ehci_bufacc bit status
8	RW	0x0	usbhost0_stat_ohci_globalsuspend USB host0 ohci_globalsuspend bit status

Bit	Attr	Reset Value	Description
7:0	RW	0x00	dphy_rx0_testdout MIPI DPHY RX0 test bus data output

GRF_PERIDMAC_CON0
Address: Operational Base + offset (0x02e0)
PERI DMAC control register 0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	peridmac_boot_addr peridmac_boot_addr[19:12] PERI DMAC boot_addr[19:12] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
7:4	RW	0xf	peridmac_boot_periph_ns peridmac_boot_periph_ns[19:16] PERI DMAC boot_peri_ns input control Controls the security state of a peripheral request interface, when the PERI DMAC exits from reset. Note: PERI DMAC don't support secure feature, these bits don't need to be configured
3	RW	0x1	peridmac_boot_manager_ns PERI DMAC boot_manager_ns input control When the DMAC exits from reset , this signal controls the security state of the DMA manager thread: 1'b0: assigns DMA manager to the secure state 1'b1: assigns DMA manager to the Non-secure state

Bit	Attr	Reset Value	Description
2:1	RW	0x1	grf_drtype_peridmac PERI DMAC type of acknowledgement or request for peripheral signals: 2'b00: single level request 2'b01: burst level request 2'b10: acknowledging a flush request 2'b11: reserved
0	RW	0x0	peridmac_boot_from_pc PERI DMAC boot_from_pc input control Controls the location in which the DMAC0 executes its initial instruction, after it exits from reset : 1'b0: DMAC waits for an instruction from APB interface 1'b1: DMAC manager thread executes the instruction that is located at the address that boot_addr[31:0] provided.

GRF_PERIDMAC_CON1
Address: Operational Base + offset (0x02e4)
PERI DMAC control register 1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	peridmac_boot_addr peridmac_boot_addr[31:20] PERI DMAC boot_addr[31:20] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

GRF_PERIDMAC_CON2
Address: Operational Base + offset (0x02e8)
PERI DMAC control register 2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xffff	peridmac_boot_irq_ns PERI DMAC boot_irq_ns input control Controls the security state of an event-interrupt resource , when the PERI DMAC exits from reset. Note : PERI DMAC don't support secure feature, these bits don't need to be configured.

GRF_PERIDMAC_CON3
Address: Operational Base + offset (0x02ec)
PERI DMAC control register 3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	wirte_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xffff	peridmac_boot_periph_ns PERI DMAC boot_peri_ns input control Controls the security state of a peripheral request interface, when the DMAC exits from reset. Note: PERI DMAC don't support secure feature, these bits don't need to be configured.

GRF_DDRC0_CON0
Address: Operational Base + offset (0x02f0)
DDRC0 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:11	RW	0x0	ddr0_dto_lb DDR0 DTO I/O internal loopback enable
10:9	RW	0x0	ddr0_dto_te DDR0 DTO I/O on-die termination enable
8:7	RW	0x0	ddr0_dto_pdr DDR0 DTO I/O receiver power down
6:5	RW	0x0	ddr0_dto_pdd DDR0 DTO I/O driver power down
4:3	RW	0x0	ddr0_dto_iom DDR0 DTO I/O mode select
2:1	RW	0x0	ddr0_dto_oe DDR0 DTO I/O output enable
0	RW	0x0	ddr0_ato_ae Enables, if set, the analog test output I/O. Connects to the AE pin of the analog test output I/O

GRF_DDRC1_CON0
Address: Operational Base + offset (0x02f4)
DDRC1 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:11	RW	0x0	ddr1_dto_lb DDR1 DTO I/O internal loopback enable
10:9	RW	0x0	ddr1_dto_te DDR1 DTO I/O on-die termination enable
8:7	RW	0x0	ddr1_dto_pdr DDR1 DTO I/O receiver power down
6:5	RW	0x0	ddr1_dto_pdd DDR1 DTO I/O driver power down
4:3	RW	0x0	ddr1_dto_iom DDR1 DTO I/O mode select
2:1	RW	0x0	ddr1_dto_oe DDR1 DTO I/O output enable
0	RW	0x0	ddr1_ato_ae Enables, if set, the analog test output I/O. Connects to the AE pin of the analog test output I/O

GRF_CPU_CON0
Address: Operational Base + offset (0x02f8)
CPU control register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	cfgaddrfilt_en_grf A17 cfgaddrfilt_en bit control
14	RO	0x0	reserved
13:10	RW	0x0	cfgend_a17 A17 cfgend bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
9	RW	0x1	tpiu_ctl_grf tpiu_ctl bit control
8:5	RW	0x1	cs_instid_grf Coresight cs_instid bit control
4	RW	0x0	l2rstdisable_grf A17 l2rstdisable bit control
3:0	RW	0x0	l1rstdisable_grf A17 l1rstdisable bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.

GRF_CPU_CON1

Address: Operational Base + offset (0x02fc)

CPU control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0ff0	cfgaddrfilt_start_grf A17 non secure filter start address[15:0]

GRF_CPU_CON2
Address: Operational Base + offset (0x0300)
CPU control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0fff	cfgaddrfilt_end_grf A17 non secure filter end address[15:0]

GRF_CPU_CON3
Address: Operational Base + offset (0x0304)
CPU control register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	cfgnmfi_a17 A17 cfgnmfi bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
7:4	RW	0x0	cfgaddrfilt_end_grf A17 non secure filter end address[19:16]
3:0	RW	0x0	cfgaddrfilt_start_grf A17 non secure filter start address[19:16]

GRF_CPU_CON4
Address: Operational Base + offset (0x0308)
CPU control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:13	RW	0x1	l2_mem_ema_grf L2 memory EMA control
12:10	RW	0x1	owl_mem_ema_grf A17 memory EMA control
9	RW	0x0	evento_clear A17 evento clear bit control
8	RW	0x0	eventi_a17 A17 eventi bit control
7:4	RO	0x0	reserved
3:0	RW	0x0	teinit_a17 A17 teinit bit control Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.

GRF_CPU_STATUS0
Address: Operational Base + offset (0x0318)
CPU status register 0

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	evento_rising_edge evento signal rising edge
13:10	RW	0x0	owl_pmupl1_grf A17 PMU Privilege level 1 event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
9:6	RW	0x0	owl_pmupl2_grf A17 PMU Privilege level 2 event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
5:2	RW	0x0	owl_pmusecure_grf A17 pmu secure event Every bit for one core, bit3 is for core3, bit2 is for core2, bit1 is for core1, bit0 is for core0.
1	RW	0x0	jtagnsw_st_grf JTAG nsw status
0	RW	0x0	jtagtop_st_grf JTAG top status

GRF_UOC0_CON0
Address: Operational Base + offset (0x0320)
UOC0 control register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbotg_linestate_irq_pd USB OTG linestate interrupt pending bit
14	RW	0x0	usbotg_linestate_irq_en USB OTG line state interrupt enable
13	RW	0x0	usbotg_siddq USB OTG IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12	RW	0x0	usbotg_port_reset USB OTG per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11:10	RO	0x0	reserved
9:8	RW	0x0	usbotg_scaledown_mode USB OTG scale down mode control

Bit	Attr	Reset Value	Description
7:5	RW	0x4	usbotg_tune USB OTG VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbotg_disable USB OTG block disable 1'b1: the USB OTG block is power down 1'b0: the USB OTG block is power up
3:1	RW	0x4	usbotg_compdistune Disconnect Threshold Adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%
0	RW	0x1	usbotg_common_on_n USB OTG common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC0_CON1
Address: Operational Base + offset (0x0324)
UOC0 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbotg_txrisetune USB OTG HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%
13:12	RW	0x3	usbotg_txhsxvtune USB OTG transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x3	usbotg_txvreftune USB OTG HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbotg_txfslstune USB OTG FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%
3	RW	0x0	usbotg_txpreemppulsetune USB OTG HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration

Bit	Attr	Reset Value	Description
2:0	RW	0x3	usbotg_sqrxtune USB OTG squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC0_CON2
Address: Operational Base + offset (0x0328)
UOC0 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbotg_acaenb USB OTG ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA

Bit	Attr	Reset Value	Description
14	RW	0x0	usbotg_dcdenb USB OTG data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RO	0x0	reserved
12:11	RW	0x1	usbotg_txrestune USB OTG source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbotg_sleepm USB OTG sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RO	0x0	reserved
8	RW	0x1	usbotg_retenable_n USB OTG retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbotg_vdatsrcenb USB OTG battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbotg_vdatdetenb USB OTG battery charging attach/connect detection enable 1'b1: enable 1'b0: disable
5	RW	0x0	usbotg_chrgsel USB OTG battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM

Bit	Attr	Reset Value	Description
4:3	RW	0x1	usbotg_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbotg_soft_con_sel 1'b0: software control usb otg disable 1'b1: software control usb otg enable
1	RW	0x0	usbotg_vbusvldextsel USB OTG external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbotg_vbusvldext USB OTG external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC0_CON3

Address: Operational Base + offset (0x032c)

UOC0 control register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbotg_dbnce_fltr_bypass USB OTG debounce filter bypass enable
14	RO	0x0	reserved
13	RW	0x0	usbotg_iddiq_sel USB OTG iddig soft control enable 1'b1: software control 1'b0: hardware control
12	RW	0x0	usbotg_iddiq USB OTG iddig software control bit
11:8	RO	0x0	reserved
7	RW	0x0	usbotg_bypasssel transmitter digital bypass select 1'b1: transmitter digital bypass mode is enabled 1'b0: transmitte digital bypass mode is disabled
6	RW	0x0	usbotg_bypassdmen DM0 transmitter digital bypass enable 1'b1: DM0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signals 1'b0: DM0 FS/LS driver is disabled in transmitter digital byapss mode
5	RW	0x0	usbotg_utmi_termselect USB OTG utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled

Bit	Attr	Reset Value	Description
4:3	RW	0x0	usbotg_utmi_xcvrselect USB OTG utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver
2:1	RW	0x0	usbotg_utmi_opmode USB OTG utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbotg_utmi_suspend_n USB OTG suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC0_CON4
Address: Operational Base + offset (0x0330)
UOC0 control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7	RW	0x0	usbotg_id_fall_edge_irq_pd USB OTG id fall edge interrupt pending bit, write 1 to this bit , it will be cleared.

Bit	Attr	Reset Value	Description
6	RW	0x0	usbotg_id_fall_edge_irq_en USB OTG id fall edge interrupt enable
5	RW	0x0	usbotg_id_rise_edge_irq_pd USB OTG id rise edge interrupt pending bit, write 1 to this bit , it will be cleared.
4	RW	0x0	usbotg_id_rise_edge_irq_en USB OTG id rise edge interrupt enable
3	RW	0x0	usbotg_bvalid_irq_pd USB OTG bvalid interrupt pending bit, write 1 to this bit, it will be cleared.
2	RW	0x0	usbotg_bvalid_irq_en USB OTG bvalid interrupt enable
1:0	RW	0x3	linestate_cnt_sel linestate signal filter time select 2'b00: 100us 2'b01: 500us 2'b10: 2.5ms 2'b11: 15ms

GRF_UOC1_CON0
Address: Operational Base + offset (0x0334)
UOC1 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_linestate_irq_pd USB HOST0 linestate interrupt pending bit
14	RW	0x0	usbhost0_linestate_irq_en USB HOST0 line state interrupt enable

Bit	Attr	Reset Value	Description
13	RW	0x0	usbhost0_siddq USB HOST0 IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12	RW	0x0	usbhost0_port_reset USB HOST0 per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11	RW	0x1	usbhost0_word_if USB HOST0 word_if bit control
10	RW	0x0	usbhost0_sim_mode USB HOST0 sim_mode bit control
9	RW	0x1	usbhost0_incrx_en USB HOST0 incrx_en bit control
8	RW	0x1	usbhost0_incr8_en USB HOST0 incr8_en bit control
7:5	RW	0x4	usbhost0_tune USB HOST0 VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbhost0_disable USB HOST0 block disable 1'b1: the USB HOST0 block is power down 1'b0: the USB HOST0 block is power up

Bit	Attr	Reset Value	Description
3:1	RW	0x4	usbhost0_compdistune USB HOST0 disconnect threshold adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%
0	RW	0x1	usbhost0_common_on_n USB HOST0 common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC1_CON1

Address: Operational Base + offset (0x0338)

UOC1 control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbhost0_txrisetune USB HOST0 HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%
13:12	RW	0x3	usbhost0_txhsxvtune USB HOST0 transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x3	usbhost0_txvreftune USB HOST0 HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbhost0_txfslstune USB HOST0 FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%
3	RW	0x0	usbhost0_txpreemppulsetune USB HOST0 HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration

Bit	Attr	Reset Value	Description
2:0	RW	0x3	usbhost0_sqrxtune USB HOST0 squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC1_CON2
Address: Operational Base + offset (0x033c)
UOC1 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_acaenb USB HOST0 ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA

Bit	Attr	Reset Value	Description
14	RW	0x0	usbhost0_dcdenb USB HOST0 data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RW	0x0	usbhost0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
12:11	RW	0x1	usbhost0_txrestune USB HOST0 source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbhost0_sleepm USB HOST0 sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RW	0x0	usbhost0_autoppd_on_overcur USB HOST0 autoppd_on_overcur bit control
8	RW	0x1	usbhost0_retenable_n USB HOST0 retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbhost0_vdatsrcenb USB HOST0 battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbhost0_vdatdetenb USB HOST0 battery charging attach/connect detection enable 1'b1: enable 1'b0: disable
5	RW	0x0	usbhost0_chrgsel USB HOST0 battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM

Bit	Attr	Reset Value	Description
4:3	RW	0x1	usbhost0_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbhost0_soft_con_sel 1'b0: software control usb host0 disable 1'b1: software control usb host0 enable
1	RW	0x0	usbhost0_vbusvldextsel USB HOST0 external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbhost0_vbusvldext USB HOST0 external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC1_CON3

Address: Operational Base + offset (0x0340)

UOC1 control register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
14	RW	0x0	usbhost0_ohci_cntsel USB HOST0 ohci_cntsel bit control
13	RW	0x0	usbhost0_utmiotg_idpullup USB HOST0 idpullup bit control
12	RW	0x1	usbhost0_utmiotg_dppulldown USB HOST0 dppulldown bit control
11	RW	0x1	usbhost0_utmiotg_dmpulldown USB HOST0 dmpulldown bit control
10	RW	0x1	usbhost0_utmiotg_drvvbus USB HOST0 drvvbus bit contrl
9:7	RO	0x0	reserved
6	RW	0x1	usbhost0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit conrol
5	RW	0x0	usbhost0_utmi_termselect USB HOST0 utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled
4:3	RW	0x0	usbhost0_utmi_xcvrselect USB HOST0 utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver

Bit	Attr	Reset Value	Description
2:1	RW	0x0	usbhost0_utmi_opmode USB HOST0 utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbhost0_utmi_suspend_n USB HOST0 suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC1_CON4
Address: Operational Base + offset (0x0344)
UOC1 control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	usbhost0_incr4_en USB HOST0 incr4_en bit control
14	RW	0x1	usbhost0_incr16_en USB HOST0 incr16_en bit control
13	RW	0x0	usbhost0_hubsetup_min USB HOST0 hubsetup_min bit control
12	RW	0x0	usbhost0_app_start_clk USB HOST0 app_start_clk bit control
11:6	RW	0x20	usbhost0_fladj_val_common USB HOST0 fladj_val_common bit control
5:0	RW	0x20	usbhost0_fladj USB HOST0 fladj bit control

GRF_UOC2_CON0
Address: Operational Base + offset (0x0348)
UOC2 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost1_linestate_irq_pd USB HOST1 linestate interrupt pending bit
14	RW	0x0	usbhost1_linestate_irq_en USB HOST1 line state interrupt enable
13	RW	0x0	usbhost1_siddq USB HOST1 IDDQ test enable This test signal enables you to perform IDDQ testing by powering down all analog blocks. 1'b1: The analog blocks are powered down. 1'b0: The analog blocks are powered up.
12	RW	0x0	usbhost1_port_reset USB HOST1 per-port reset When asserted, this customer-specific signal resets the corresponding port transmit and receive logic without disabling the clocks within the PHY. 1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. 1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK cycles.
11:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:5	RW	0x4	usbhost1_tune USB HOST1 VBUS valid threshold adjustment This bus adjusts the voltage level for the VBUS Valid threshold. 3'b111: +9% 3'b110: +6% 3'b101: +3% 3'b100: Design default 3'b011: -3% 3'b010: -6% 3'b001: -9% 3'b000: -12%
4	RW	0x0	usbhost1_disable USB HOST1 block disable 1'b1: the USB HOST1 block is power down 1'b0: the USB HOST1 block is power up
3:1	RW	0x4	usbhost1_compdistune USB HOST1 disconnect threshold adjustment This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 3'b111: +4.5% 3'b110: +3% 3'b101: +1.5% 3'b100: Design default 3'b011: -1.5% 3'b010: -3% 3'b001: -4.5% 3'b000: -6%
0	RW	0x1	usbhost1_common_on_n USB HOST1 common block power-down control This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend or Sleep mode. 1'b1: In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. 1'b0: In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered.

GRF_UOC2_CON1
Address: Operational Base + offset (0x034c)
UOC2 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	usbhost1_txrisetune USB HOST1 HS transmitter rise/fall time adjustment This bus adjusts the rise/fall times of the high-speed waveform. 2'b11: -20% 2'b10: -15% 2'b01: design default 2'b00: +10%
13:12	RW	0x3	usbhost1_txhsxvtune USB HOST1 transmitter high-speed crossover adjustment This bus adjusts the voltage at which the DP and DM signals cross while transmitting in HS mode. 2'b11: Default setting 2'b10: +15 mV 2'b01: -15 mV 2'b00: Reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x3	usbhost1_txvreftune USB HOST1 HS DC voltage level adjustment This bus adjusts the high-speed DC level voltage. 4'b1111: +8.75% 4'b1110: +7.5% 4'b1101: +6.25% 4'b1100: +5% 4'b1011: +3.75% 4'b1010: +2.5% 4'b1001: +1.25% 4'b1000: Design default 4'b0111: -1.25% 4'b0110: -2.5% 4'b0101: -3.75% 4'b0100: -5% 4'b0011: -6.25% 4'b0010: -7.5% 4'b0001: -8.75% 4'b0000: -10%
7:4	RW	0x3	usbhost1_txfslstune USB HOST1 FS/LS source impedance adjustment This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 4'b1111: -5% 4'b0111: -2.5% 4'b0011: Design default 4'b0001: +2.5% 4'b0000: +5%
3	RW	0x0	usbhost1_txpreemppulsetune USB HOST1 HS transmitter pre-emphasis duration control This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. transition in HS mode. 1'b1: 1X, short pre-emphasis current duration 1'b0: (desian default) 2X, long pre-emphasis currrent duration

Bit	Attr	Reset Value	Description
2:0	RW	0x3	usbhost1_sqrxtune USB HOST1 squelch threshold adjustment This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 3'b111: -20% 3'b110: -15% 3'b101: -10% 3'b100: -5% 3'b011: Design default 3'b010: +5% 3'b001: +10% 3'b000: +15%

GRF_UOC2_CON2
Address: Operational Base + offset (0x0350)
UOC2 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbhost1_acaenb USB HOST1 ACA ID_OTG pin resistance detection enable 1'b1: enable detection on resistance on the ID_OTG pin of an ACA 1'b0: disable detection on resistance on the ID_OTG pin of an ACA

Bit	Attr	Reset Value	Description
14	RW	0x0	usbhost1_dcdenb USB HOST1 data contact detection enable 1'b1: IDP_SRC current is sourced onto DP, pull-down resistance on DMA is enabled 1'b0: IDP_SRC current is disable, pull-down resistance on DM is disabled
13	RO	0x0	reserved
12:11	RW	0x1	usbhost1_txrestune USB HOST1 source impedance adjustment 2'b11: source impedance is desreased by 4ohm 2'b10: source impedance is desreased by 2ohm 2'b01: design default 2'b00: source impedance is desreased by 1.5ohm
10	RW	0x1	usbhost1_sleepm USB HOST1 sleep mode enable Asserting this signal place the USB PHY in sleep mode. 1'b0: sleep mode enable 1'b1: normal mode
9	RO	0x0	reserved
8	RW	0x1	usbhost1_retenable_n USB HOST1 retention mode enable 0: retention mode enable 1: retention mode disable
7	RW	0x0	usbhost1_vdatsrcenb USB HOST1 battery charging sourcing select 1'b1: data source voltage is enable 1'b0: data source voltage is disable
6	RW	0x0	usbhost1_vdatdetenb USB HOST1 battery charging attach/connect detection enable 1'b1: enable 1'b0: disable
5	RW	0x0	usbhost1_chrgsel USB HOST1 battery charging source select 1'b1: data source voltage is sourced onto DM and sunk from DP 1'b0: data source voltage is sourced onto DP and sunk from DM

Bit	Attr	Reset Value	Description
4:3	RW	0x1	usbhost1_txpreempamptune 2'b11: 3X pre-emphasis current 2'b10: 2X pre-emphasis current 2'b01: 1X pre-emphasis current 2'b00: HS Transmitter Pre-Emphasis is disabled
2	RW	0x0	usbhost1_soft_con_sel 1'b0: software control usb host1 disable 1'b1: software control usb host1 enable
1	RW	0x0	usbhost1_vbusvldextsel USB HOST1 external VBUS valid select This signal selects the VBUSVLDEXT input or the internal Session Valid comparator to indicate when the VBUS signal on the USB cable is valid. 1'b1: The VBUSVLDEXT input is used. 1'b0: The internal Session Valid comparator is used.
0	RW	0x0	usbhost1_vbusvldext USB HOST1 external VBUS valid indicator This signal is valid in Device mode and only when the VBUSVLDEXTSEL signal is set to 1. VBUSVLDEXT indicates whether the VBUS signal on the USB cable is valid. In addition, BUSVLDEXT enables the pullup resistor on the D+ line. 1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled. 1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled.

GRF_UOC2_CON3

Address: Operational Base + offset (0x0354)

UOC2 control register 3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	usbhost1_scaledown_mode USB HOST1 scale down mode control
13	RW	0x0	usbhost1_utmiotg_idpullup USB HOST1 idpullup bit control
12	RW	0x1	usbhost1_utmiotg_dppulldown USB HOST1 dppulldown bit control
11	RW	0x1	usbhost1_utmiotg_dmpulldown USB HOST1 dmpulldown bit control
10	RW	0x1	usbhost1_utmiotg_drvvbus USB HOST1 drvvbus bit contrl
9:6	RO	0x0	reserved
5	RW	0x0	usbhost1_utmi_termselect USB HOST1 utmi termination select 1'b1: full speed terminations are enabled 1'b0: high speed terminations are enabled
4:3	RW	0x0	usbhost1_utmi_xcvrselect USB HOST1 utmi transceiver select 2'b11: sends an LS packet on an FS bus or receives an LS packet 2'b10: LS transceiver 2'b01: FS transceiver 2'b00: HS transceiver

Bit	Attr	Reset Value	Description
2:1	RW	0x0	usbhost1_utmi_opmode USB HOST1 utmi operation mode This controller bus selects the UTMI+ operation mode 2'b11: normal operation without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encoding 2'b01: no-driving 2'b00: normal
0	RW	0x1	usbhost1_utmi_suspend_n USB HOST1 suspend mode enable 1'b1: normal operation mode 1'b0: suspend mode

GRF_UOC3_CON0
Address: Operational Base + offset (0x0358)
UOC3 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	hsicphy_soft_con_sel HSIC PHY software control enale
13	RW	0x1	hsicphy_txbitstuffenh HSIC high byte transmit bit-stuffing enable this controller signal controls biy stuffing on DATAIN[15:8] when OPMODE[1:0]=2'b11 1'b1: bit stuffing is enabled 1'b0: bit stuffing is disabled

Bit	Attr	Reset Value	Description
12	RW	0x1	hsicphy_txbitstuffen HSIC low byte transmit bit-stuffing enable this controller signal controls biy stuffing on DATAIN[7:0] when OPMODE[1:0]=2'b11 1'b1: bit stuffing is enabled 1'b0: bit stuffing is disabled
11	RW	0x0	hsichhy_siddq HSIC SIDDQ test enable 1'b1: the analog blocks are power down 1'b0: the analog blocks are power up
10	RW	0x0	hsicphy_port_reset HSIC per-port reset when asserted, this customer-specific signal reset the corresponding prot's transmit and receive logic without disabling the clocks within the HSIC PHY 1'b1: the transmit and receive FSMs are reset 1'b0: tjhe transmit and receive FSMs are operational
9:6	RW	0x3	hsicphy_txsrtune drive slew rate adjustment 4'b1111: +20% 4'b0111: +10% 4'b0011: design default 4'b0001: -10% 4'b0000: -20%
5:4	RW	0x2	hsicphy_txrpdtune HSIC driver pull-down impedance adjustment 2'b11: -5% 2'b10: design default 2'b01: +5% 2'b00: +11%
3:2	RW	0x2	hsicphy_txrputune HSIC driver pull-up impedance adjustment 2'b11: -5% 2'b10: design default 2'b01: +5% 2'b00: +11%
1	RW	0x1	hsicphy_dmpulldown HSIC bus keepers resistor enable This control signal selects the HSIC PHY to operate as a host or deivce.

Bit	Attr	Reset Value	Description
0	RW	0x1	hsicphy_dppulldown HSIC bus keepers resistor enable This control signal detects that the HSIC PHY is being used as a host.

GRF_UOC3_CON1
Address: Operational Base + offset (0x035c)
UOC3 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4	RW	0x0	hsic_utmi_xcvrselect HSIC PHY transceiver select 1'b1: transceiver is in suspend, resume or connect mode 1'b0: transceiver is in HS mode
3:2	RW	0x0	hsic_utmi_opmode HSIC PHY operation mode 2'b11: normal mode without SYNC or EOP generation 2'b10: disable bit stuffing and NRZI encodeing 2'b01: Non-driving 2'b00: normal
1	RW	0x1	hsic_utmi_suspend_n HSIC PHY suspend mode enable Asserting this signal places the HSIC PHY in suspend mode. 1'b1: normal mode 1'b0: suspend mode

Bit	Attr	Reset Value	Description
0	RW	0x1	hsic_utmi_sleep_n HSIC PHY sleep mode enable Asserting this signal places the HSIC PHY in sleep mode. 1'b1: normal mode 1'b0: sleep mode

GRF_UOC4_CON0
Address: Operational Base + offset (0x0360)
UOC4 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	drvvbus_out_sel0 USB PHY drv vbus output select 0 2'b00: USB OTG drv vbus 2'b01: USB HOST0 drv vbus 2'b1x: USB HOST1 drv vbus
13:12	RW	0x1	drvvbus_out_sel1 USB PHY drv vbus output select 1 2'b00: USB OTG drv vbus 2'b01: USB HOST0 drv vbus 2'b1x: USB HOST1 drv vbus
11:10	RO	0x0	reserved
9	RW	0x0	hsic_app_prt_ovrcur HSIC app_prt_ovrcur bit control
8	RW	0x0	hsic_autoppd_on_overcur HSIC autoppd_on_overcur bit control
7	RW	0x1	hsic_word_if HSIC word_if bit control
6	RW	0x0	hsic_sim_mode HSIC sim_mode bit control

Bit	Attr	Reset Value	Description
5	RW	0x0	hsic_incrx_en HSIC incrx_en bit control
4	RW	0x0	hsic_incr8_en HSIC incr8_en bit control
3	RW	0x0	hsic_incr4_en HSIC incr4_en bit control
2	RW	0x0	hsic_incr16_en HSIC incr16_en bit control
1	RW	0x0	hsic_hubsetup_min HSIC hubsetup_min bit control
0	RW	0x0	hsic_app_start_clk HSIC app_start_clk bit control

GRF_UOC4_CON1
Address: Operational Base + offset (0x0364)
UOC4 control register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:6	RW	0x20	hsic_fladj_val_common HSIC fladj_val_common bit control
5:0	RW	0x20	hsic_fladj HSIC fladj bit control

GRF_PVTM_CON0
Address: Operational Base + offset (0x0368)
PVT monitor control register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x0	pvtm_gpu_osc_en pd_gpu PVT monitor oscilator enable 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_gpu_start pd_gpu PVT monitor start control
7:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en pd_core PVT monitor oscilator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start pd_core PVT monitor start control

GRF_PVTM_CON1
Address: Operational Base + offset (0x036c)
PVT monitor control register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_core_cal_cnt pd_core pvtm calculator counter

GRF_PVTM_CON2
Address: Operational Base + offset (0x0370)
PVT monitor control register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_gpu_cal_cnt pd_gpu pvtm calculator counter

GRF_PVTM_STATUS0

Address: Operational Base + offset (0x0374)
PVT monitor status register 0

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_freq_done pd_core pvtm frequency calculate done stutus
0	RW	0x0	pvtm_gpu_freq_done pd_gpu pvtm frequency calculate done stutus

GRF_PVTM_STATUS1
Address: Operational Base + offset (0x0378)
PVT monitor status register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_freq_cnt pd_core pvtm frequency count

GRF_PVTM_STATUS2
Address: Operational Base + offset (0x037c)
PVT monitor status register 2

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pvtm_gpu_freq_cnt pd_gpu pvtm frequency count

GRF_IO_VSEL
Address: Operational Base + offset (0x0380)
IO voltage select

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	gpio1830_v18sel GPIO1830 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
8	RW	0x0	gpio30_v18sel GPIO30 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
7	RW	0x0	sdcard_v18sel SDCARD IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
6	RW	0x0	audio_v18sel AUDIO IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
5	RW	0x0	bb_v18sel BB IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
4	RW	0x0	wifi_v18sel WIFI IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
3	RW	0x0	flash1_v18sel FLASH1 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
2	RW	0x1	flash0_v18sel FLASH0 IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
1	RW	0x0	dvp_v18sel DVP IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V
0	RW	0x0	lcdc_v18sel LCDC IO domain 1.8V voltage selection 1'b0: 3.3V 1'b1: 1.8V

GRF_SARADC_TESTBIT
Address: Operational Base + offset (0x0384)
SARADC Test bit register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	saradc_testbit SARADC test bit

GRF_TSADC_TESTBIT_L
Address: Operational Base + offset (0x0388)
TSADC Test bit low register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	tsadc_testbit_l Low 16bits of TSADC test bit

GRF_TSADC_TESTBIT_H
Address: Operational Base + offset (0x038c)
TSADC Test bit high register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	tsadc_testbit_h High 16bits of TSADC test bit

GRF_OS_REG0
Address: Operational Base + offset (0x0390)
OS register 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg0 OS register 0

GRF_OS_REG1
Address: Operational Base + offset (0x0394)
OS register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg1 OS register 1

GRF_OS_REG2
Address: Operational Base + offset (0x0398)
OS register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg2 OS register 2

GRF_OS_REG3
Address: Operational Base + offset (0x039c)
OS register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg3 OS register 3

GRF_SOC_CON15
Address: Operational Base + offset (0x03a4)
SoC control register 15

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	grf_dclk1_lvds_inv_sel Invertion of VOP_LIT dclk for LVDS selection 1'b1: invert 1'b0: not invert
14	RW	0x0	grf_dclk1_lvds_div2_sel 2 divide frequency of VOP_LIT dclk for LVDS selection 1'b1: 2 divide frequency 1'b0: no divide frequency
13	RW	0x0	grf_dclk0_lvds_inv_sel Invertion of VOP_BIG dclk for LVDS selection 1'b1: invert 1'b0: not invert
12	RW	0x0	grf_dclk0_lvds_div2_sel 2 divide frequency of VOP_BIG dclk for LVDS selection 1'b1: 2 divide frequency 1'b0: no divide frequency
11	RO	0x0	reserved
10:8	RW	0x0	dphy_tx0_turnrequest MIPI DPHY TX0 turn around request Every bit for one lane, bit2 is for lane3, bit2 is for lane2, bit0 is for lane1.

Bit	Attr	Reset Value	Description
7:4	RW	0x0	dphy_tx1rx1_turnrequest MIPI DPHY TX1RX1 turn around request Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
3:0	RW	0x0	dphy_rx0_turnrequest MIPI DPHY RX0 turn around request Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.

GRF_SOC_CON16
Address: Operational Base + offset (0x03a8)
SoC control register 16

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1	RW	0x0	grf_con_dsi1_dpiupdatecfg DSI host1 dpiupdatecfg bit control
0	RW	0x0	grf_con_dsi0_dpiupdatecfg DSI host0 dpiupdatecfg bit control