SONY

Diagonal 6.43 mm (Type 1/2.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX415-AAQR-C

STARVIS

Description

The IMX415-AAQR-C is a diagonal 6.4 mm (Type 1/2.8) CMOS active pixel type solid-state image sensor with a square pixel array and 8.46 M effective pixels. This chip operates with analog 2.9 V, digital 1.1 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Input frequency: 24 MHz / 27 MHz / 37.125 MHz / 72 MHz / 74.25 MHz
- ◆ Number of recommended recording pixels: 3840 (H) × 2160 (V) approx. 8.29M pixel
- ◆ Readout mode
  - All-pixel scan mode
  - Horizontal / Vertical 2/2-line binning mode
  - Window cropping mode
  - Horizontal / Vertical direction - Normal / Inverted readout mode
- ◆ Readout rate
  - Maximum frame rate in
  - All-pixel scan mode: 12 bit: 60.3 frame/s, 10 bit: 90.9 frame/s
- ◆ High dynamic range (HDR) function
  - Multiple exposure HDR
  - Digital overlap HDR
- ◆ Synchronizing sensors function
- ◆ Variable-speed shutter function (resolution 1H units)
- ◆ CDS / PGA function
  - 0 dB to 30 dB : Analog Gain 30 dB (step pitch 0.3 dB)
  - 30.3 dB to 72 dB : Analog Gain 30 dB + Digital Gain 0.3 dB to 42 dB (step pitch 0.3 dB)
- ◆ Supports I/O
  - CSI-2 serial data output (2 Lane / 4 Lane), RAW10 / RAW12 output
- ◆ Recommended exit pupil distance: –30 mm to –∞

E19504

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 6.4 mm (Type 1/2.8) approx. 8.40 M pixels, All pixels
- ◆ Total number of pixels
  3864 (H) × 2228 (V) approx. 8.60 M pixels
- ◆ Number of effective pixels
  3864 (H) × 2192 (V) approx. 8.46 M pixels
- ◆ Number of active pixels
  3864 (H) × 2176 (V) approx. 8.40 M pixels
- ◆ Number of recommended recording pixels
  3840 (H) × 2160 (V) approx. 8.29 M pixels
- ◆ Unit cell size
  1.45 µm (H) × 1.45 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 36 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 1 pixels, rear 1 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog: 2.9 V)	AV_{DD}	-0.3	3.3	V	
Supply voltage (interface: 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital: 1.1 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	
Storage temperature	Tstg	-40	85	˚C	

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog: 2.9 V)	AV_{DD1}	2.80	2.90	3.00	V
Supply voltage (interface: 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital: 1.1 V)	DV_{DD1}	1.00	1.10	1.20	V
Performance guarantee temperature	Tspec	-10	—	60	˚C

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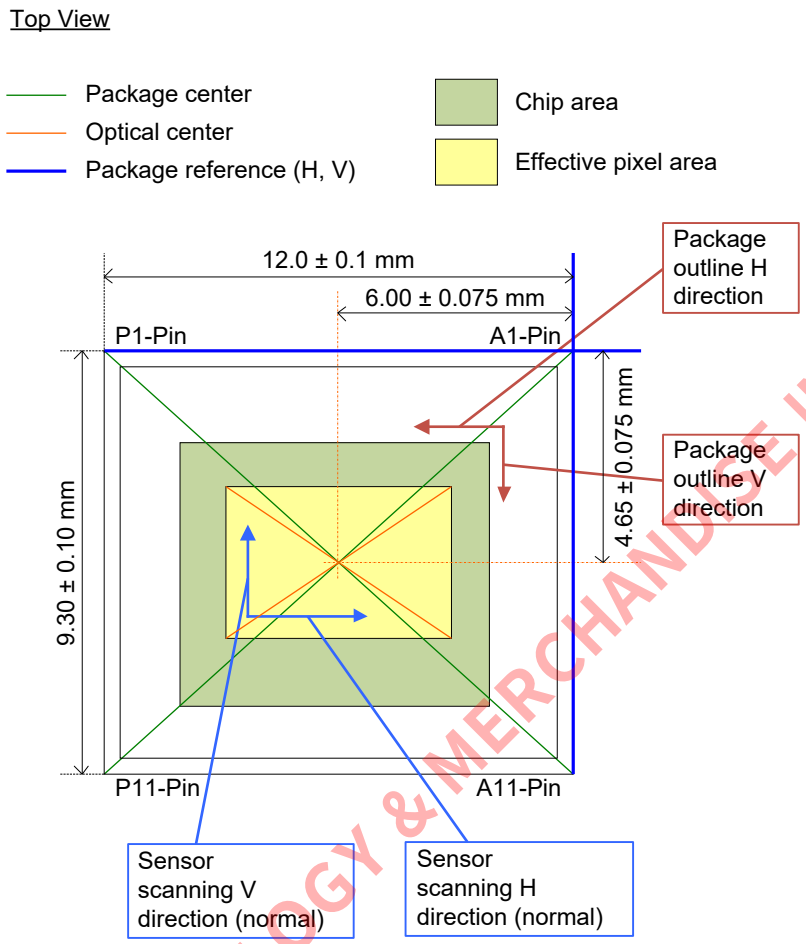
General-0.0.9

Contents

Description ... 1
Features ... 1
Device Structure ... 2
Absolute Maximum Ratings ... 3
Application Conditions ... 3
USE RESTRICTION NOTICE ... 4
Optical Center ... 7
Pixel Arrangement ... 8
Block Diagram and Pin Configuration ... 9
Pin Description ... 11
Electrical Characteristics ... 14
  DC Characteristics ... 14
  Current Consumption ... 15
  AC Characteristics ... 16
    Master Clock Waveform (INCK) ... 16
    System Clear (XCLR) ... 17
    XVS / XHS Input Characteristics in Slave Mode (Register XMASTER = 1) ... 18
    XVS / XHS Input Characteristics in Master Mode (Register XMASTER = 0) ... 18
    Serial Communication ... 19
I/O Equivalent Circuit Diagram ... 21
Spectral Sensitivity Characteristics ... 22
Image Sensor Characteristics ... 23
Image Sensor Characteristics Measurement Method ... 24
  Measurement Conditions ... 24
  Color Coding of Physical Pixel Array ... 24
  Definition of standard imaging conditions ... 24
  Measurement Method ... 25
Setting Registers Using Serial Communication ... 26
  Description of Setting Registers (I^2C) ... 26
  Register Communication Timing (I^2C) ... 27
  Communication Protocol ... 28
  Register Write and Read (I^2C) ... 29
    Single Read from Random Location ... 29
    Single Read from Current Location ... 29
    Sequential Read Starting from Random Location ... 30
    Sequential Read Starting from Current Location ... 30
    Single Write to Random Location ... 31
    Sequential Write Starting from Random Location ... 31
Register Map ... 32
Readout Drive mode ... 48
  Operating mode ... 48
  Image Data Output Format (CSI-2 output) ... 50
    Frame Format ... 50
    Frame Structure ... 50
    Embedded Data Line ... 51
  Image Data Output Format ... 53
    All-pixel mode ... 54
    Horizontal/Vertical 2/2-line binning mode ... 57
    Window Cropping Mode ... 62
Description of Various Function ... 64
  Standby Mode ... 64
  Slave Mode and Master Mode ... 65
  Gain Adjustment Function ... 67
  Black Level Adjustment Function ... 68
  Normal Operation and Inverted Operation ... 69
  Shutter and Integration Time Settings ... 70
    Example of Integration Time Setting ... 70
  Normal Exposure Operation (Controlling the Integration Time in 1H Units) ... 71

Long Exposure Operation (Control by Expanding the Number of Lines per Frame) ... 72
Example of Integration Time Settings ... 73
Signal Output ... 74
CSI-2 output ... 74
MIPI Transmitter ... 76
Number of Internal A/D Conversion Bits Setting ... 77
Output Signal Range ... 77
INCK Setting ... 78
Register Hold Setting ... 81
Mode Transitions ... 82
Other Function ... 83
Power-on and Power-off Sequence ... 84
Power-on sequence ... 84
Slew Rate Limitation of Power-on Sequence ... 85
Power-off sequence ... 86
Sensor Setting Flow ... 87
Setting Flow in Sensor Slave Mode ... 87
Setting Flow in Sensor Master Mode ... 88
Peripheral Circuit ... 89
Spot Pixel Specifications ... 90
Zone Definition ... 90
Notice on White Pixels Specifications ... 91
Measurement Method for Spot Pixels ... 92
Spot Pixel Pattern Specification ... 93
Marking ... 94
Notes On Handling ... 95
Package Outline ... 97
List of Trademark Logos and Definition Statements ... 98

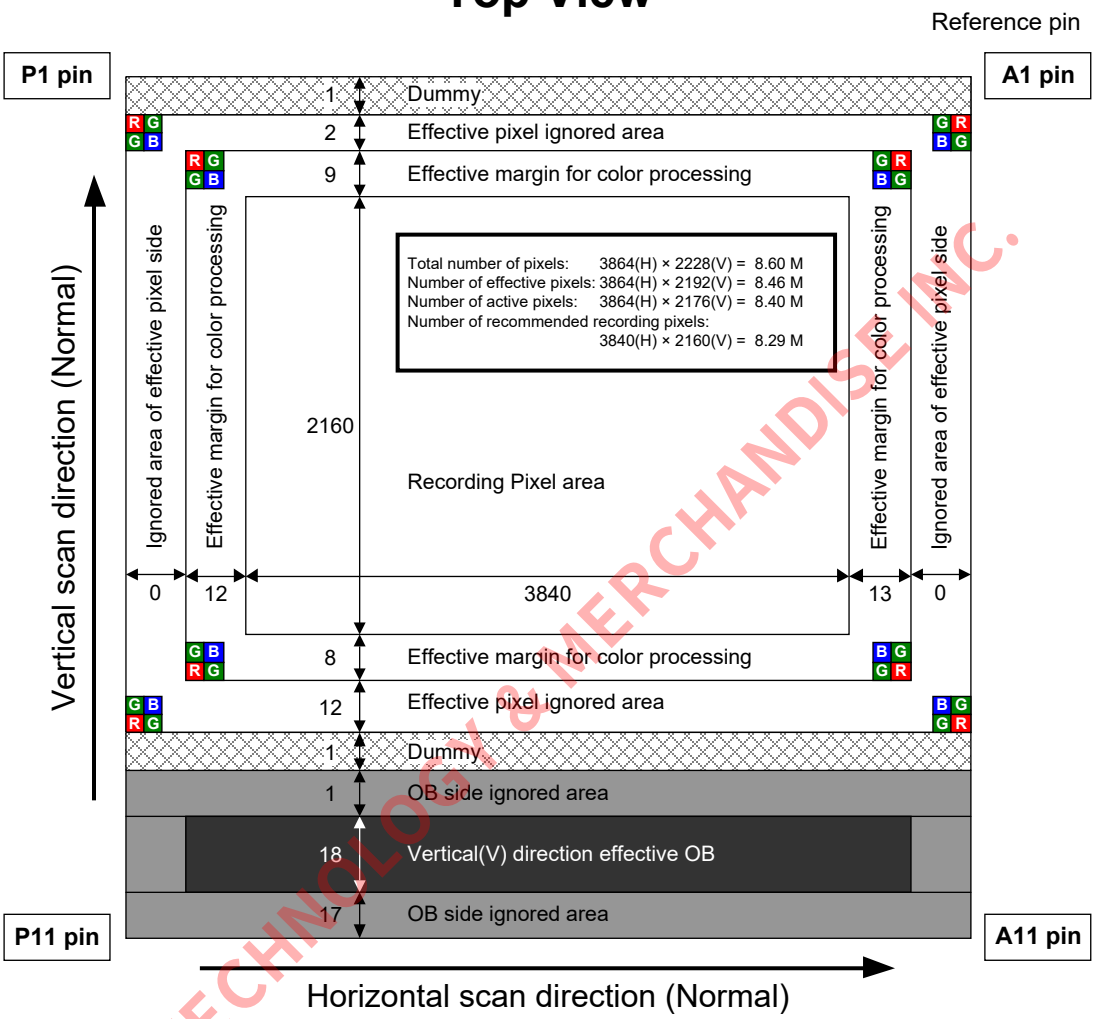
Optical Center



Optical Center

Pixel Arrangement

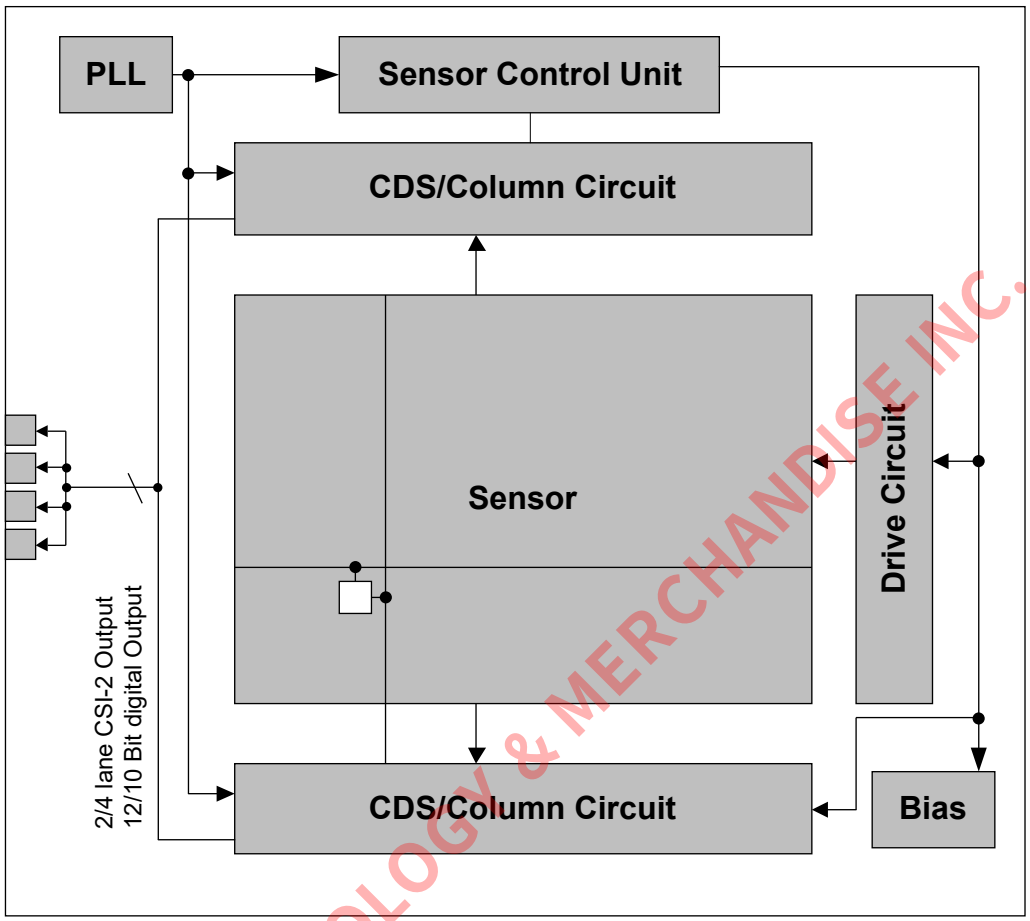
Top View



* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.
Dummy is the effective pixels to ignore the data content.
The last Effective line and column are not read-out.

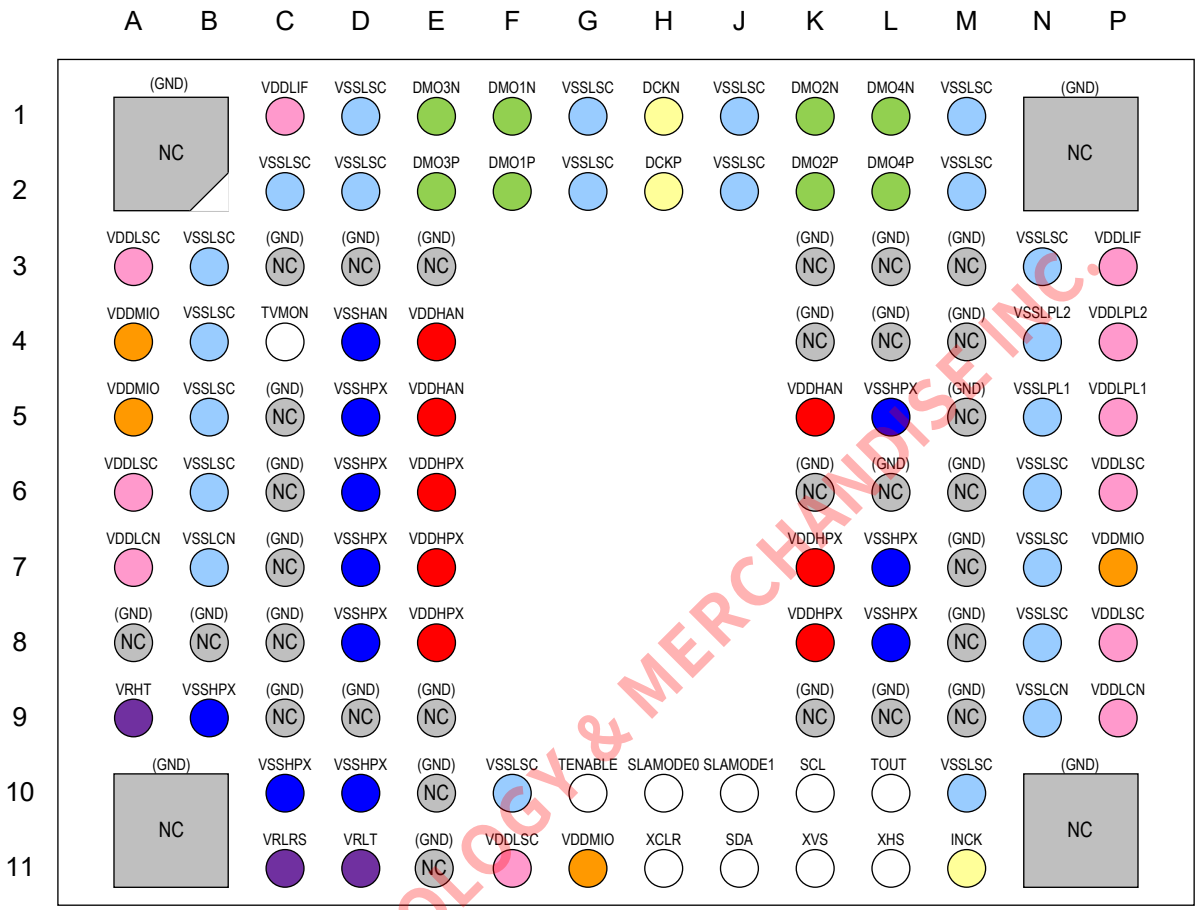
Pixel Arrangement

Block Diagram and Pin Configuration



Block Diagram

Bottom View



Power Supply (2.9V)
Power Supply (1.8V)
Power Supply (1.1V)
Capacitor connection
GND (2.9V)
GND (1.8V / 1.1V)
Clock
Data output

*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

Pin Description

No.	Pin No	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connectable
2	A3	Power	D	VDDLSC	1.1 V power supply
3	A4	Power	D	VDDMIO	1.8 V power supply
4	A5	Power	D	VDDMIO	1.8 V power supply
5	A6	Power	D	VDDLSC	1.1 V power supply
6	A7	Power	D	VDDLCN	1.1 V power supply
7	A8	—	—	N.C.	GND connectable
8	A9	O	A	VRHT	Capacitor connection
9	A11	—	—	N.C.	GND connectable
10	B3	GND	D	VSSLSC	1.1V GND
11	B4	GND	D	VSSLSC	1.1V GND
12	B5	GND	D	VSSLSC	1.1V GND
13	B6	GND	D	VSSLSC	1.1V GND
14	B7	GND	D	VSSLCN	1.1V GND
15	B8	—	—	N.C.	GND connectable
16	B9	GND	A	VSSHPX	2.9V GND
17	C1	Power	D	VDDLIF	1.1 V power supply
18	C2	GND	D	VSSLSC	1.1V GND
19	C3	—	—	N.C.	GND connectable
20	C4	O	A	TVMON	TEST output pin, OPEN
21	C5	—	—	N.C.	GND connectable
22	C6	—	—	N.C.	GND connectable
23	C7	—	—	N.C.	GND connectable
24	C8	—	—	N.C.	GND connectable
25	C9	—	—	N.C.	GND connectable
26	C10	GND	A	VSSHPX	2.9V GND
27	C11	O	A	VRLRS	Capacitor connection
28	D1	GND	D	VSSLSC	1.1V GND
29	D2	GND	D	VSSLSC	1.1V GND
30	D3	—	—	N.C.	GND connectable
31	D4	GND	A	VSSHAN	2.9V GND
32	D5	GND	A	VSSHPX	2.9V GND
33	D6	GND	A	VSSHPX	2.9V GND
34	D7	GND	A	VSSHPX	2.9V GND
35	D8	GND	A	VSSHPX	2.9V GND
36	D9	—	—	N.C.	GND connectable
37	D10	GND	A	VSSHPX	2.9V GND
38	D11	O	A	VRLT	Capacitor connection
39	E1	O	D	DMO3N	CSI-2 output (data)
40	E2	O	D	DMO3P	CSI-2 output (data)
41	E3	—	—	N.C.	GND connectable
42	E4	Power	A	VDDHAN	2.9 V power supply
43	E5	Power	A	VDDHAN	2.9 V power supply
44	E6	Power	A	VDDHPX	2.9 V power supply
45	E7	Power	A	VDDHPX	2.9 V power supply
46	E8	Power	A	VDDHPX	2.9 V power supply

No.	Pin No	I/O	Analog / Digital	Symbol	Description
47	E9	—	—	N.C.	GND connectable
48	E10	—	—	N.C.	GND connectable
49	E11	—	—	N.C.	GND connectable
50	F1	O	D	DMO1N	CSI-2 output (data)
51	F2	O	D	DMO1P	CSI-2 output (data)
52	F10	GND	D	VSSLSC	1.1V GND
53	F11	Power	D	VDDLSC	1.1 V power supply
54	G1	GND	D	VSSLSC	1.1V GND
55	G2	GND	D	VSSLSC	1.1V GND
56	G10	I	D	TENABLE	Test enable, OPEN
57	G11	Power	D	VDDMIO	1.8 V power supply
58	H1	O	D	DCKN	CSI-2 output (clock)
59	H2	O	D	DCKP	CSI-2 output (clock)
60	H10	I	D	SLAMODE0	Select slave address
61	H11	I	D	XCLR	System clear
62	J1	GND	D	VSSLSC	1.1V GND
63	J2	GND	D	VSSLSC	1.1V GND
64	J10	I	D	SLAMODE1	Select slave address
65	J11	I/O	D	SDA	Serial data communication
66	K1	O	D	DMO2N	CSI-2 output (data)
67	K2	O	D	DMO2P	CSI-2 output (data)
68	K3	—	—	N.C.	GND connectable
69	K4	—	—	N.C.	GND connectable
70	K5	Power	A	VDDHAN	2.9 V power supply
71	K6	—	—	N.C.	GND connectable
72	K7	Power	A	VDDHPX	2.9 V power supply
73	K8	Power	A	VDDHPX	2.9 V power supply
74	K9	—	—	N.C.	GND connectable
75	K10	I/O	D	SCL	Serial clock input
76	K11	I/O	D	XVS	Vertical sync signal
77	L1	O	D	DMO4N	CSI-2 output (data)
78	L2	O	D	DMO4P	CSI-2 output (data)
79	L3	—	—	N.C.	GND connectable
80	L4	—	—	N.C.	GND connectable
81	L5	GND	A	VSSHPX	2.9V GND
82	L6	—	—	N.C.	GND connectable
83	L7	GND	A	VSSHPX	2.9V GND
84	L8	GND	A	VSSHPX	2.9V GND
85	L9	—	—	N.C.	GND connectable
86	L10	I/O	D	TOUT	Digital TEST output pin, OPEN
87	L11	I/O	D	XHS	Horizontal sync signal
88	M1	GND	D	VSSLSC	1.1V GND
89	M2	GND	D	VSSLSC	1.1V GND
90	M3	—	—	N.C.	GND connectable
91	M4	—	—	N.C.	GND connectable
92	M5	—	—	N.C.	GND connectable
93	M6	—	—	N.C.	GND connectable
94	M7	—	—	N.C.	GND connectable
95	M8	—	—	N.C.	GND connectable

No.	Pin No	I/O	Analog / Digital	Symbol	Description
96	M9	—	—	N.C.	GND connectable
97	M10	GND	D	VSSLSC	1.1V GND
98	M11	I	D	INCK	Master clock input
99	N3	GND	D	VSSLSC	1.1V GND
100	N4	GND	A	VSSLPL2	1.1V GND
101	N5	GND	A	VSSLPL1	1.1V GND
102	N6	GND	D	VSSLSC	1.1V GND
103	N7	GND	D	VSSLSC	1.1V GND
104	N8	GND	D	VSSLSC	1.1V GND
105	N9	GND	D	VSSLCN	1.1V GND
106	P1	—	—	N.C.	GND connectable
107	P3	Power	D	VDDLIF	1.1 V power supply
108	P4	Power	A	VDDLPL2	1.1 V power supply
109	P5	Power	A	VDDLPL1	1.1 V power supply
110	P6	Power	D	VDDLSC	1.1 V power supply
111	P7	Power	D	VDDMIO	1.8 V power supply
112	P8	Power	D	VDDLSC	1.1 V power supply
113	P9	Power	D	VDDLCN	1.1 V power supply
114	P11	—	—	N.C.	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}		2.80	2.90	3.00	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.00	1.10	1.20	V
Digital input voltage		XHS XVS XCLR INCK SLAMODE0 SLAMODE1	VIH	XVS / XHS Slave Mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS TOUT	VOH	XVS / XHS Master Mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

Current Consumption

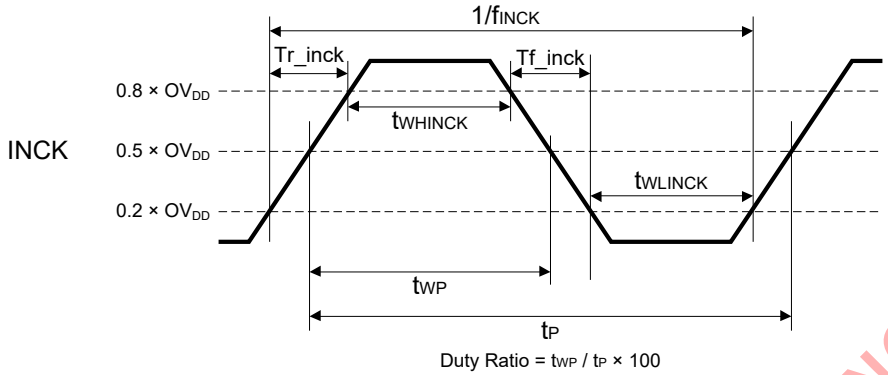
Item	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 / 4 Lane, 2079 Mbps 12 bit, 60 frame/s All-pixel mode	I_{AVDD}	128	156	mA
	I_{OVDD}	3	3	mA
	I_{DVDD}	187	250	mA
Standby current	I_{AVDD_STB}	–	0.2	mA
	I_{OVDD_STB}	–	0.2	mA
	I_{DVDD_STB}	–	15.1	mA

Operating current: (Typ.) Supply voltage 2.9 V / 1.8 V / 1.1 V, Tj = 25 ˚C, standard luminous intensity.
(Max.) Supply voltage 3.0 V / 1.9 V / 1.2 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage 3.0 V / 1.9 V / 1.2 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

AC Characteristics

Master Clock Waveform (INCK)

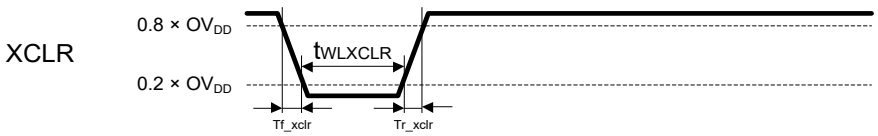


INCK 24MHz, 27MHz, 37125MHz, 72MHz, 74.25MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 24 MHz, 27 MHz, 37.125 MHz, 72 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

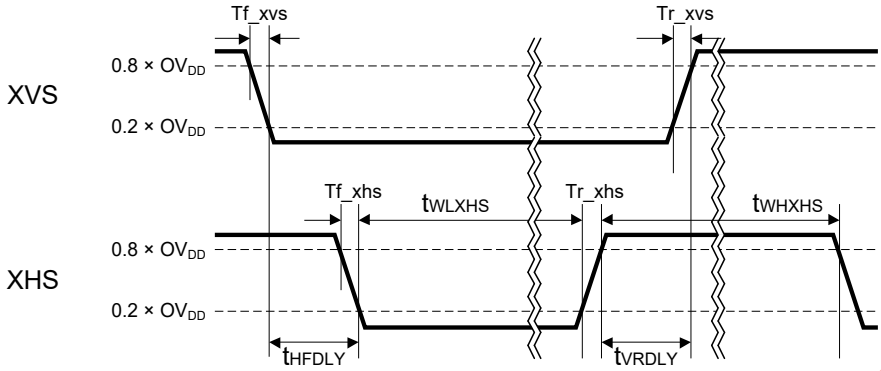
* The INCK fluctuation affects the frame rate.

System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	4 / f_{INCK}	—	—	ns	
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Slave Mode (Register XMASTER = 1)



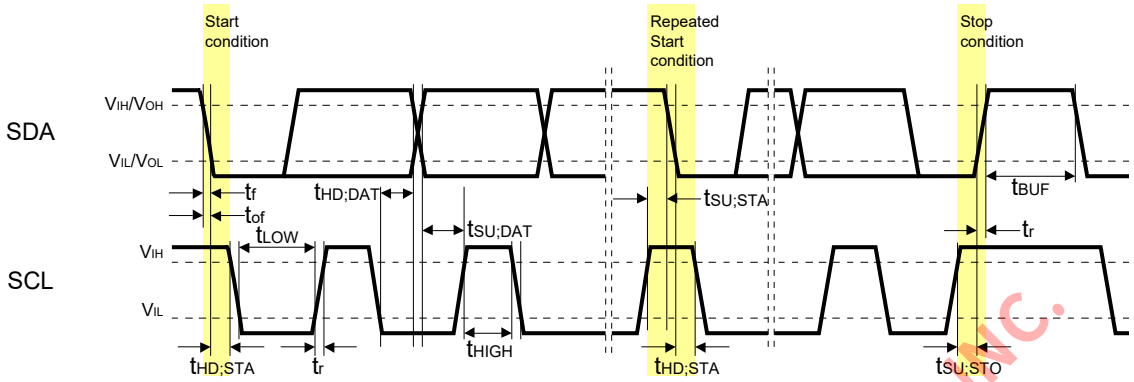
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Master Mode (Register XMASTER = 0)

* XVS and XHS cannot be used for the sync signal to pixels.
  Be sure to detect sync code to detect the start of effective pixels in 1 line.
  For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

Serial Communication

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	–0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Input current	Ii	–10	—	10	μA	0.1 × OV_{DD} to 0.9 × OV_{DD}
Input Capacitance for SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics (Standard-mode, Fast-mode)

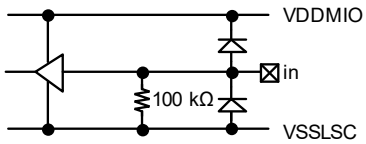
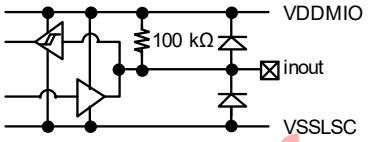
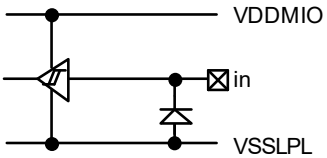
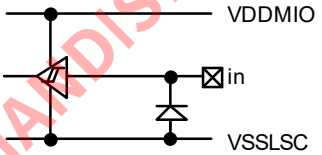
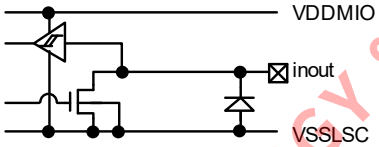
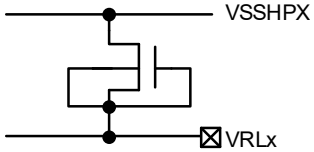
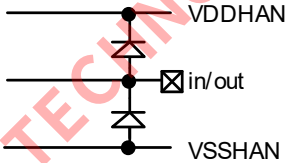
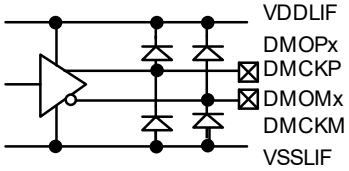
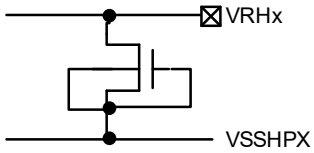
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	400	kHz	
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs	
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs	
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs	
Data set-up time	$t_{SU;DAT}$	100	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	300	ns	
Fall time of both SDA and SCL signals	t_f	—	—	300	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs	
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs	
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I²C AC Characteristics (Fast-mode Plus)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	1000	kHz	INCK ≥ 16 MHz
Hold time (Start Condition)	$t_{HD;STA}$	0.26	—	—	µs	
Low period of the SCL clock	t_{LOW}	0.5	—	—	µs	
High period of the SCL clock	t_{HIGH}	0.26	—	—	µs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.26	—	—	µs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs	
Data set-up time	$t_{SU;DAT}$	50	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	120	ns	
Fall time of both SDA and SCL signals	t_f	—	—	120	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.26	—	—	µs	
Bus free time between a STOP and START Condition	t_{BUF}	0.5	—	—	µs	
Output fall time	tof	—	—	120	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS TOUT	
INCK		XCLR SLAMODE1 SLAMODE2	
SDA SCL		VRLRS VRLT	
TVMON		DMOPx DMOMx DMCKP DMCKM	
VRHT			

Spectral Sensitivity Characteristics

(Characteristics in the wafer status)

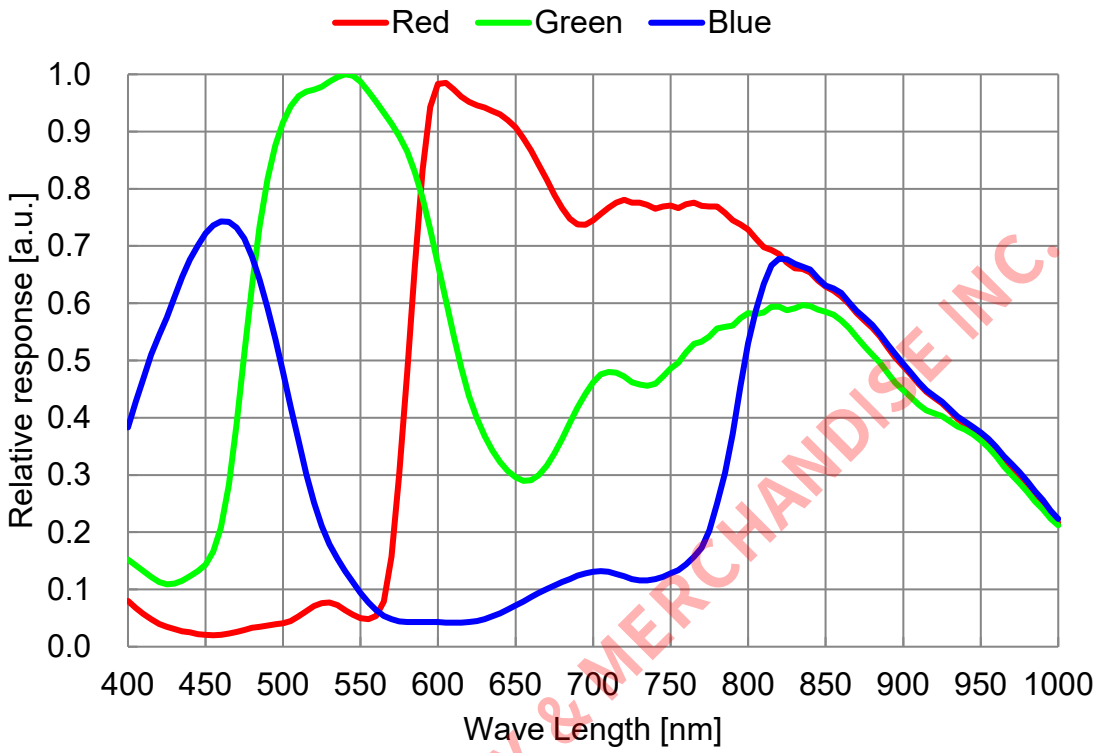


Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, All-pixel mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	1740 (255)	2048 (300)	—	Digit (mV)	1	1/30 s storage 12 bit converted value
Sensitivity ratio	R / G	RG	0.42	—	0.58	—	2	—
	B / G	BG	0.26	—	0.44	—		
Saturation signal		Vsat	3895 (570)	—	—	Digit (mV)	3	12 bit converted value
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	μV	5	12 bit converted value
Dark signal		Vdt	—	—	0.89 (0.13)	Digit (mV)	6	1/30 s storage 12 bit converted value
Dark signal shading		ΔVdt	—	—	0.89 (0.13)	Digit (mV)	7	1/30 s storage 12 bit converted value

Note) 1. Converted value into mV using 1Digit = 0.1465 mV for 12-bit output and 1Digit = 0.5865 mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.
3. The characteristics above apply to effective pixel area.

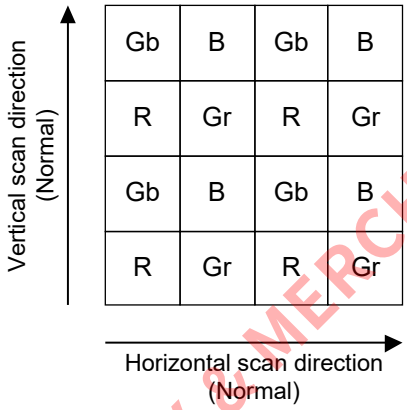
Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.



Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100 / 30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 300 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 300 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 300 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 300 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates each average output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [µV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 6, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

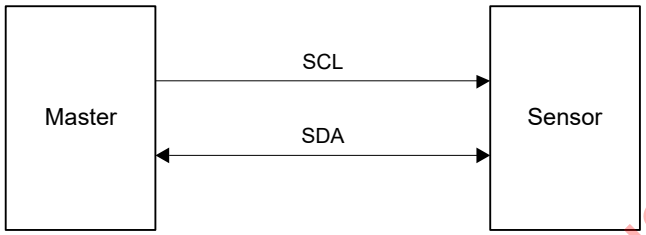
   ΔVdt = Vdmax – Vdmin [mV]

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I²C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I²C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE0 and SLAMODE1 pins, SLAVE address can be changed.



Pin connection of serial communication

SLAVE Address

SLAMODE1 pin	SLAMODE0 pin	MSB							LSB
Low	Low	0	0	1	1	0	1	0	R / W
Low	High	0	0	1	0	0	0	0	R / W
High	Low	0	1	1	0	1	1	0	R / W
High	High	0	1	1	0	1	1	1	R / W

* R/W is data direction bit

R / W

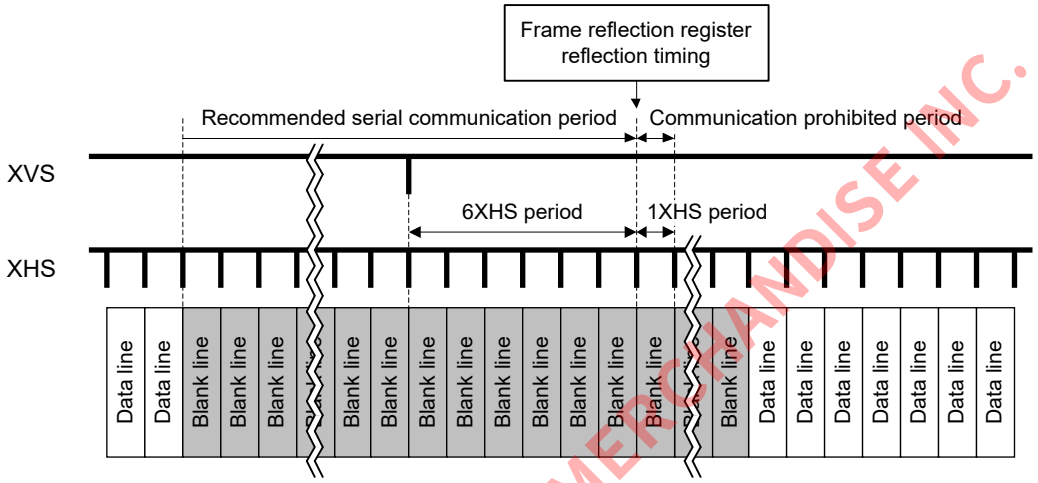
R / W bit	Data direction
0	Write (Master to Sensor)
1	Read (Sensor to Master)

I²C pin description

Symbol	Pin No.	Remarks
SCL	K10	I²C serial clock input
SDA	J11	I²C serial data communication

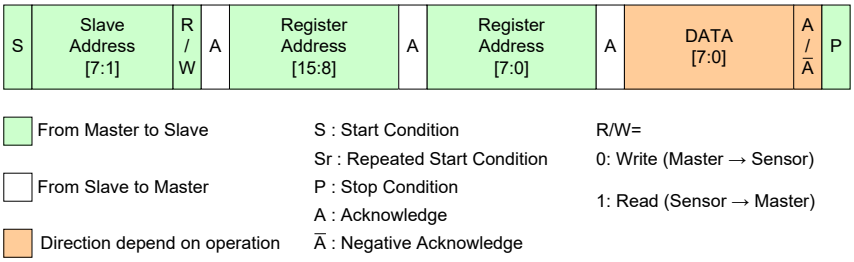
Register Communication Timing (I²C)

In I²C communication system, communication can be performed excluding the prohibited 1H period as described in the below figure.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by “Frame reflection register reflection timing”.
For the registers marked “I” in the item of Reflection timing, the settings are reflected when the communication is performed.
Using REGHOLD function is recommended for register setting using I²C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



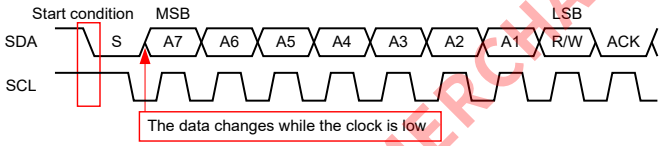
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

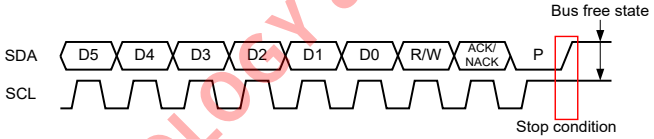


Communication Protocol

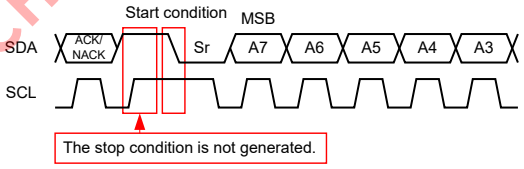
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

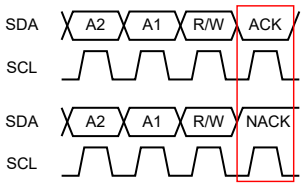


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



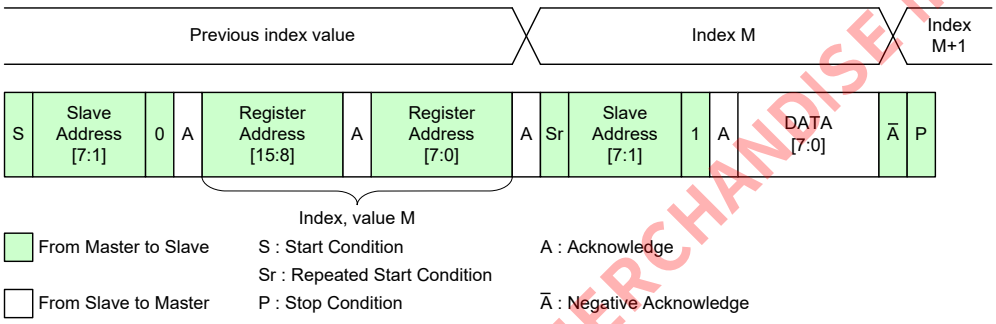
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

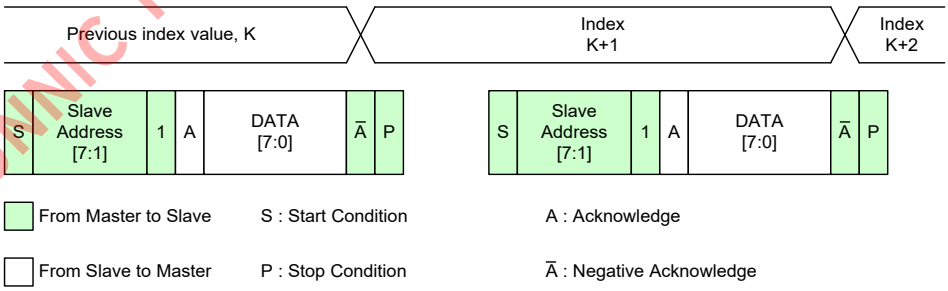
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose, it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

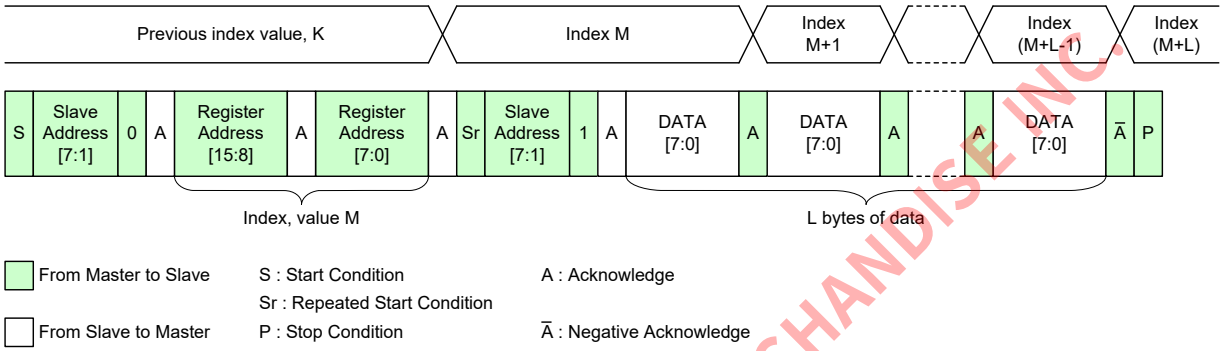
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

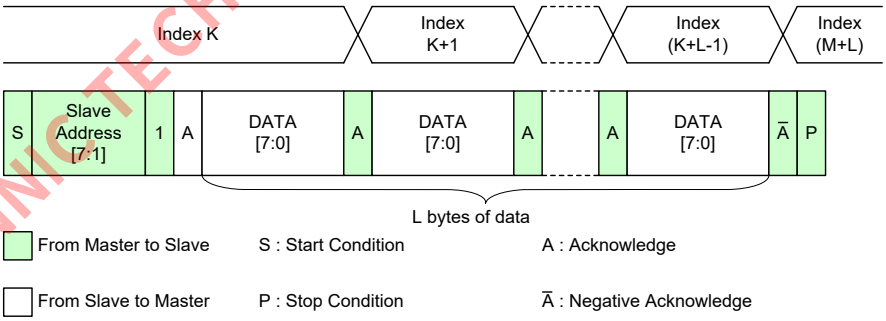
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition.
Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

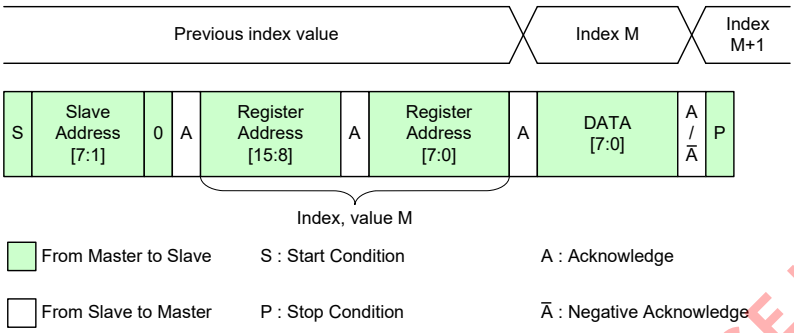
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA.
This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

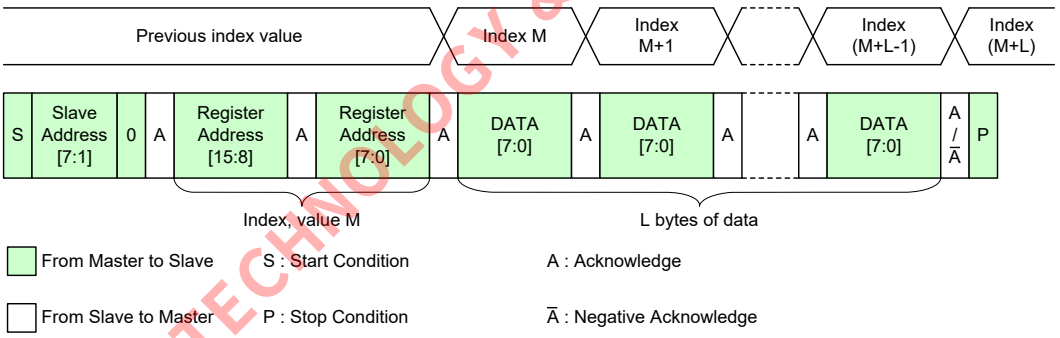
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 4352 bytes (256 × 17) of registers, composed of registers with LSB addresses 00h to FFh that correspond to MSB address 30h to 40h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 4352 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers with Serial Communication”.

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for LSB address; 3000h to 40FFh.

* For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.
** In Gain setting only, it is reflected on the next frame which was settings.
*** Setting except for the setting values described in the description column is prohibited.

(1) Registers corresponding to address = 30**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	I
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3003h	0	XMASTER	Select Master /Slave mode 0: Master mode 1: Slave mode	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3008h	0	BCWAIT_TIME [9:0]	LSB	0FFh	FFh	S
	1					
	2					
	3					
	4		The value is set according to INCK. Refer to “INCK setting”			
	5					
	6					
	7					
3009h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
300Ah	0	CPWAIT_TIME [9:0]	LSB	0B6h	B6h	S
	1					
	2					
	3					
	4		The value is set according to INCK. Refer to “INCK setting”			
	5					
	6					
	7					
300Bh	0				A0h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “1h”	1h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “1h”	1h		—
301Ch	0	WINMODE [3:0]	Window mode setting 0: All-pixel mode, Horizontal/Vertical 2/2-line binning 4: Window cropping mode	0h	00h	V
	1					
	2					
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3020h	0	HADD	Mode setting 0h: All-pixel mode 1h: Horizontal 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3021h	0	VADD	Mode setting 0h: All-pixel mode 1h: Vertical 2 binning	0h	00h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3022h	0 1	ADDMODE [1:0]	Mode setting 0h: All-pixel mode 1h: Horizontal/Vertical 2/2-line binning	0h	00h	S
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3024h	0	VMAX [19:0]	LSB	008CAh	CAh	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		When sensor master mode vertical span setting. For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.			
3025h	0				08h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3026h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3028h	0	HMAX [15:0]	LSB	0226h	26h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		When sensor master mode horizontal span setting. For details, see the item of “Slave Mode and Master Mode” in the section of “Description of Various Functions”.			
3029h	0				02h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3030h	0	HREVERSE	Horizontal direction Readout inversion control 0: Normal 1: Inverted	0h	00h	V
	1	VREVERSE	Vertical direction Readout inversion control 0: Normal 1: Inverted	0h		V
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3031h	0 1	ADBIT [1:0]	AD conversion bits setting 0: AD 10 bit 1: AD 12 bit (11 bit + digital dither)	1h	01h	S
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3032h	0	MDBIT	Number of output bit setting 0: 10 bit 1: 12 bit	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3033h	0 1 2 3	SYS_MODE [3:0]	Output IF mode setting 0: 2376 Mbps 2: 2079 Mbps 4: 1782 Mbps 5: 891 Mbps 7: 594 Mbps 8: 1140 / 1485 Mbps 9: 720 Mbps	4h	04h	S
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3040h	0	PIX_HST [12:0]	LSB In window cropping mode Start position (Horizontal direction) Multiples of 2	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3041h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3042h	0	PIX_HWIDTH [12:0]	LSB In window cropping mode Cropping width (Horizontal direction) Multiples of 24	0F18h	18h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3043h	0				0Fh	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3044h	0	PIX_VST [12:0]	LSB In window cropping mode Start position (Vertical direction) Designated in Line ×2, Multiples of 4	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3045h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3046h	0	PIX_VWIDTH [12:0]	LSB	1120h	20h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode Cropping width (Vertical direction)			
	6					
	7		Designated in Line × 2, Multiples of 4			
3047h	0				11h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3050h	0	SHR0 [19:0]	LSB	00066h	66h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3051h	0		Storage time adjustment Designated in line units.		00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3052h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3081h	[7:0]	—	Fixed to “00h”	00h	00h	S

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3090h	0	GAIN_PCG_0 [8:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		Gain setting (0.0dB to 72.0dB / 0.3dB step)			
3091h	0		MSB		00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30C0h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to Low 2: VSYNC output	2h	2Ah	I
	1					
	2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to Low 2: HSYNC output	2h		I
	3					
	4	—	Fixed to “2h”	2h		—
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30C1h	0	XVS_DRV [1:0]	XVS pin setting 0: XVS output (Master mode) 3: HiZ (Slave mode)	3h	0Fh	S
	1					
	2	XHS_DRV [1:0]	XHS pin setting 0: XHS output (Master mode) 3: HiZ (Slave mode)	3h		S
	3					
	4	—	Fixed to “0h”	0h		—
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30CCh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XVSLNG [1:0]	XVS pulse width setting in master mode. 0: 1H 1: 2H 2: 4H 3: 8H	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30CDh	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XHSLNG [1:0]	XHS pulse width setting in master mode. 0: 16clock 1: 32clock 2: 64clock 3: 128clock	0h		I
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30D9h	0	DIG_CLP_VSTART [4:0]	The value is set according to Readout mode. 2: Horizontal / Vertical 2/2-line binning mode 6: All-pixel scan mode	06h	06h	S
	1					
	2					
	3					
	4					
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30DAh	0	DIG_CLP_VNUM [1:0]	The value is set according to Readout mode. 1: Horizontal / Vertical 2/2-line binning mode 2: All-pixel scan mode	2h	02h	S
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30E2h	0	BLKLEVEL [9:0]	LSB	032h	32h	I
	1					
	2					
	3		Black level offset value setting			
	4					
	5		10-bit readout mode: 1digit/1h			
	6		12-bit readout mode: 4digit/1h			
	7					
30E3h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

(2) Registers corresponding to address = 31**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3115h	[7:0]	INCKSEL1 [7:0]	The value is set according to INCK. Refer to “INCK setting”	00h	00h	S
3116h	[7:0]	INCKSEL2 [7:0]	The value is set according to INCK. Refer to “INCK setting”	28h	28h	S
3118h	0	INCKSEL3 [10:0]	LSB	0C0h	C0h	S
	1					
	2					
	3					
	4					
	5		The value is set according to INCK. Refer to “INCK setting”			
	6					
	7					
3119h	0				00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
311Ah	0	INCKSEL4 [10:0]	LSB	0E0h	E0h	S
	1					
	2					
	3					
	4					
	5		The value is set according to INCK. Refer to “INCK setting”			
	6					
	7					
311Bh	0				00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
311Eh	[7:0]	INCKSEL5 [7:0]	The value is set according to INCK. Refer to “INCK setting”	28h	28h	S

(3) Registers corresponding to address = 32**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
32D4h	[7:0]	—	Set to “21h”	20h	20h	S
32ECh	[7:0]	—	Set to “A1h”	A0h	A0h	S

(4) Registers corresponding to address = 34**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
3452h	[7:0]	—	Set to “7Fh”	00h	00h	S
3453h	[7:0]	—	Set to “03h”	00h	00h	S

(5) Registers corresponding to address = 35**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
358Ah	[7:0]	—	Set to “04h”	06h	06h	S
35A1h	[7:0]	—	Set to “02h”	00h	00h	S

(6) Registers corresponding to address = 36**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By Address	
36BCh	[7:0]	—	Set to “0Ch”	00h	00h	S
36CCh	[7:0]	—	Set to “53h”	FFh	FFh	S
36CDh	[7:0]	—	Set to “00h”	01h	01h	S
36CEh	[7:0]	—	Set to “3Ch”	00h	00h	S
36D0h	[7:0]	—	Set to “8Ch”	FFh	FFh	S
36D1h	[7:0]	—	Set to “00h”	01h	01h	S
36D2h	[7:0]	—	Set to “71h”	00h	00h	S
36D4h	[7:0]	—	Set to “3Ch”	00h	00h	S
36D6h	[7:0]	—	Set to “53h”	FFh	FFh	S
36D7h	[7:0]	—	Set to “00h”	01h	01h	S
36D8h	[7:0]	—	Set to “71h”	00h	00h	S
36DAh	[7:0]	—	Set to “8Ch”	FFh	FFh	S
36DBh	[7:0]	—	Set to “00h”	01h	01h	S

(7) Registers corresponding to address = 37**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3701h	[7:0]	ADBIT1 [7:0]	The value is set according to AD Conversion bits 00h: AD 10-bit 03h: AD 12-bit (11 bit + digital dither)	03h	03h	S
3724h	[7:0]	—	Set to “02h”	0Ah	0Ah	S
3726h	[7:0]	—	Set to “02h”	0Ah	0Ah	S
3732h	[7:0]	—	Set to “02h”	00h	00h	S
3734h	[7:0]	—	Set to “03h”	0Ah	0Ah	S
3736h	[7:0]	—	Set to “03h”	0Ah	0Ah	S
3742h	[7:0]	—	Set to “03h”	00h	00h	S

(8) Registers corresponding to address = 38**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3862h	[7:0]	—	Set to “E0h”	7Fh	7Fh	S
38CCh	[7:0]	—	Set to “30h”	33h	33h	S
38CDh	[7:0]	—	Set to “2Fh”	33h	33h	S

(9) Registers corresponding to address = 39**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
395Ch	[7:0]	—	Set to “0Ch”	00h	00h	S

(10) Registers corresponding to address = 3A**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3A42h	[7:0]	—	Set to “D1h”	11h	11h	S
3A4Ch	[7:0]	—	Set to “77h”	37h	37h	S
3AE0h	[7:0]	—	Set to “02h”	00h	00h	S
3AECh	[7:0]	—	Set to “0Ch”	00h	00h	S

(11) Registers corresponding to address = 3B**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3B00h	[7:0]	—	Set to “2Eh”	28h	28h	S
3B06h	[7:0]	—	Set to “29h”	23h	23h	S
3B98h	[7:0]	—	Set to “25h”	19h	19h	S
3B99h	[7:0]	—	Set to “21h”	19h	19h	S
3B9Bh	[7:0]	—	Set to “13h”	19h	19h	S
3B9Ch	[7:0]	—	Set to “13h”	19h	19h	S
3B9Dh	[7:0]	—	Set to “13h”	19h	19h	S
3B9Eh	[7:0]	—	Set to “13h”	16h	16h	S
3BA1h	[7:0]	—	Set to “00h”	04h	04h	S
3BA2h	[7:0]	—	Set to “06h”	09h	09h	S
3BA3h	[7:0]	—	Set to “0Bh”	09h	09h	S
3BA4h	[7:0]	—	Set to “10h”	0Dh	0Dh	S
3BA5h	[7:0]	—	Set to “14h”	0Dh	0Dh	S
3BA6h	[7:0]	—	Set to “18h”	0Dh	0Dh	S
3BA7h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BA8h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BA9h	[7:0]	—	Set to “1Ah”	0Dh	0Dh	S
3BACh	[7:0]	—	Set to “EDh”	00h	00h	S
3BADh	[7:0]	—	Set to “01h”	00h	00h	S
3BAEh	[7:0]	—	Set to “F6h”	22h	22h	S
3BAFh	[7:0]	—	Set to “02h”	00h	00h	S
3BB0h	[7:0]	—	Set to “A2h”	84h	84h	S
3BB1h	[7:0]	—	Set to “03h”	00h	00h	S
3BB2h	[7:0]	—	Set to “E0h”	A2h	A2h	S
3BB3h	[7:0]	—	Set to “03h”	00h	00h	S
3BB4h	[7:0]	—	Set to “E0h”	11h	11h	S
3BB5h	[7:0]	—	Set to “03h”	01h	01h	S
3BB6h	[7:0]	—	Set to “E0h”	ECh	ECh	S
3BB7h	[7:0]	—	Set to “03h”	01h	01h	S
3BB8h	[7:0]	—	Set to “E0h”	7Ah	7Ah	S
3BBAh	[7:0]	—	Set to “E0h”	D1h	D1h	S
3BBCh	[7:0]	—	Set to “DAh”	ECh	ECh	S
3BBEh	[7:0]	—	Set to “88h”	F5h	F5h	S
3BC0h	[7:0]	—	Set to “44h”	43h	43h	S
3BC2h	[7:0]	—	Set to “7Bh”	7Ah	7Ah	S
3BC4h	[7:0]	—	Set to “A2h”	A1h	A1h	S
3BC8h	[7:0]	—	Set to “BDh”	D1h	D1h	S
3BCAh	[7:0]	—	Set to “BDh”	DBh	DBh	S

(12) Registers corresponding to address = 40**h.

Address	bit	Register name	Description	Default value		Reflection timing
				By register	By address	
4001h	0	LANEMODE [2:0]	Output interface selection 1: CSI-2 2lane 3: CSI-2 4lane	3h	03h	S
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
4004h	[7:0]	TXCLKESC_FREQ [15:0]	The value is set according to INCK. Refer to “INCK setting”	1290h	90h	S
4005h	[7:0]				12h	
400Ch	0	INCKSEL6	The value is set according to INCK. Refer to “INCK setting”	1h	01h	S
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
4018h	[7:0]	TCLKPOST [15:0]	Global timing setting	00B7h	B7h	S
4019h	[7:0]				00h	
401Ah	[7:0]	TCLKPREPARE [15:0]	Global timing setting	0067h	67h	S
401Bh	[7:0]				00h	
401Ch	[7:0]	TCLKTRAIL [15:0]	Global timing setting	006Fh	6Fh	S
401Dh	[7:0]				00h	
401Eh	[7:0]	TCLKZERO [15:0]	Global timing setting	01DFh	DFh	S
401Fh	[7:0]				01h	
4020h	[7:0]	THSPREPARE [15:0]	Global timing setting	006Fh	6Fh	S
4021h	[7:0]				00h	
4022h	[7:0]	THSZERO [15:0]	Global timing setting	00CFh	CFh	S
4023h	[7:0]				00h	
4024h	[7:0]	THSTRAIL [15:0]	Global timing setting	006Fh	6Fh	S
4025h	[7:0]				00h	
4026h	[7:0]	THSEXIT [15:0]	Global timing setting	00B7h	B7h	S
4027h	[7:0]				00h	
4028h	[7:0]	TLPX [15:0]	Global timing setting	005Fh	5Fh	S
4029h	[7:0]				00h	
4074h	0	INCKSEL7 [2:0]	The value is set according to INCK. Refer to “INCK setting”	0h	00h	S
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Readout Drive mode

Operating mode

The table below shows the operating modes available with this sensor.
These frame rates indicate the maximum rates for each mode. When using a typical frame rate, please refer to the "List of Setting Register" at section "Image Data Output Format".

Mode	Lane	Data rate [Mbps/Lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording Pixels H [pixels]	Recording Pixels V [lines]	INCK [MHz]	1H period [Clock]	1V period [XHS]
All pixel	2	2079	10	10	44.4	3840	2160	27, 37.125, 74.25	746 (*1)	2238
			12	12	37.5				887 (*1)	
		1782	10	10	38.5			27, 37.125, 74.25	861 (*1)	
			12	12	32.4				1022 (*1)	
		1440	10	10	31.6			24, 72	1016 (*2)	
		891	10	10	19.8			27, 37.125, 74.25	1668 (*1)	
			12	12	16.6				1990 (*1)	
		720	10	10	16.2			24, 72	1985 (*2)	
		594	10	10	13.4			27, 37.125, 74.25	2238 (*1)	
			12	12	11.2				2958 (*1)	
	4	2376	10	10	90.9			27, 37.125, 74.25	365 (*1)	
		2079	10	10	82.9			27, 37.125, 74.25	400 (*1)	
			12	12	60.3				550 (*1)	
		1782	10	10	72.4			27, 37.125, 74.25	458 (*1)	
			12	12	60.3				550 (*1)	
		1485	10	10	61.6			27, 37.125, 74.25	538 (*1)	
		1440	10	10	60.4			24, 72	532 (*2)	
			12	12	51.1				629 (*2)	
		891	10	10	38.5			27, 37.125, 74.25	861 (*1)	
			12	12	32.4				1022 (*1)	
		720	10	10	31.6			24, 72	1017 (*2)	
			12	12	26.5				1210 (*2)	
		594	10	10	26.2			27, 37.125, 74.25	1265 (*1)	
			12	12	22.0				1506 (*1)	

(*1) Clock frequency = 74.25 [MHz]
(*2) Clock frequency = 72 [MHz]

Mode	Lane	Data rate [Mbps/Lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording Pixels H [pixels]	Recording Pixels V [lines]	INCK [MHz]	1H period [Clock*]	1V period [XHS]
Horizontal/ Vertical 2/2-line binning	2	2079	10	12	70.5	1920	1080	27, 37.125, 74.25	470 (*1)	2238
		1782	10	12	61.5			27, 37.125, 74.25	539 (*1)	
		891	10	12	32.4			27, 37.125, 74.25	1024 (*1)	
		594	10	12	21.9			27, 37.125, 74.25	1509 (*1)	
	4	2079	10	12	90.9			27, 37.125, 74.25	365 (*1)	
		1782	10	12	90.9			27, 37.125, 74.25	365 (*1)	
		1440	10	12	88.1			24, 72	365 (*2)	
		891	10	12	61.5			27, 37.125, 74.25	539 (*1)	
		720	10	12	51.0			24, 72	630 (*2)	
		594	10	12	42.4			27, 37.125, 74.25	782 (*1)	

(*1) Clock frequency = 74.25 [MHz]
(*2) Clock frequency = 72 [MHz]

Image Data Output Format (CSI-2 output)

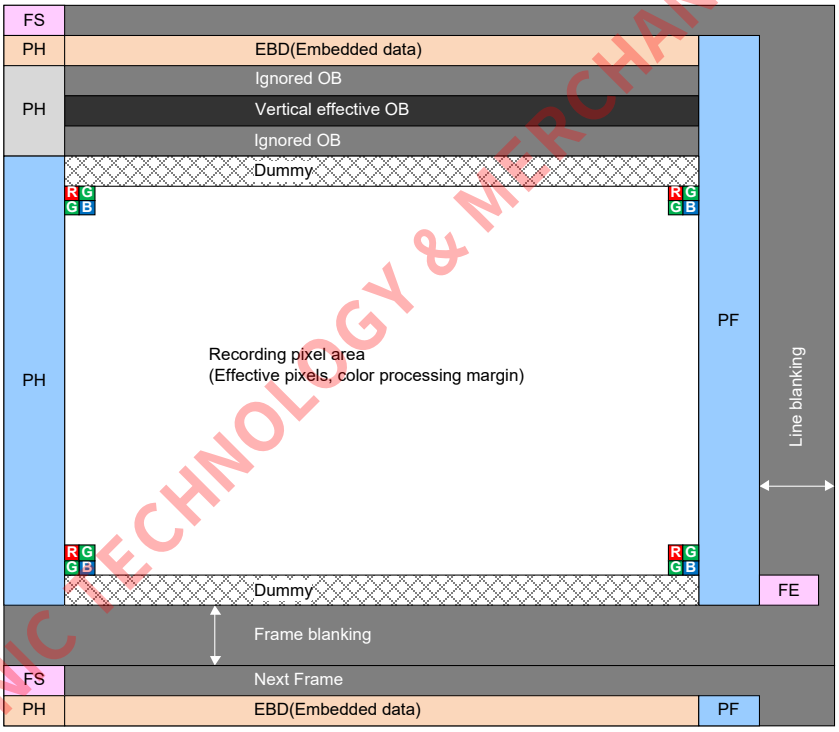
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 3032h MDBIT [0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

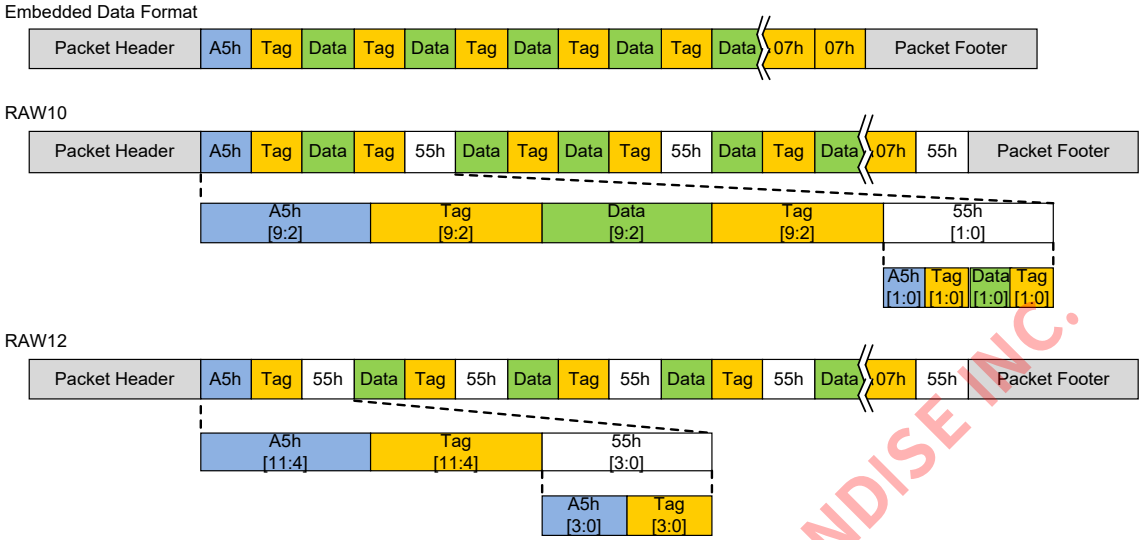
Frame Structure



Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.



The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found treat as end of Data.

Specific output examples are shown below.

Pixel (8bit)	bit	I²C address [HEX]	Data Byte Description	Description
1	[7:0]	—	—	ignored
2	[3:0]	301C[3:0]	WINMODE	
3	[3:0]	—	—	ignored
	[4]	3030[0]	HREVERSE	
	[6:5]	3022[1:0]	ADDMODE	
	[7]	—	—	ignored
4 to 8	[7:0]	—	—	ignored
9	[4:0]	—	—	ignored
	[5]	3030[1]	VREVERSE	
	[7:6]	—	—	ignored
10	[7:0]	—	—	ignored
11	[5:0]	—	—	ignored
	[7:6]	3031[1:0]	ADBIT	
12	[7:0]	—	—	ignored
13	[2:0]	4001[2:0]	LANEMODE	
	[3]	3032[0]	MDBIT	
	[7:4]	3030[3:0]	SYS_MODE	
18 to 23	[7:0]	—	—	ignored
24	[7:0]	3050[7:0]	SHR0	
25	[7:0]	3051[7:0]		
26	[3:0]	3052[3:0]		
	[7:4]	—	—	ignored
27 to 53	[7:0]	—	—	ignored
54	[7:0]	30E2[7:0]	BLKLEVEL	
55	[1:0]	30E3[1:0]		
	[7:2]	—		ignored
56 to 216	[7:0]	—	—	ignored

Output data is Data[7:0] = 00h from 217 to 224 pixel.
Output data is Data[7:0] = 07h from 225 to end pixel.

Image Data Output Format

The table below shows the register setting example of typical frame rate.
The frame rate is obtained by the following formula when using other frame rates.

Frame rate [frame / s] = 1 / (V_{TTL} × (1H period))

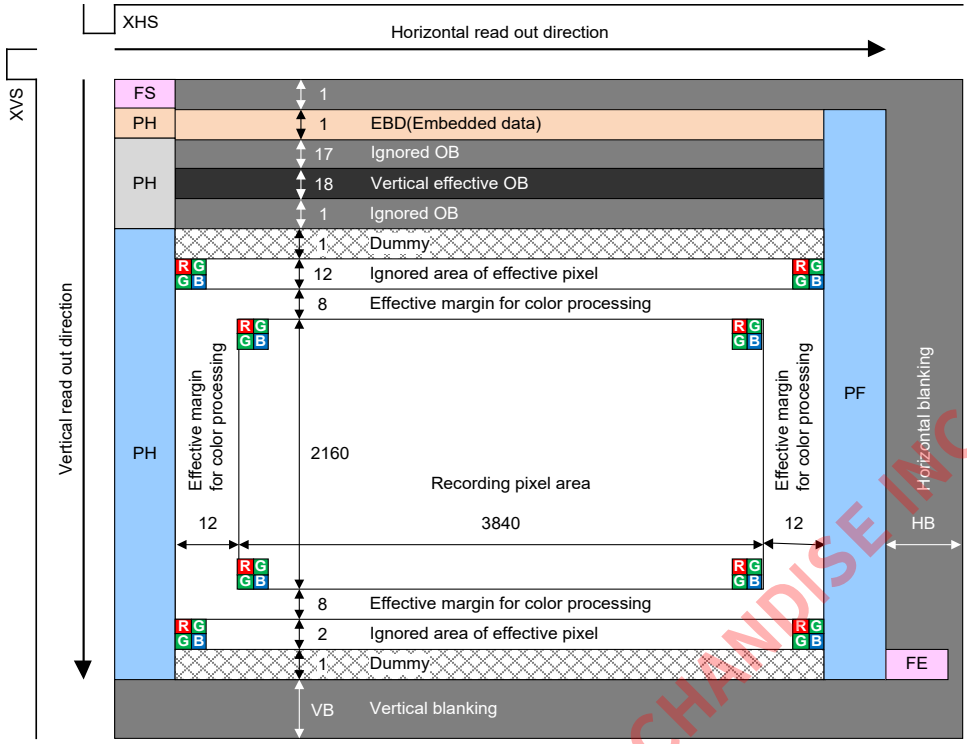
V_{TTL}	:	1 frame line length or VMAX
	:	“1V period” or more in “Operating mode”
1H period (unit [s])	:	“1H period” or more in “Operating mode”

All-pixel mode

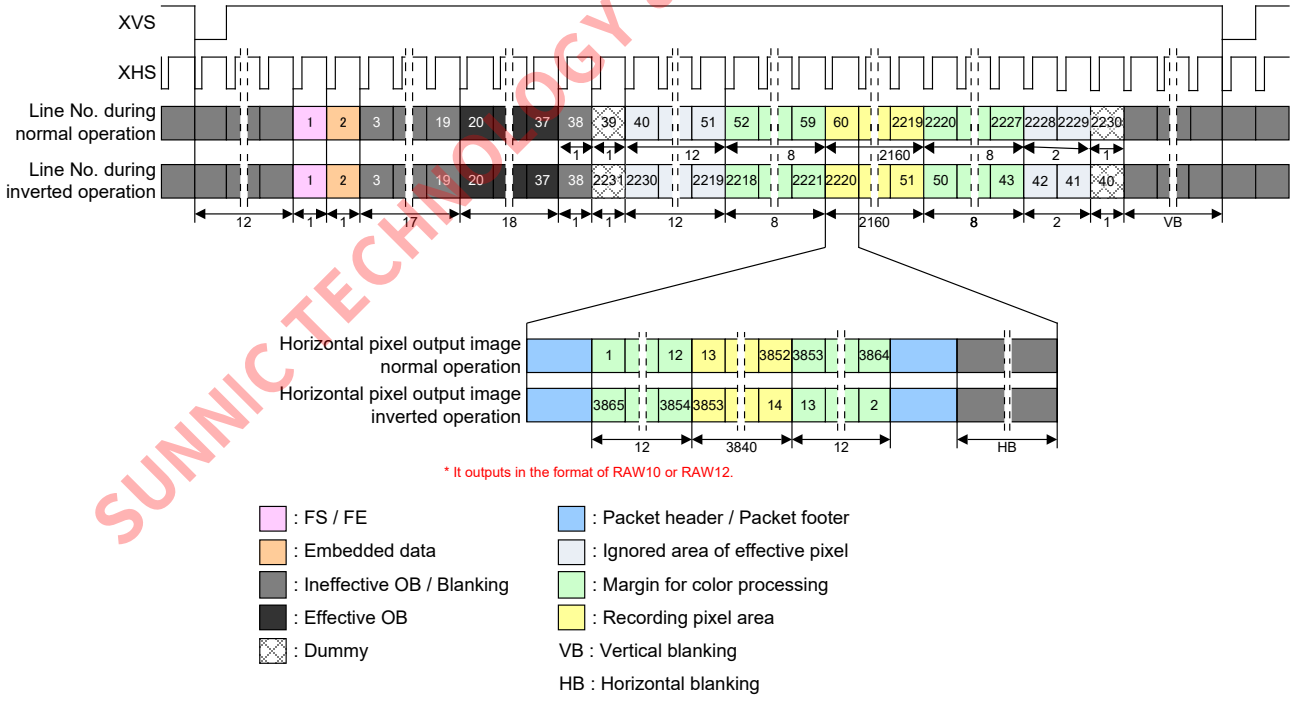
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane						Remarks
				10	15	15.74	30	30	30.01	[frame/s]
				594	891	720	1782	2079	1440	[Mbps/lane]
				44.5	29.7	28.3	14.9	14.9	14.9	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”						
3009h	[1:0]									
300Ah	[7:0]	CPWAIT_TIME	0B6h							
300Bh	[1:0]									
301Ch	[3:0]	WINMODE	0h	0h						All pixel mode
3022h	[1:0]	ADDMODE	0h	0h						All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh						
3025h	[7:0]									
3026h	[3:0]									
3028h	[7:0]	HMAX	226h	CE4h	898h	7F0h	44Ch	44Ch	42Ah	
3029h	[7:0]									
3030h	[0]	HREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h / 1h	0h / 1h	0h	0h / 1h	0h / 1h	0h	0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	0h / 1h	0h / 1h	0h	0h / 1h	0h / 1h	0h	0: 10 bit, 1: 12 bit
3033h	[3:0]	SYS_MODE	4h	7h	5h	9h	4h	2h	8h	
3115h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”						
3116h	[7:0]	INCKSEL2	28h							
3118h	[7:0]	INCKSEL3	0C0h							
3119h	[2:0]									
311Ah	[7:0]	INCKSEL4	0E0h							
311Bh	[2:0]									
311Eh	[7:0]	INCKSEL5	28h							
3200h to 3BFFh	[7:0]	Refer to “Register Map”								
4001h	[2:0]	LAMEMODE	3h	1h						2lame
4004h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”						
4005h	[7:0]									
400Ch	[0]	INCKSEL6	1h							
4018h	[7:0]	TCLKPOST	00B7h	0067h	007Fh	006Fh	00B7h	00D7h	009Fh	Global timing
4019h	[7:0]									
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	0037h	002Fh	0067h	007Fh	0057h	Global timing
401Bh	[7:0]									
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	0037h	002Fh	006Fh	007Fh	0057h	Global timing
401Dh	[7:0]									
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00F7h	00BFh	01DFh	0237h	0187h	Global timing
401Fh	[7:0]									
4020h	[7:0]	THSPREPARE	006Fh	002Fh	003Fh	002Fh	006Fh	0087h	005Fh	Global timing
4021h	[7:0]									
4022h	[7:0]	THSZERO	00CFh	004Fh	006Fh	0057h	00CFh	00EFh	00A7h	Global timing
4023h	[7:0]									
4024h	[7:0]	THSTRAIL	006Fh	002Fh	003Fh	002Fh	006Fh	0087h	005Fh	Global timing
4025h	[7:0]									
4026h	[7:0]	THSEXIT	00B7h	0047h	005Fh	004Fh	00B7h	00DFh	0097h	Global timing
4027h	[7:0]									
4028h	[7:0]	TLPX	005Fh	0027h	002Fh	0027h	005Fh	006Fh	004Fh	Global timing
4029h	[7:0]									
4074h	[2:0]	INCKSEL7	0h	Refer to “INCK setting”						

Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane								Remarks
				20 / 25	25 / 30.01	30	30.01 / 60.03	60	60	60	90	[frame/s]
				594	720	891	1440	1485	1782	2079	2376	[Mbps/lane]
				22.3 / 17.8	17.8 / 14.9	14.9	14.9 / 7.5	7.5	7.5	7.5	5.0	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”								
3009h	[1:0]											
300Ah	[7:0]	CPWAIT_TIME	0B6h									
300Bh	[1:0]											
301Ch	[3:0]	WINMODE	0h	0h								All pixel mode
3022h	[1:0]	ADDMODE	0h	0h								All pixel mode
3024h	[7:0]	VMAX	8CAh	8CAh								
3025h	[7:0]											
3026h	[3:0]											
3028h	[7:0]	HMAX	226h	672h / 528h	500h / 42Ah	44Ch	42Ah / 215h	226h	226h	226h	16Eh	
3029h	[7:0]											
3030h	[0]	HREVERSE	0h	0h / 1h								0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h								0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	1h / 0h	1h / 0h	0h / 1h	1h / 0h	0h	0h / 1h	0h / 1h	0h	0: 10 bit, 1: 12 bit
3032h	[0]	MDBIT	1h	1h / 0h	1h / 0h	0h / 1h	1h / 0h	0h	0h / 1h	0h / 1h	0h	0: 10 bit, 1: 12 bit
3033h	[3:0]	SYS_MODE	4h	7h	9h	5h	8h	8h	4h	2h	0h	
3115h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”								
3116h	[7:0]	INCKSEL2	28h									
3118h	[7:0]	INCKSEL3	0C0h									
3119h	[2:0]											
311Ah	[7:0]	INCKSEL4	0E0h									
311Bh	[2:0]											
311Eh	[7:0]	INCKSEL5	28h									
3200h to 3BFFh	[7:0]	Refer to “Register Map”										
4001h	[2:0]	LANEMODE	3h	3h								4lane
4004h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”								
4005h	[7:0]											
400Ch	[0]	INCKSEL6	1h									
4018h	[7:0]	TCLKPOST	00B7h	0067h	006Fh	007Fh	009Fh	00A7h	00B7h	00D7h	00E7h	Global timing
4019h	[7:0]											
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	002Fh	0037h	0057h	0057h	0067h	007Fh	008Fh	Global timing
401Bh	[7:0]											
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	002Fh	0037h	0057h	005Fh	006Fh	007Fh	008Fh	Global timing
401Dh	[7:0]											
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00BFh	00F7h	0187h	0197h	01DFh	0237h	027Fh	Global timing
401Fh	[7:0]											
4020h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	003Fh	005Fh	005Fh	006Fh	0087h	0097h	Global timing
4021h	[7:0]											
4022h	[7:0]	THSZERO	00CFh	004Fh	0057h	006Fh	00A7h	00AFh	00CFh	00EFh	010Fh	Global timing
4023h	[7:0]											
4024h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	003Fh	005Fh	005Fh	006Fh	0087h	0097h	Global timing
4025h	[7:0]											
4026h	[7:0]	THSEXIT	00B7h	0047h	004Fh	005Fh	0097h	009Fh	00B7h	00DFh	00F7h	Global timing
4027h	[7:0]											
4028h	[7:0]	TLPX	005Fh	0027h	0027h	002Fh	004Fh	004Fh	005Fh	006Fh	007Fh	Global timing
4029h	[7:0]											
4074h	[2:0]	INCKSEL7	0h	Refer to “INCK setting”								



Pixel Array Image Drawing in All pixel mode



Drive Timing Chart for All pixel mode

Horizontal/Vertical 2/2-line binning mode

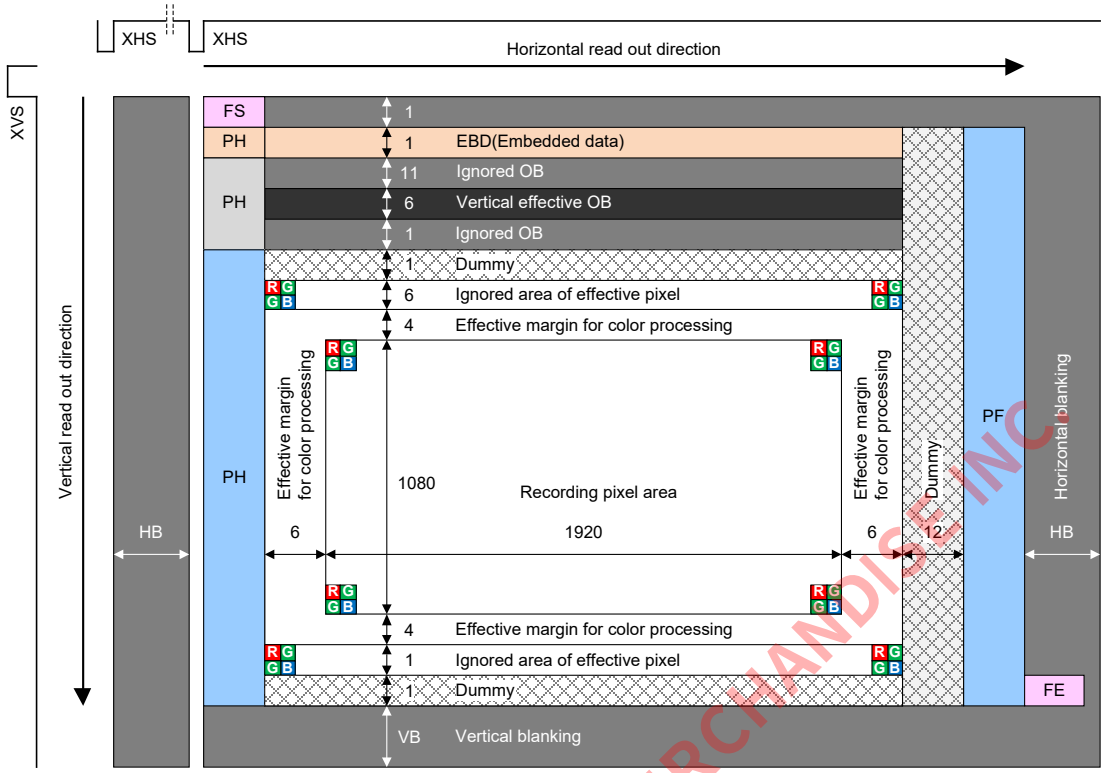
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane				Remarks
				10	15	30	30	[frame/s]
				594	891	1782	2079	[Mbps/lane]
				44.5	29.7	14.9	14.9	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”				
3009h	[1:0]							
300Ah	[7:0]	CPWAIT_TIME	0B6h					
300Bh	[1:0]							
301Ch	[3:0]	WINMODE	0h	0h				All pixel mode
3020h	[0]	HADD	0h	1h				Horizontal 2 binning
3021h	[0]	VADD	0h	1h				Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h				H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh				
3025h	[7:0]							
3026h	[3:0]							
3028h	[7:0]	HMAX	226h	CE4h	898h	44Ch	44Ch	
3029h	[7:0]							
3030h	[0]	HREVERSE	0h	0h / 1h				0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h				0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h				10 bit
3032h	[0]	MDBIT	1h	1h				12 bit
3033h	[3:0]	SYS_MODE	4h	7h	5h	4h	2h	
30D9h	[4:0]	DIG_CLP_VSTAET	06h	02h				H/V 2/2-line binning
30DAh	[1:0]	DIG_VLP_VNUM	2h	1h				H/V 2/2-line binning
3115h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”				
3116h	[7:0]	INCKSEL2	28h					
3118h	[7:0]	INCKSEL3	0C0h					
3119h	[2:0]							
311Ah	[7:0]	INCKSEL4	0E0h					
311Bh	[2:0]							
311Eh	[7:0]	INCKSEL5	28h					
3200h to 3BFFh	[7:0]	Refer to “Register Map”						
4001h	[2:0]	LANEMODE	3h	1h				2lane
4004h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”				
4005h	[7:0]							
400Ch	[0]	INCKSEL6	1h					
4018h	[7:0]	TCLKPOST	00B7h	0067h	007Fh	00B7h	00D7h	Global timing
4019h	[7:0]							
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	0037h	0067h	007Fh	Global timing
401Bh	[7:0]							
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	0037h	006Fh	007Fh	Global timing
401Dh	[7:0]							
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00F7h	01DFh	0237h	Global timing
401Fh	[7:0]							
4020h	[7:0]	THSPREPARE	006Fh	002Fh	003Fh	006Fh	0087h	Global timing
4021h	[7:0]							
4022h	[7:0]	THSZERO	00CFh	004Fh	006Fh	00CFh	00EFh	Global timing
4023h	[7:0]							

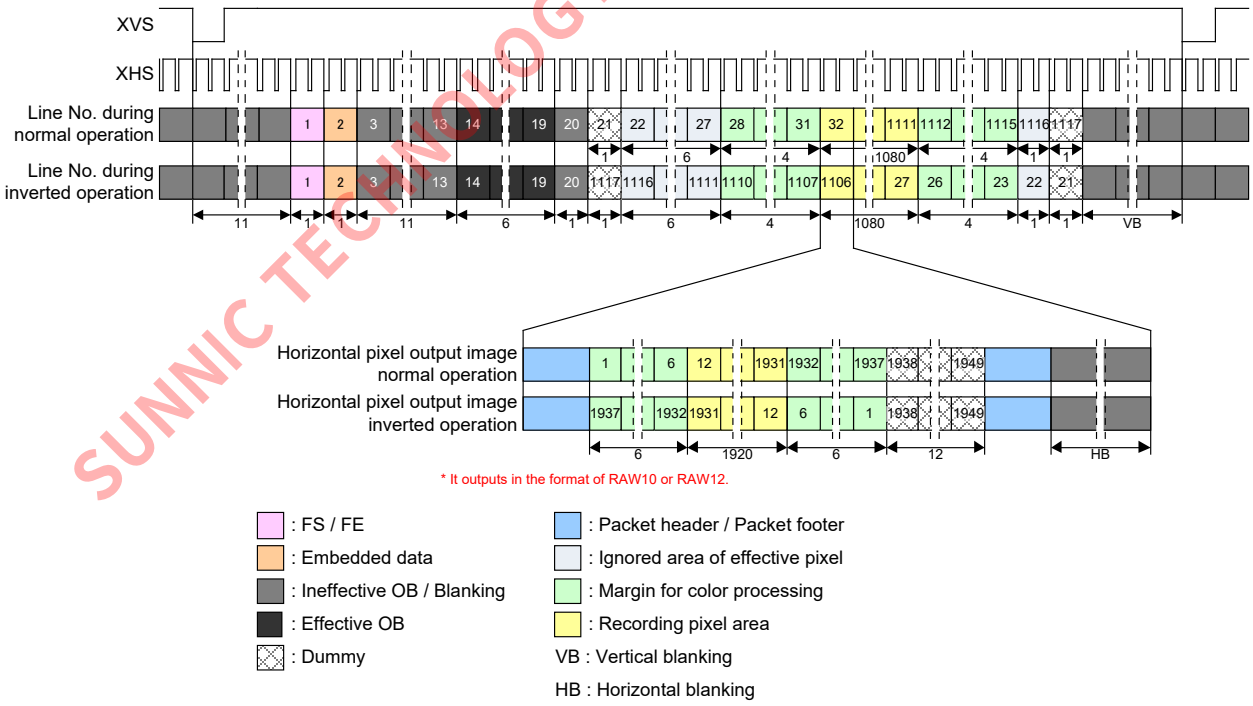
Address	bit	Register Name	Initial Value	CSI-2 serial / 2lane				Remarks
				10	15	30	30	[frame/s]
				594	891	1782	2079	[Mbps/lane]
4024h	[7:0]	THSTRAIL	006Fh	002Fh	003Fh	006Fh	0087h	Global timing
4025h	[7:0]							
4026h	[7:0]	THSEXIT	00B7h	0047h	005Fh	00B7h	00DFh	Global timing
4027h	[7:0]							
4028h	[7:0]	TLPX	005Fh	0027h	002Fh	005Fh	006Fh	Global timing
4029h	[7:0]							
4074h	[2:0]	INCKSEL7	0h	Refer to “INCK setting”				

Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane						Remarks
				20	25	30	30.01	60	60	[frame/s]
				594	720	891	1440	1782	2079	[Mbps/lane]
				22.3	17.8	14.9	14.9	7.5	7.5	1H period [μs]
3008h	[7:0]	BCWAIT_TIME	0FFh	Refer to “INCK setting”						
3009h	[1:0]									
300Ah	[7:0]	CPWAIT_TIME	0B6h							
300Bh	[1:0]									
301Ch	[3:0]	WINMODE	0h	0h						All pixel mode
3020h	[0]	HADD	0h	1h						Horizontal 2 binning
3021h	[0]	VADD	0h	1h						Vertical 2 binning
3022h	[1:0]	ADDMODE	0h	1h						H/V 2/2-line binning
3024h	[7:0]	VMAX	8CAh	8CAh						
3025h	[7:0]									
3026h	[3:0]									
3028h	[7:0]	HMAX	226h	672h	4FFh	44Ch	42Ah	226h	226h	
3029h	[7:0]									
3030h	[0]	HREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
	[1]	VREVERSE	0h	0h / 1h						0: Nor. , 1: Inv.
3031h	[1:0]	ADBIT	1h	0h						10 bit
3032h	[0]	MDBIT	1h	1h						12 bit
3033h	[3:0]	SYS_MODE	4h	7h	9h	5h	8h	4h	2h	
30D9h	[4:0]	DIG_CLP_VSTAET	06h	02h						H/V 2/2-line binning
30DAh	[1:0]	DIG_VLP_VNUM	2h	1h						H/V 2/2-line binning
3115h	[7:0]	INCKSEL1	00h	Refer to “INCK setting”						
3116h	[7:0]	INCKSEL2	28h							
3118h	[7:0]	INCKSEL3	0C0h							
3119h	[2:0]									
311Ah	[7:0]	INCKSEL4	0E0h							
311Bh	[2:0]									
311Eh	[7:0]	INCKSEL5	28h							
3200h to 3BFFh	[7:0]	Refer to “Register Map”								
4001h	[2:0]	LANEMODE	3h	3h						4lane
4004h	[7:0]	TXCLCKES_FREQ	1290h	Refer to “INCK setting”						
4005h	[7:0]									
400Ch	[0]	INCKSEL6	1h							
4018h	[7:0]	TCLKPOST	00B7h	0067h	006Fh	007Fh	009Fh	00B7h	00D7h	Global timing
4019h	[7:0]									
401Ah	[7:0]	TCLKPREPARE	0067h	0027h	002Fh	0037h	0057h	0067h	007Fh	Global timing
401Bh	[7:0]									
401Ch	[7:0]	TCLKTRAIL	006Fh	0027h	002Fh	0037h	0057h	006Fh	007Fh	Global timing
401Dh	[7:0]									
401Eh	[7:0]	TCLKZERO	01DFh	00B7h	00BFh	00F7h	0187h	01DFh	0237h	Global timing
401Fh	[7:0]									
4020h	[7:0]	THSPREPARE	006Fh	002Fh	002Fh	003Fh	005Fh	006Fh	0087h	Global timing
4021h	[7:0]									
4022h	[7:0]	THSZERO	00CFh	004Fh	0057h	006Fh	00A7h	00CFh	00EFh	Global timing
4023h	[7:0]									

Address	bit	Register Name	Initial Value	CSI-2 serial / 4lane						Remarks
				20	25	30	30.01	60	60	[frame/s]
				594	720	891	1440	1782	2079	[Mbps/lane]
4024h	[7:0]	THSTRAIL	006Fh	002Fh	002Fh	003Fh	005Fh	006Fh	0087h	Global timing
4025h	[7:0]									
4026h	[7:0]	THSEXIT	00B7h	0047h	004Fh	005Fh	0097h	00B7h	00DFh	Global timing
4027h	[7:0]									
4028h	[7:0]	TLPX	005Fh	0027h	0027h	002Fh	004Fh	005Fh	006Fh	Global timing
4029h	[7:0]									
4074h	[2:0]	INCKSEL7	0h	Refer to “INCK setting”						



Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode



Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode

In "2/2 binning", pixels binning by normal direction and inverted direction are shifted by the same color one pixel.

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
This function support All-pixel mode, Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR, Digital overlap HDR and Vertical / Horizontal direction-normal / inverted readout mode of each modes.

Cropping position is set, regarding effective pixel with dummy start position as origin (0, 0) in normal mode direction. That is a start point which is an offset from the origin and cropping width.
Cropping is available from each driving mode and horizontal period is fixed to the value at same as the mode before window cropping. Pixels cropped by horizontal cropping setting are output with left shifted and that extends the horizontal blanking period.
Window position and size is used fixed value. (An ignore frame is output when it is changed.)

Window cropping image is shown in the figure below.
The same physical pixel area as all-pixel mode is cropped when start position and width are same setting in Horizontal/Vertical 2/2-line binning mode, Multiple exposure HDR and Digital overlap HDR.
At inverted mode, it is the same as the “Recording pixel with Effective margin for color processing (green rectangle in the figure) “ area in normal mode.

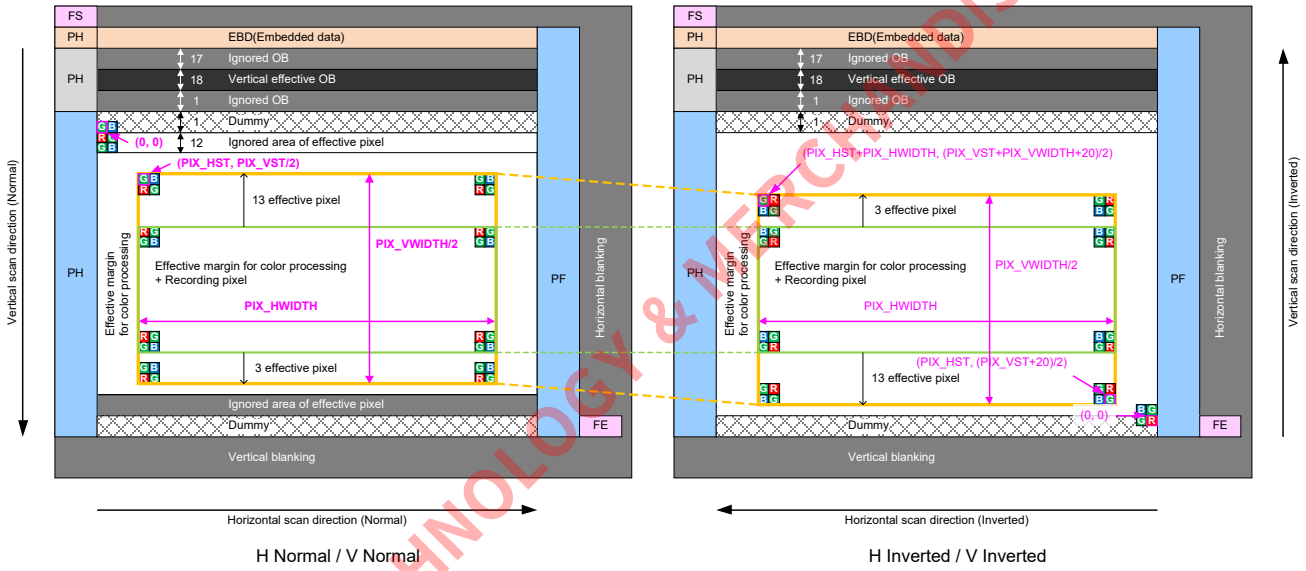


Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction

Supplement) The first readout pixel color is “G” at windows cropping mode in inverted direction.

List of Setting Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
WINMODE	301Ch	[3:0]	0h	4h: Window Cropping mode	
PIX_HST	3040h	[7:0]	0000h	Effective pixel Start position (Horizontal direction)	Specified as a multiple of 2
	3041h	[4:0]			
PIX_HWIDTH	3042h	[7:0]	0F18h	Effective pixel Cropping width (Horizontal direction)	Specified as a multiple of 24
	3043h	[4:0]			
PIX_VST	3044h	[7:0]	0000h	Effective pixel Star position (Vertical direction) Designated in V units (Line×2)	Specified as a multiple of 4
	3045h	[4:0]			
PIX_VWIDTH	3046h	[7:0]	1120h	Effective pixel Cropping width (Vertical direction) Designated in V units (Line×2)	Specified as a multiple of 4
	3047h	[4:0]			

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

Set WINMODE: 4h.

◆ PIX_VST, PIX_VWIDTH

Set PIX_VST, PIX_VWIDTH to a multiple of 4.

$PIX\_VST = n_1 \times 4$
$PIX\_VWIDTH = n_2 \times 4$

Cropped starting position and width is set multiple of 2 addresses, because PIX_VST, PIX_VWIDTH is internal V address unit.

Cropped area is needed to set pre 13 pixel, rear 3 pixel for signal processing.

◆ PIX_HST, PIX_HWIDTH

Set PIX_HST to a multiple of 2.
Set PIX_HWIDTH to a multiple of 24.

$PIX\_HST = n_3 \times 2$
$PIX\_VWIDTH = n_4 \times 24$

Where n_{1-4} are integer equal or more than 0.

V_{TTL} (1frame line length or VMAX) ≥ (PIX_VWIDTH / 2) + 46
Set V_{TTL} to 1222 or more.

$V_{TTL} \geq 1222$

◆ Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))
1H period (unit: [s]) : Set "1H period" or more in the table of "Operating mode" before cropping mode.

Description of Various Function

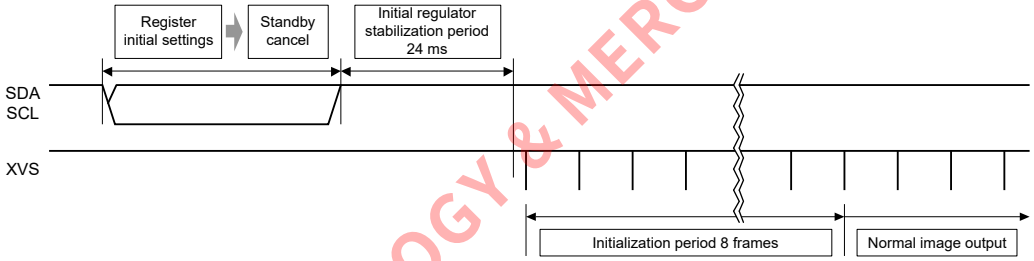
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
STANDBY	3000h	[0]	1h	1h: Standby 0h: Operating	Register communication is executed in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization 24 ms or more.
For details of the sequence of setting and cancel standby mode, see the sensor setting flow after power on.



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER register. Establish the XMASTER status before canceling the system reset. (Do not switch this register status during operation.)

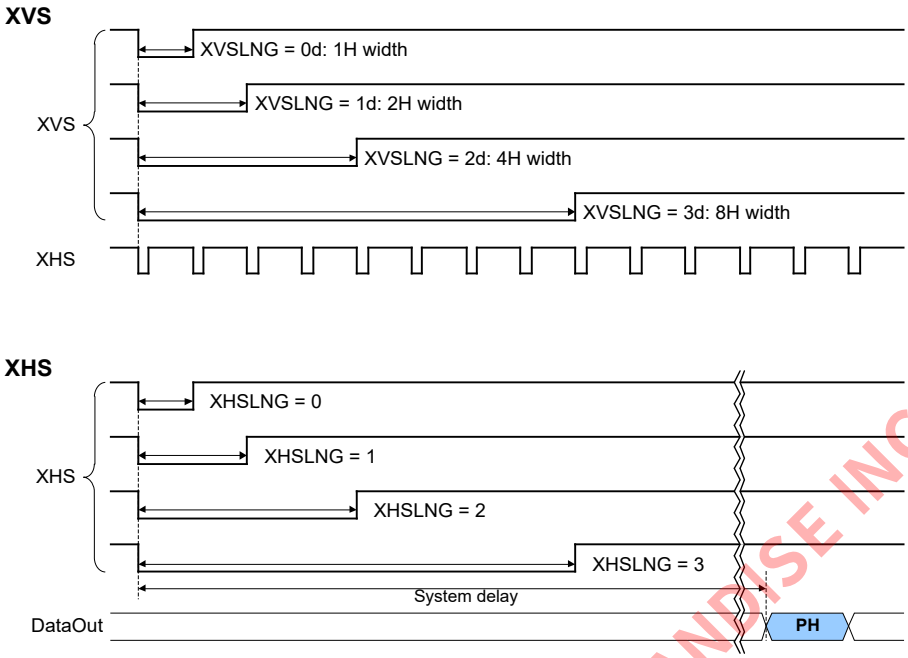
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register 0h in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMASTER	3003h	[0]	0h	0h: Master mode 1h: Slave mode	

List of Register in Master Mode

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMSTA	3002h	[0]	1h	1h: Master operation ready 0h: Master operation start	The master operation starts by setting 0.
VMAX [19:0]	3024h	[7:0]	008CAh	See the item of each drive mode.	Line number per frame designated
	3025h	[7:0]			
	3026h	[3:0]			
HMAX [15:0]	3028h	[7:0]	0226h	See the item of each drive mode.	Clock number per line designated
	3029h	[7:0]			
XVSOUTSEL [1:0]	30C0h	[1:0]	2h	0h: Fixed to Low 2h: VSYNC output	
XHSOUTSEL [1:0]		[3:2]	2h	0h: Fixed to Low 2h: HSYNC output	
XVS_DRV [1:0]	30C1h	[1:0]	3h	0h: XVS output (Master mode) 3h: Hi-z (Slave mode)	
XHS_DRV [1:0]		[3:2]	3h	0h: XHS output (Master mode) 3h: Hi-z (Slave mode)	
XVSLNG [1:0]	30CCh	[5:4]	0h	0h: 1H, 1h: 2H, 2h: 4H, 3h: 8H	XVS low level pulse width designated
XHSLNG [1:0]	30CDh	[6:5]	0h	0h: 16clock, 1h: 32clock 2h: 64clock, 3h: 128clock See the next	XHS low level pulse width designated



XVS/XHS output waveform in sensor master mode

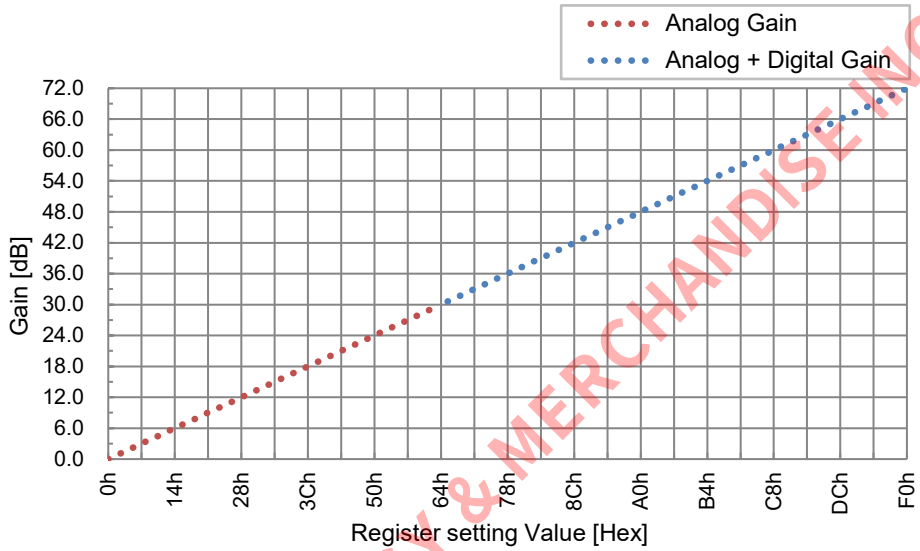
The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 72dB by the GAIN_PCG_0 [8:0] register setting. The same setting is applied in all colors.

The value which is 10/3 times the gain is set to register. (0.3 dB step)

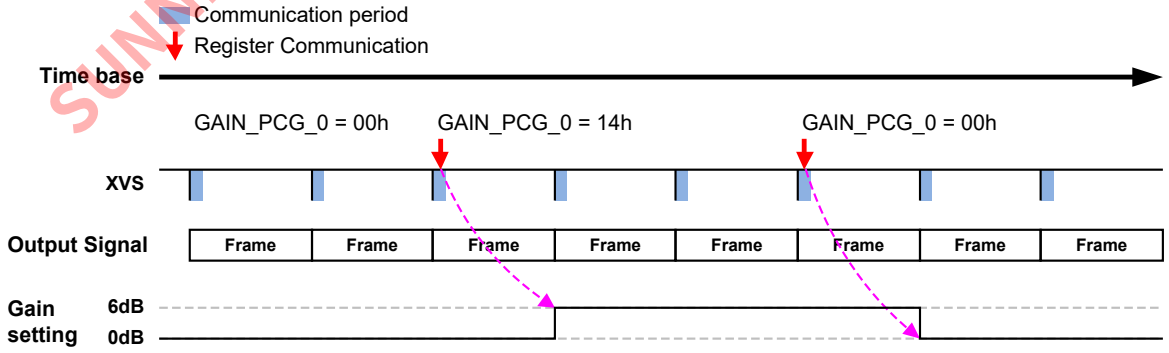
Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN_PCG_0 = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN_PCG_0 = 2Ah



List of PGC Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit		Setting range	
GAIN_PCG_0 [8:0]	3090h	[7:0]	000h	00h-F0h (0d-240d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	3091h	[0]			

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [9:0] register.
Note that the offset unit changes according to the output bit setting.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 LSB. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 LSB.

Use with values shown below is recommended.
10-bit output: 032h (50d)
12-bit output: 032h (200d)

List of Black Level Adjustment Register

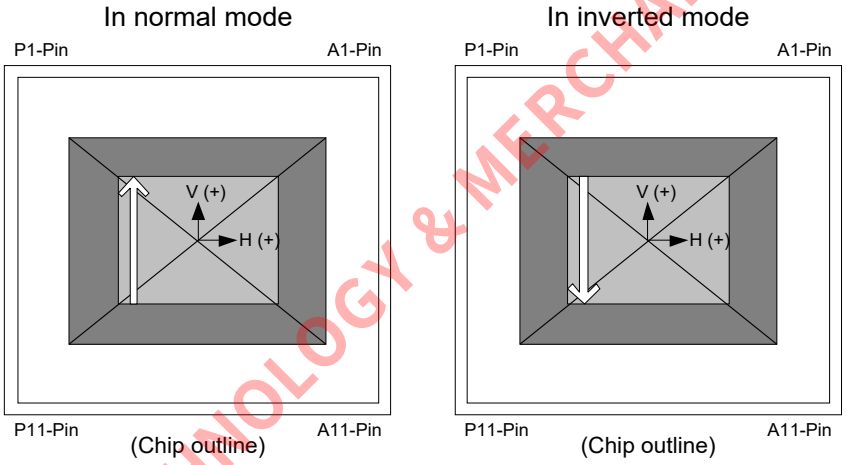
Register	Register details		Initial value	Setting value
	Address	bit		
BLKLEVEL [9:0]	30E2h	[7:0]	032h	000h to 3FFh
	30E3h	[1:0]		

Normal Operation and Inverted Operation

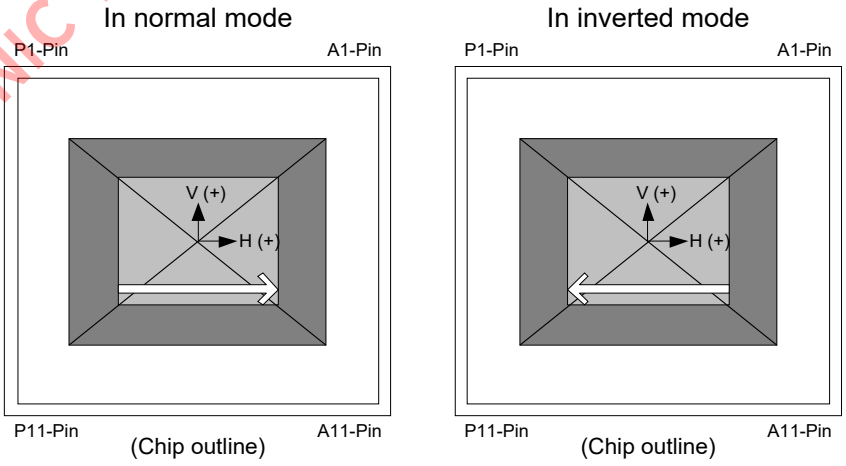
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register settings and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. See the section of “List of Setting Register” for the other register settings.
One invalid frame is generated when reading immediately after the readout vertical direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
HREVERSE	3030h	[0]	0h	0h: Normal 1h: Inverted
VREVERSE		[1]	0h	0h: Normal 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - SHR0 × (1H period) + T_{offset}

Where T_{offset} is 1.79 [µs] at AD 10bit mode and 2.68 [µs] at AD 12bit mode.

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See “Operating Modes” for the 1H period.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

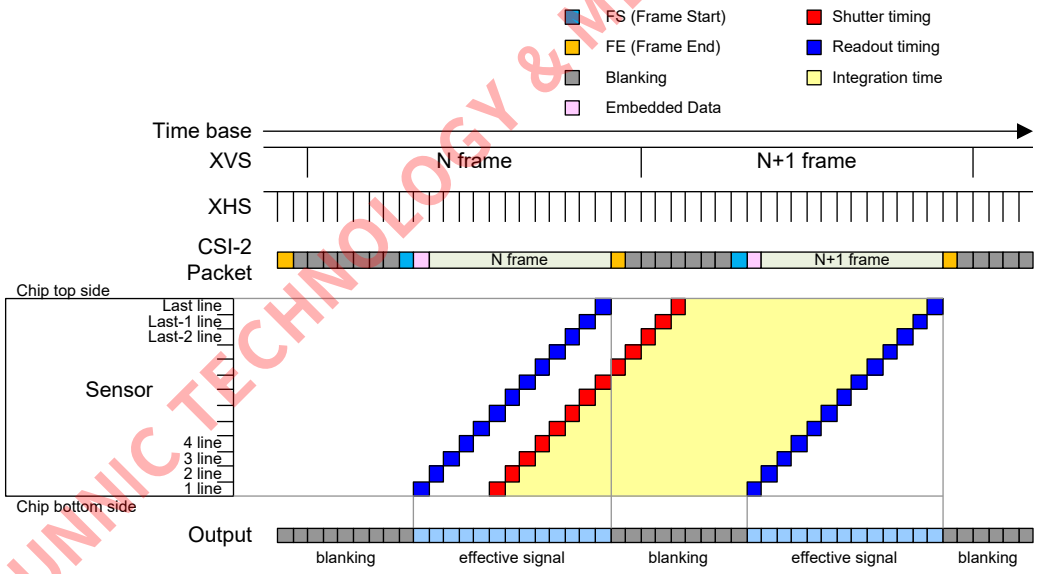


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 8 and (Number of lines per frame - 4). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register	Register details		Initial value	Setting value
	Address	bit		
SHR0 [19:0]	3050h	[7:0]	00066h	Sets the shutter sweep time. 8 to (Number of lines per frame - 4) * Others: Setting prohibited
	3051h	[7:0]		
	3052h	[3:0]		
VMAX [19:0]	3024h	[7:0]	008CAh	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	3025h	[7:0]		
	3026h	[3:0]		

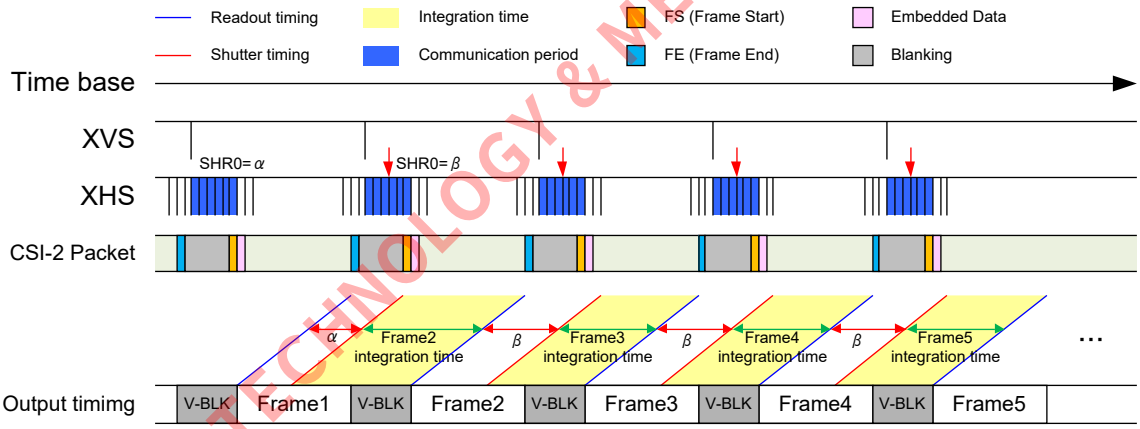


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [19:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

Although the maximum value of long exposure operation changes in each mode, the maximum of long time exposure is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

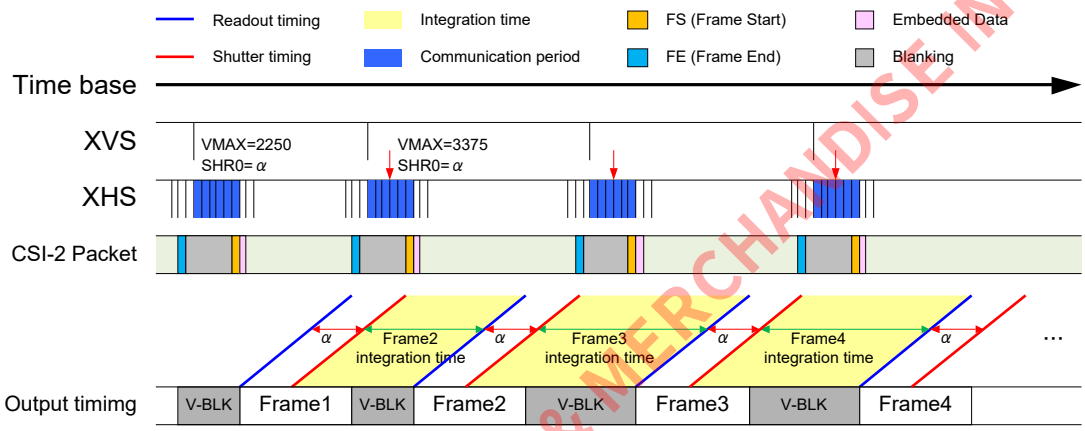


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time
	VMAX*	SHR0**	
All-pixel scan mode	2250	2246	4H + T_{offset}
		⋮	⋮
		N	(2250 - N) H + T_{offset}
		⋮	⋮
		8	2242H + T_{offset}

Where T_{offset} is 1.79 [µs] at AD 10bit mode and 2.68 [µs] at AD 12bit mode.

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHR0 setting value (N) is set between “8” and “the VMAX value (M) – 4”.

Signal Output
CSI-2 output

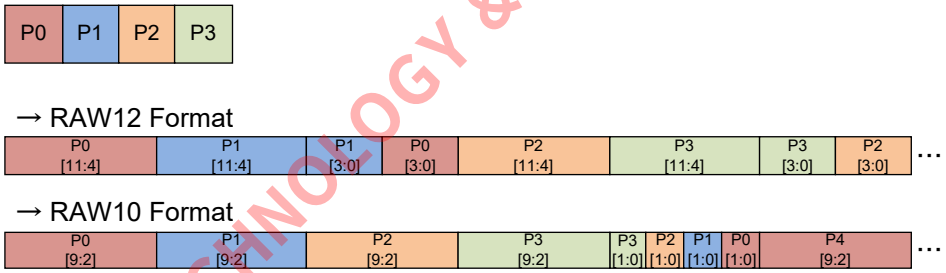
The output formats of this sensor support the following modes.

CSI-2 serial 2 Lane / 4 Lane, RAW10 / RAW12

The 2 Lane / 4 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin.
The DMO1P / DMO1N are called the Lane1 data signal, the DMO2P / DMO2N are called the Lane2 data signal, the DMO3P / DMO3N are called the Lane3 data signal, the DMO4P / DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DCKP / DCKN of the CSI-2 pins.
In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The bit rate maximum value is 2376 Mbps / Lane in 4 Lane mode and 2079 Mbps / Lane in 2 Lane mode.
The select of RAW10 / RAW12 is set by the register: MDBIT [0]. The number of output lanes is set by the register: LANEMODE [2:0].
Unused lanes output signals conformed to MIPI standard.

Register	Register details		Initial value	Setting value
	Address	bit		
MDBIT	3032h	[0]	1h	0h: RAW10 1h: RAW12
LANEMODE [2:0]	4011h	[2:0]	3h	1h: 2 Lane 3h: 4 Lane

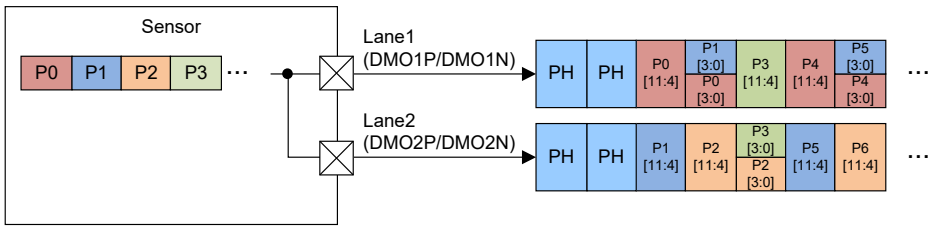
The formats of RAW12 and RAW10 are shown below.



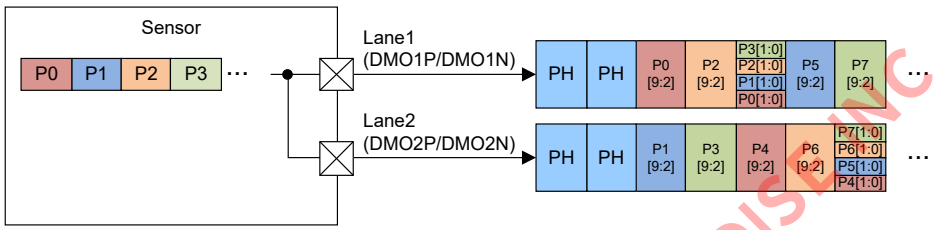
The Example of Format of RAW12 / RAW10

The each formal of 2 Lane and 4 Lane are shown below.

a) 2 Lane-RAW12

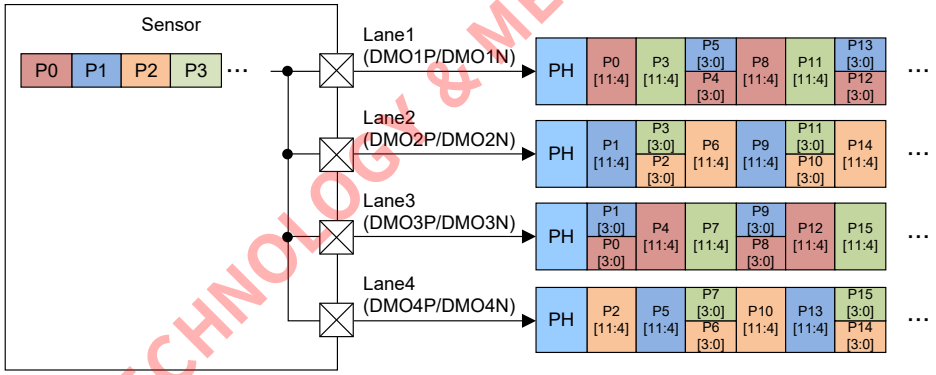


b) 2 Lane-RAW10

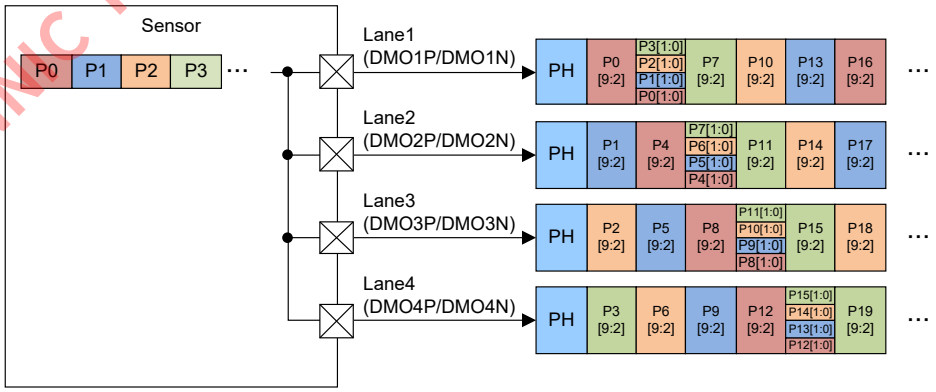


2 Lane Output Format

c) 4 Lane-RAW12



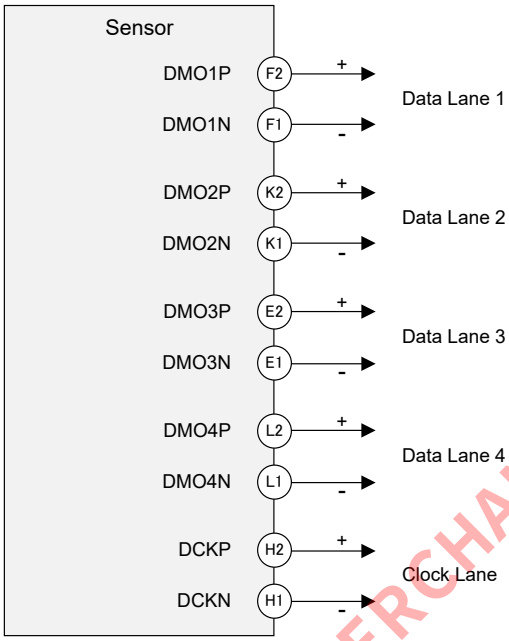
d) 4 Lane-RAW10



4 Lane Output Format

MIPI Transmitter

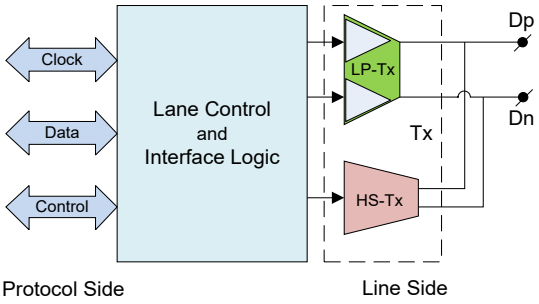
Output pins (DMOP1, DMOM1, DMOP2, DMOM2, DMOP3, DMOM3, DMOP4, DMOM4, DCKP, DCKM) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.20.00
・MIPI Alliance Specification for D-PHY Version 1.20.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane is 2376 Mbps / Lane.



Universal Lane Module Functions

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of “Operating Modes” for the correspondence with each mode.

List of Bit Width Selection

Register	Register details		Initial value	Setting value
	Address	bit		
ADBIT	3031h	[0]	1h	0: 10 bit 1: 12 bit

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 24 MHz, 27 MHz, 37.125 MHz, 72 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

In the MIPI Alliance Specification for D-PHY Version 1.2,
when operating above 1500 Mbps, an initial deskew sequence shall be transmitted before High-Speed Data Transmission. When operating at or below 1500 Mbps, the transmission of the initial deskew sequence is optional. When operating at or above 1440 Mbps, this Sensor transmits the initial deskew burst.

INCK Setting Register

Data rate: 2376Mbps / lane

Register	Register details		Initial value	INCK		
	Address	Bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	0h	0h	0h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	108h	100h	100h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 2079Mbps / lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	2h	2h	2h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0E7h	0E0h	0E0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1782Mbps / lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	4h	4h	4h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0C6h	0C0h	0C0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1485 Mbps / lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	8h	8h	8h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0A5h	0A0	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h	0h

Data rate: 1440Mbps / lane

Register	Register details		Initial value	INCK	
	Address	bit		24 [MHz]	72 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	54h	F8h
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	3Bh	B0h
SYS_MODE	3034h	[3:0]	4h	8h	8h
INCKSEL1	3115h	[7:0]	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0B4h	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0FCh	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	0600h	1200h
INCKSEL6	400Ch	[0]	1h	1h	1h
INCKSEL7	4074h	[2:0]	0h	0h	0h

Data rate: 891Mbps / lane

Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	5h	5h	5h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0C6h	0C0h	0C0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	0h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h	1h

Data rate: 720Mbps / lane

Register	Register details		Initial value	INCK	
	Address	bit		24 [MHz]	72 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	54h	F8h
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	3Bh	B0h
SYS_MODE	3034h	[3:0]	4h	9h	9h
INCKSEL1	3115h	[7:0]	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	0B4h	0A0h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0FCh	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	0600h	1200h
INCKSEL6	400Ch	[0]	1h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h

Data rate: 594Mbps / lane

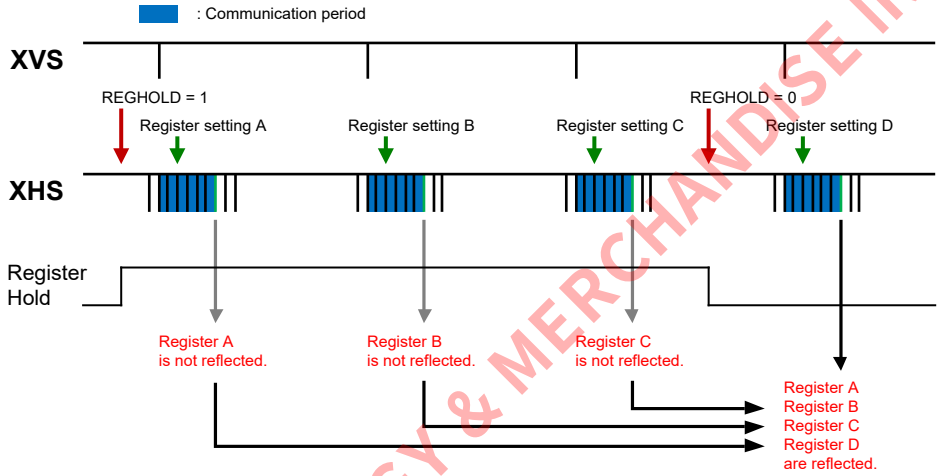
Register	Register details		Initial value	INCK		
	Address	bit		27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	3009-08h	[9:0]	0FFh	05Dh	07Fh	0FFh
CPWAIT_TIME	300B-0Ah	[9:0]	0B6h	042h	05Bh	0B6h
SYS_MODE	3034h	[3:0]	4h	7h	7h	7h
INCKSEL1	3115h	[7:0]	00h	00h	00h	00h
INCKSEL2	3116h	[7:0]	28h	23h	24h	28h
INCKSEL3	3119-18h	[10:0]	0C0h	084h	080h	080h
INCKSEL4	311B-1Ah	[10:0]	0E0h	0E7h	0E0h	0E0h
INCKSEL5	311Eh	[7:0]	28h	23h	24h	28h
TXCLKESC_FREQ	4005-04h	[15:0]	1290h	06C0h	0948h	1290h
INCKSEL6	400Ch	[0]	1h	0h	0h	0h
INCKSEL7	4074h	[2:0]	0h	1h	1h	1h

Register Hold Setting

V reflected register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 prevents the registers that set thereafter from being reflected at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the desired frame to reflect the register.

Register Hold Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
REGHOLD	3001h	[0]	0h	0: Invalid 1: Valid (Register hold)



Register Hold Setting

Mode Transitions

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
Horizontal direction normal	→	Horizontal direction inverted	Via the Standby state is unnecessary.
Horizontal direction inverted	→	Horizontal direction normal	
All-pixel scan mode	→	Window cropping mode	Via the Standby state is unnecessary. One invalid frame is generated.
Window cropping mode	→	All-pixel scan mode	
Vertical direction normal	→	Vertical direction inverted	
Vertical direction inverted	→	Vertical direction normal	
Vertical direction line number change (Master mode : VMAX change, Slave mode : XVS interval change)			
Horizontal direction 1H period change (Master mode : HMAX change, Slave mode : XHS interval change)			
- Transition between modes other than above - Change the input frequency of INCK *1 - Change the register setting noted “S” in the reflection timing column of the Register Map.			Via the standby state is necessary.

*1 When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Other Function

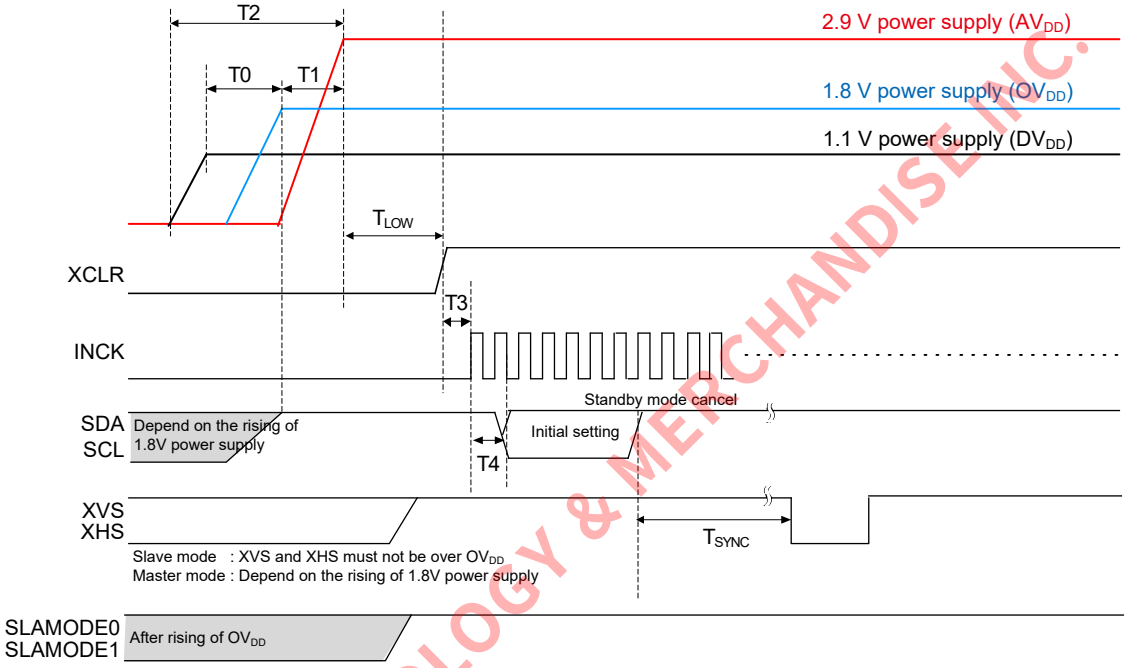
This sensor has the function as below. About detail, refer to each application note.

- Digital overlap HDR (2 / 3 frame)
- Multiple exposure HDR (2 / 4 frame)
- Additional Function of Synchronizing Sensors

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.1 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
3. The system clear is applied by setting XCLR to High level. The maser clock input after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

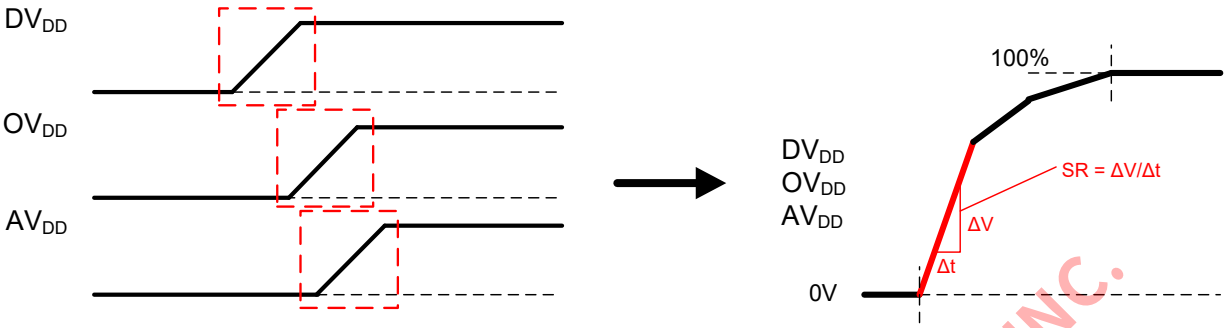


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.1 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
2.9 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	1	—	μs
Clear OFF → Communication start	T4	20	—	μs
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	24	—	ms

Slew Rate Limitation of Power-on Sequence

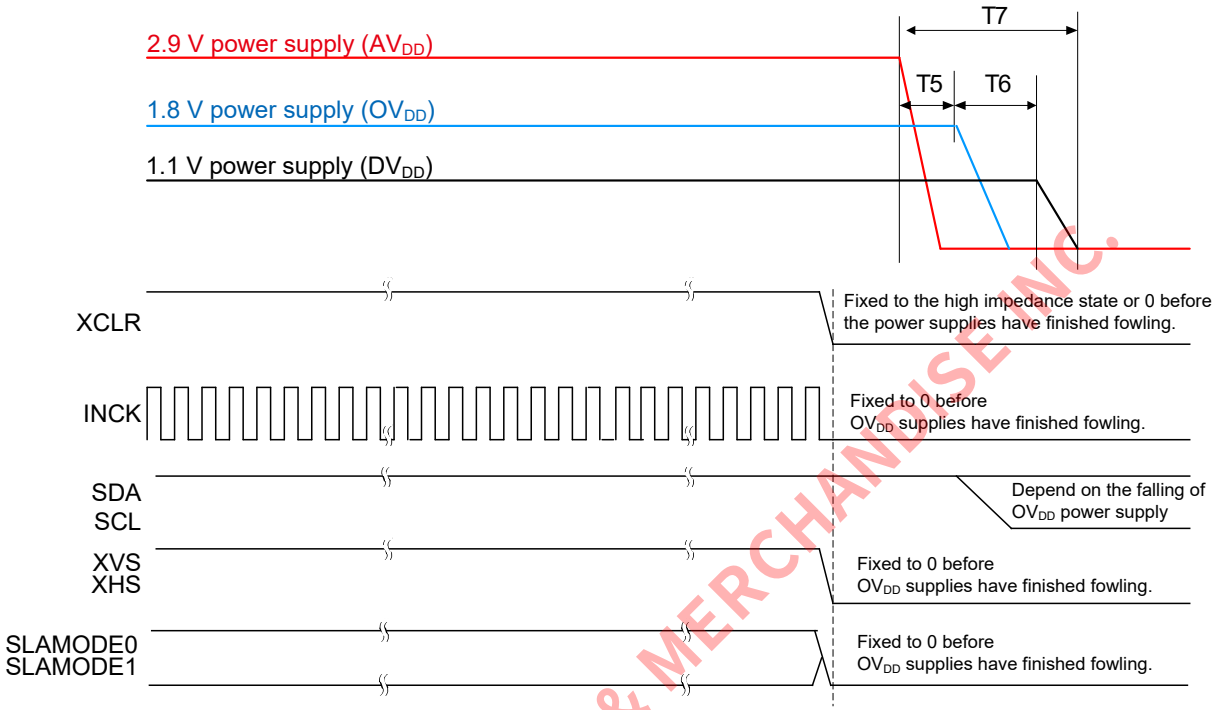
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.1 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		AV_{DD} (2.9 V)	—	25	mV/μs	

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.1 V power supply (DV_{DD}). In addition, all power supplies should be falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



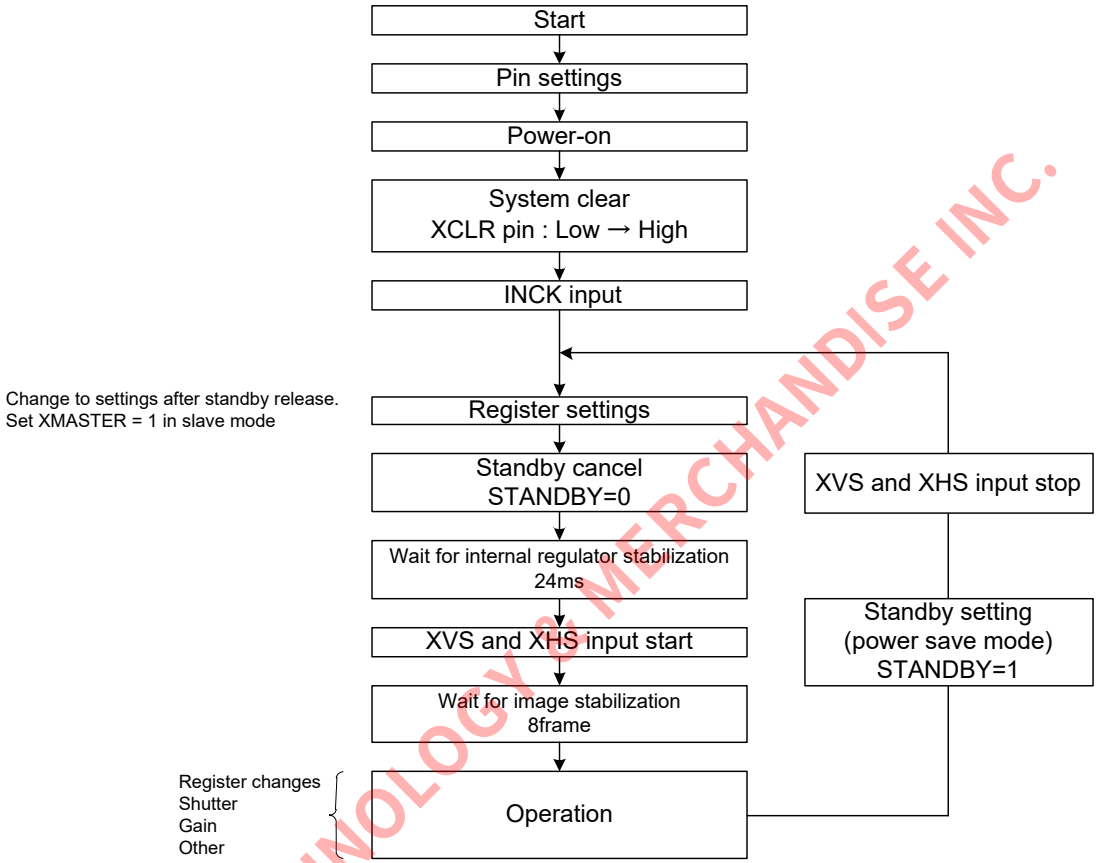
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
2.9 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.1 V power shut down	T6	0	—	ns
Shut down time of all power supply	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

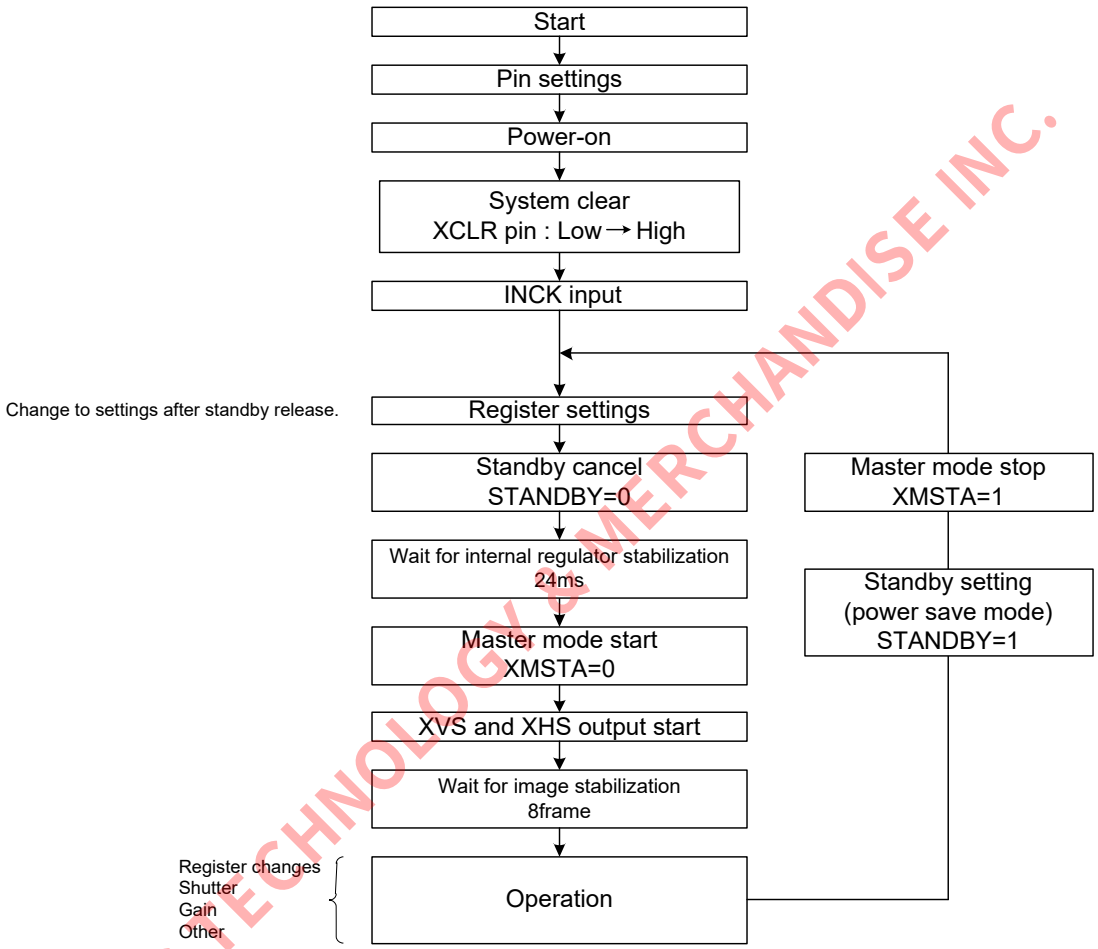
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

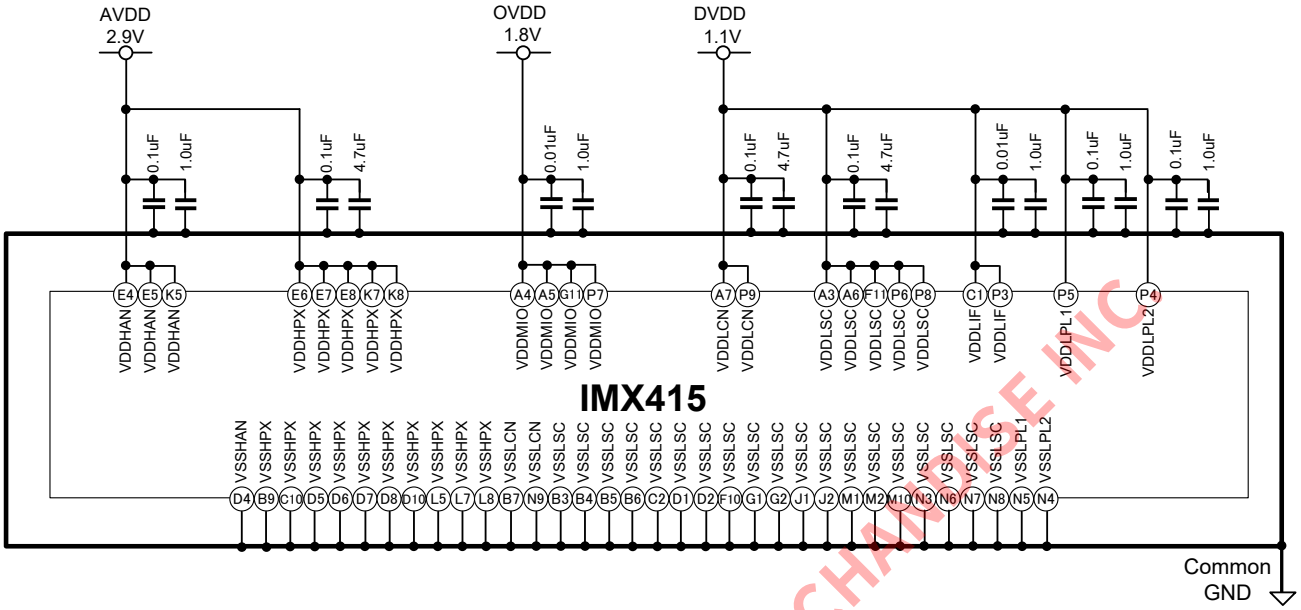
Setting Flow in Sensor Master Mode

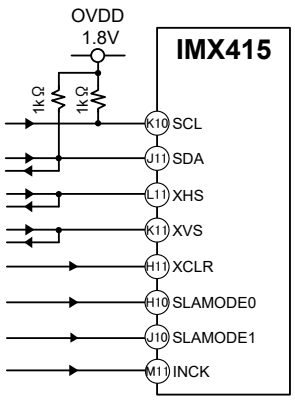
The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time set "master mode stop" by setting XMSTA to "1".

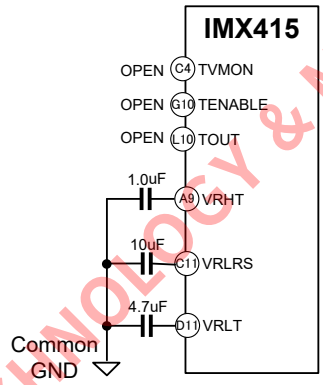


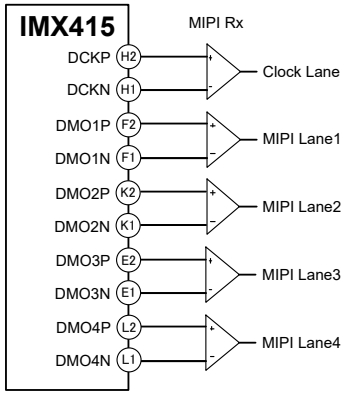
Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit









Application circuits shown are typical examples illustrating the operation of the devices.
Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

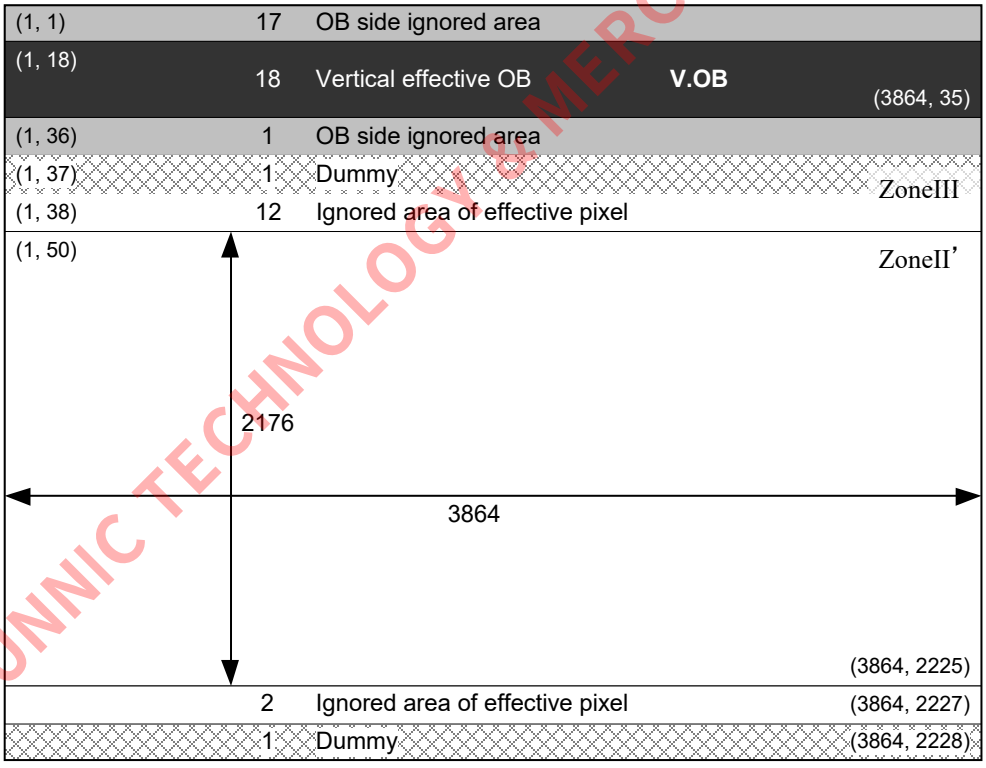
Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	60	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	800		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ 428 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	19 pcs
10.0 mV or higher	10 pcs
24.0 mV or higher	4 pcs
50.0 mV or higher	2 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

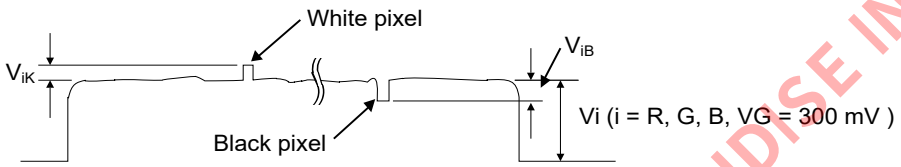
Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 300 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

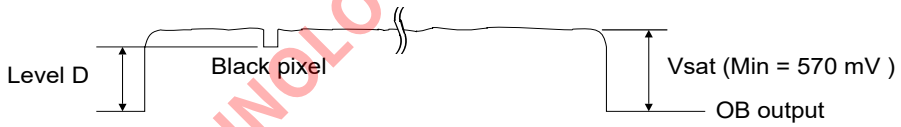
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

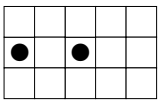
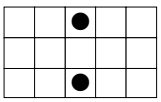


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specification

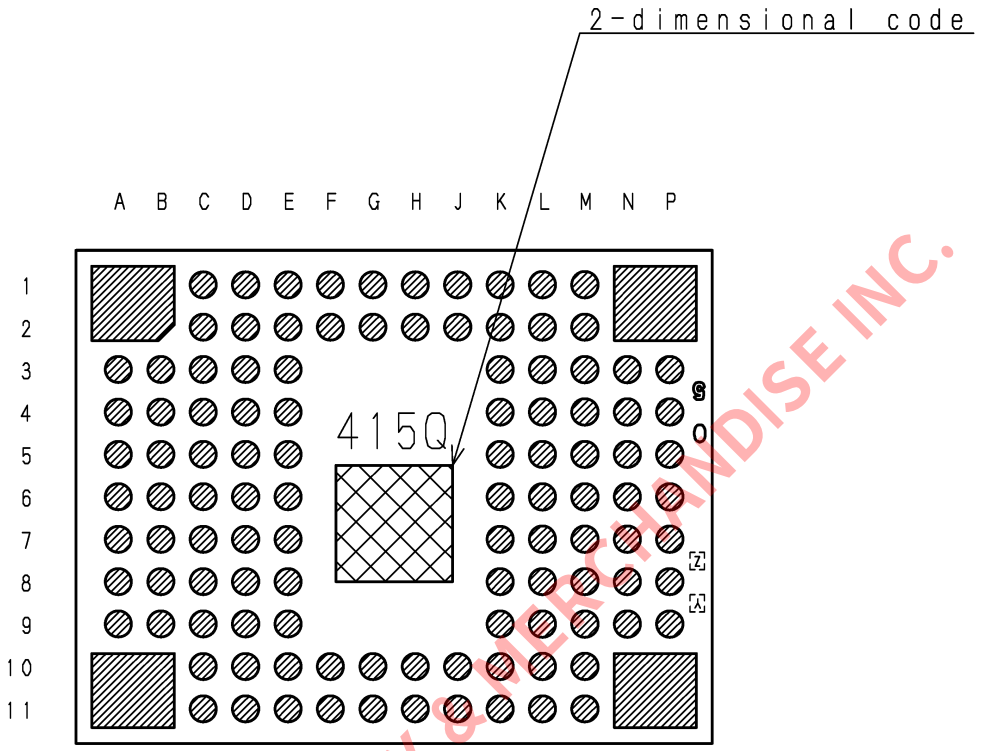
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern (R G / G B)	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1.”●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-C415AAQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

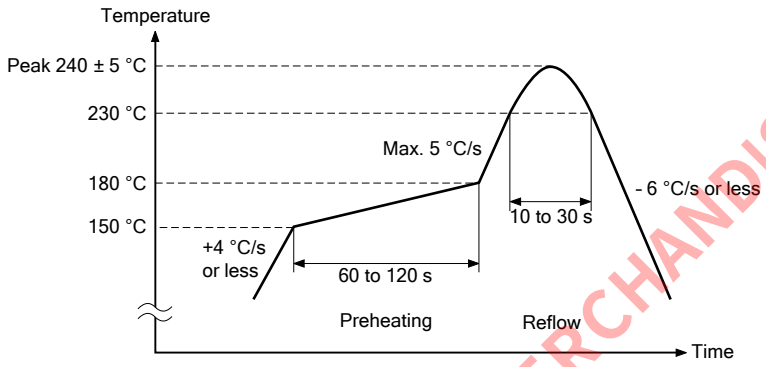
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.
(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

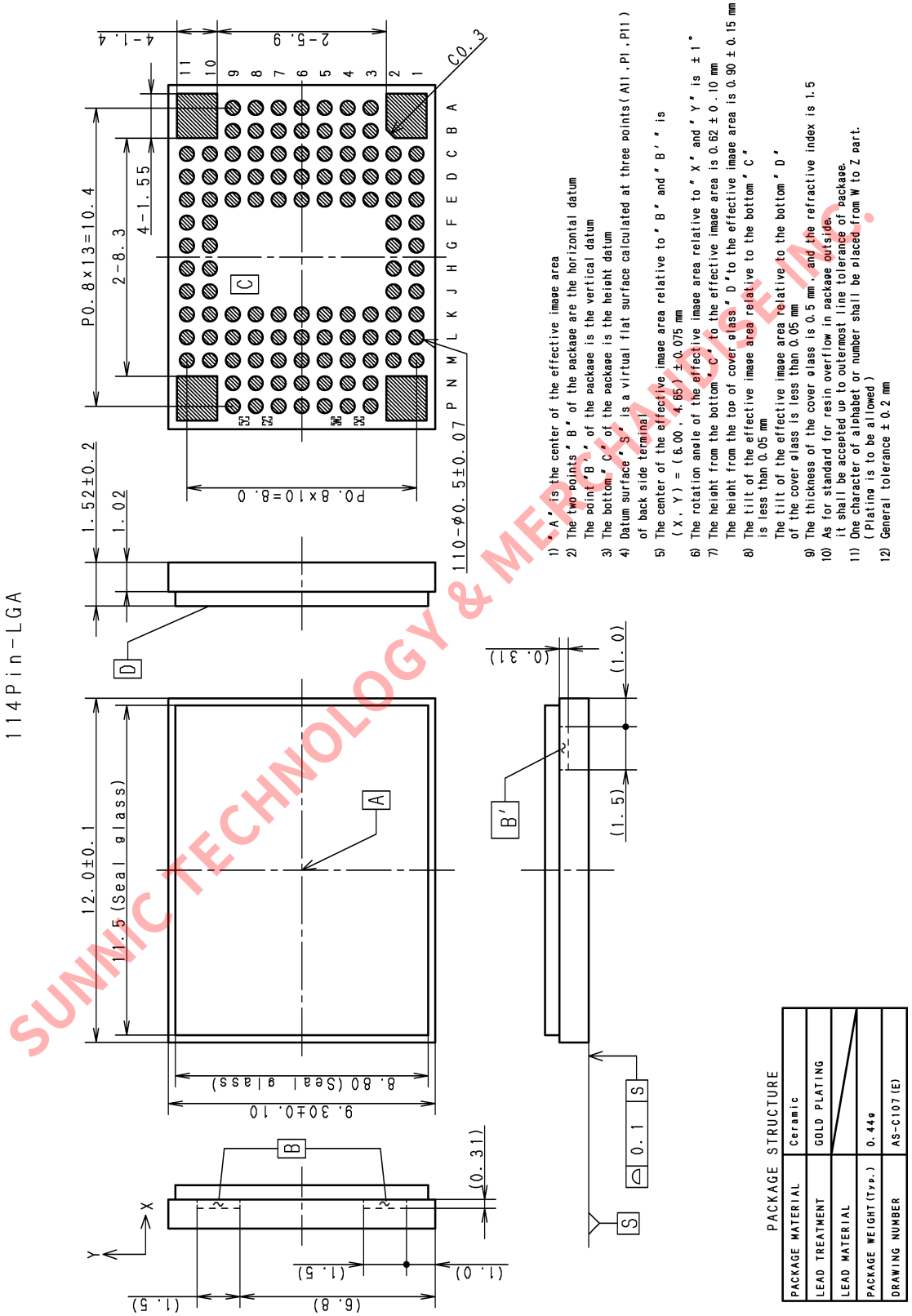
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.
(6) Please perform the tilt adjustment for the optical axis in your company as required.

Package Outline

(Unit: mm)



1) 'A' is the center of the effective image area
2) The two points 'B' of the package are the horizontal datum
   The point 'B' of the package is the vertical datum
3) The bottom 'C' of the package is the height datum
4) Datum surface 'S' is a virtual flat surface calculated at three points (A11, P1, P11) of back side terminal
5) The center of the effective image area relative to 'B' and 'B'' is (X, Y) = (6.00, 4.65) ± 0.075 mm
6) The rotation angle of the effective image area relative to 'X' and 'Y' is ±1°
7) The height from the bottom 'C' to the effective image area is 0.62 ± 0.10 mm
   The height from the top of cover glass 'D' to the effective image area is 0.90 ± 0.15 mm
8) The tilt of the effective image area relative to the bottom 'C' is less than 0.05 mm
   The tilt of the effective image area relative to the bottom 'D' of the cover glass is less than 0.05 mm
9) The thickness of the cover glass is 0.5 mm, and the refractive index is 1.5
10) As for standard for resin overflow in package outside, it shall be accepted up to outermost line tolerance of package.
11) One character of alphabet or number shall be placed from W to Z part. (Plating is to be allowed)
12) General tolerance ± 0.2 mm

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT(Typ.)	0.44g
DRAWING NUMBER	AS-C107(E)

List of Trademark Logos and Definition Statements

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Ver.	Page	Contain of Change
2018 / 08 / 09	0.1	–	First Edition
2018 / 11 / 20	0.2	2	Added: Image size, Diagonal
		8	Correction: Fig. Pixel Arrangement
		10	Correction: Fig. Pin Configuration; Pin name: A7, P9, B7, N9, N5 Pin color: A4, A5, G11, P7, A9
		12	Correction: Pin No. K2; Analog/Digital “—” to D
		13	Correction: Pin No. P7 Description; 1.1V to 1.8V
		14	Deleted: pins SDA, SCL
		27	Correction: Immediately -> “I”, Reconsideration of sentences
		28	Correction: SDL -> SCL
		34	Correction: CPWAIT_TIME; Default Value 0h -> 0B6h WINMODE; Horizontal/Vertical 2/2-line binning setting 1 -> 0
		35, 37, 44	Correction: Reflection timing V -> S HADD, VADD, ADDMODE, ADBIT, MDBIT, ADBIT1
		41, 55, 57	Add: Register DIG_CLP_VSTART, DIG_CLP_VNUM
		42	Correction: Reflection timing V -> I BLKLEVEL
		44, 45	Added: Register address 358Ah, 35A1h, 36BCh, 36CCh-36CEh, 36D0h-36D2h, 36D4h, 36D6h-36D8h, 36DAh, 36DBh, 3724h, 3726h, 3734h, 3736h, 38CCh, 38CDh, 395Ch, 3A4Ch, 3AE0h, 3B00h, 3B06h Deleted: Register address 35A0h
		47	Correction: All pixel 4Lane 720Mbps/lane 12bit; 30.01fps -> 25fps
		49, 54, 59, 60	Correction: Fig. Image Drawing; “FE” position
		53	Correction: [1485Mbps/lane]; TCLKPOST: 0007h -> 00A7h, TCLKTRAIL: 00h5F -> 005Fh [2376Mbps/lane]; 60fps -> 90fps, 7.5us -> 5.0us, HMAX: 226h -> 16Eh, ADBIT/MDBIT: 1h -> 0h, TCLKPOST: 009Fh -> 00E7h, TCLKPREPARE: 0057h -> 008Fh, TCLKTRAIL: 0057h -> 008Fh, TCLKZERO: 0187h -> 027Fh, THSPREPARE: 005Fh -> 0097h, THSZERO: 00A7h -> 010Fh, THSTRAIL: 005Fh -> 0097h, THSEXIT: 0097h -> 00F7h, TLPX: 004F -> 007Fh
		54, 59	Correction: Fig. Drive Timing Chart for All pixel mode, Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binning mode
		65	Correction: 3091h [1] -> [0]
		76 - 78	Correction: bit length SYS_MODE, INCKSEL4, INCKSEL5
		87	Correction: Peripheral Circuit; Pin D11(VRLT) Capacitor value 10uF -> 4.7uF

Date of change	Ver.	Page	Contain of Change
2019 / 02 / 18	0.3	1	Correction: Description, 8.42 M effective pixels -> 8.46 M
		1	Update: Readout rate, CDS/PGA function TBD
		15	Update: Current Consumption
		24	Correction: Color Coding Diagram; added scan direction
		27	Correction: Register Communication Timing, description
		37	Update: SYS_MODE 2376Mbps TBD
		39	Correction: PIX_VWIDTH Description
		40, 66	Update: GAIN_PGC_0 TBD
		43 - 46	Added: Register address 3081h, 32D4h, 32ECh, 3452h, 3453h, 3732h, 3742h, 3862h, 3A42h, 3B98h, 3B99h, 3B9Bh, 3B9Ch, 3B9Dh, 3B9Eh, 3BA1h - 3BA9h, 3BACh - 3BB8h, 3BBAh, 3BBCh, 3BBEh, 3BC0h, 3BC2h, 3BC4h, 3BC8h, 3BCAh
		48	Update: Data rate 2376Mbps/Lane TBD
		50	Correction: MDBIT address
		55	Correction: Fig. Pixel Array Image Drawing in All pixel mode; added read out direction, Fig. Drive Timing Chart; inverted operation
		60	Correction: Fig. Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode; added read out direction, Fig. Drive Timing Chart; 1 XHS/Line -> 2 XHS/Line, inverted operation
		62	Correction: Restriction on Window cropping mode, added V_{TTL}
		63, 86, 87	Update: After standby mode, Time TBD
		66	Correction: Fig. GAIN Reflection Timing, GAIN -> GAIN_PCG_0
		69	Correction: Formula Integration time, added T_{offset}
		71	Update: the maximum of long time exposure TBD
		75	Correction: Fig. Relationship between Pin Name and MIPI Output Lane, DCKM -> DCKN
		80	Correction: Resister Hold Setting
		83	Update: T_{SYNC} TBD
		95	Update: Notes On Handling; added 5. (6)

Date of change	Ver.	Page	Contain of Change
2019 / 03 / 28	0.4	1	Correction: Maximum frame rate, 12bit 60 frame/s -> 60.3, 10bit 90 -> 90.9
		1	Update: List analog and digital gain respectively
		15	Update: Current Consumption
		19 20	Correction: Standard mode, Fast mode -> Standard-mode, Fast-mode ; Fast mode + -> Fast-mode Plus
		22	Update: Spectral Sensitivity Characteristics (TBD)
		23	Update: Image Sensor Characteristics from TBD
		25	Update: Measurement Method 2. 3. 4. from TBD
		25	Correction: Measurement Method 3. measure the average values -> measure the minimum values
		39	Correction: register 3081h Set to “02h” -> Fixed to “00h”
		48, 49	Update: updated to expression of maximum frame rate
		53	Added: frame rate formula
		54, 55, 57, 59	Added: 3500h to 3BFFh -> 3200h to 3BFFh
		63	Correction: 1H period description at Window cropping mode
		73	Correction: Integration time, added T_{offset}
		77	Correction: Output Signal Range Deleted “but output is not performed over the full range,”
		78	Added: the initial deskew burst
		90	Update: Spot Pixel Specifications from TBD
		91	Update: Example of Annual Number of Occurrence from TBD
		92	Correction: Measurement Method for Spot Pixels Incorrect form corrected Update: Measurement Method for Spot Pixels from TBD mV
2019 / 05 / 21	E19504	–	First Edition (Official Edition)
		7	Update: Optical Center tolerance from TBD
		22	Update: Spectral Sensitivity Characteristics from TBD
		24	Correction: Measurement Condition 2. Sentence reconsidered
		27	Correction: Description and figure of “communication prohibited period”
		62	Correction: Description and figure of inverted mode
		63	Correction: 1farame -> 1frame
		64	Correction: a normal image is output from the 8 frames -> 9 frames
		67	Added: Gain graph
		94	Update: Marking from TBD
		97	Update: Package Outline from TBD