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Description

Note

Option

Generate Bill of Materials

Header:
 Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

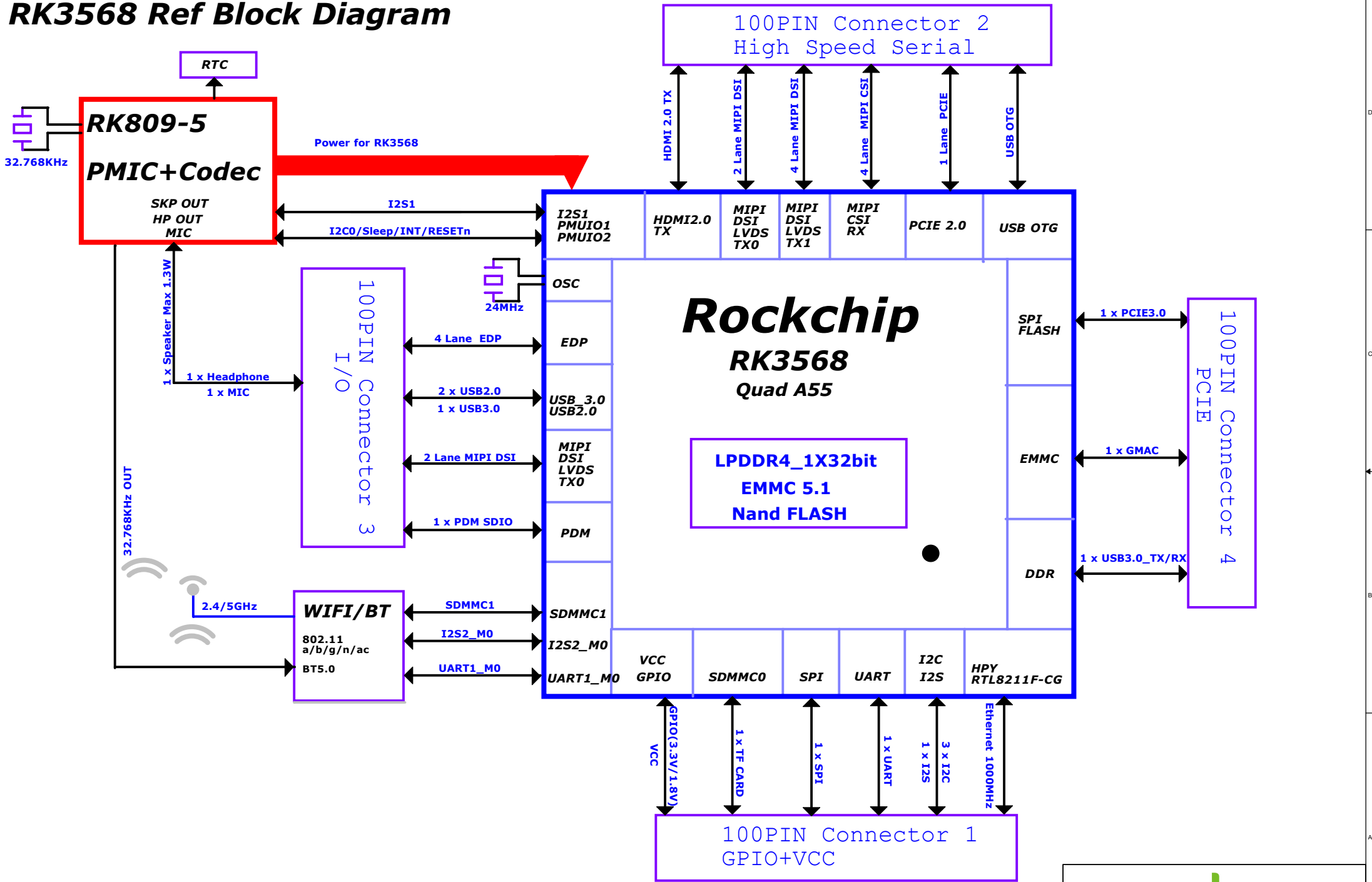
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Notes

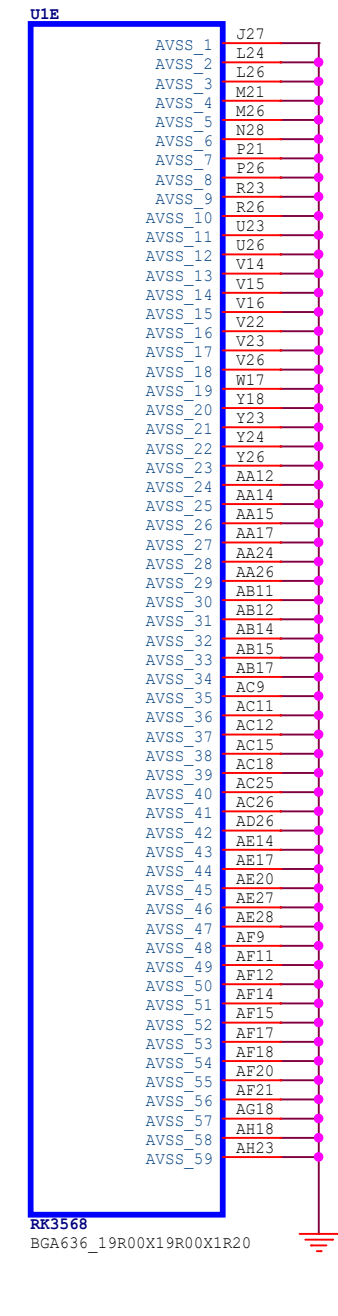
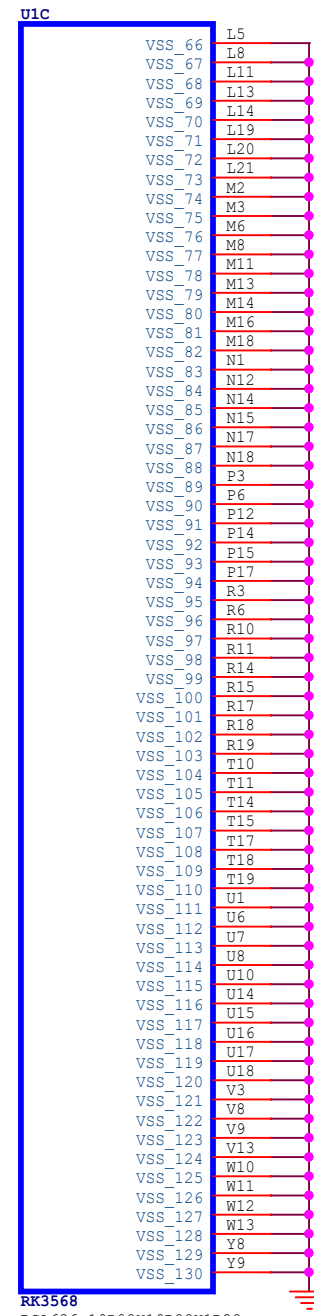
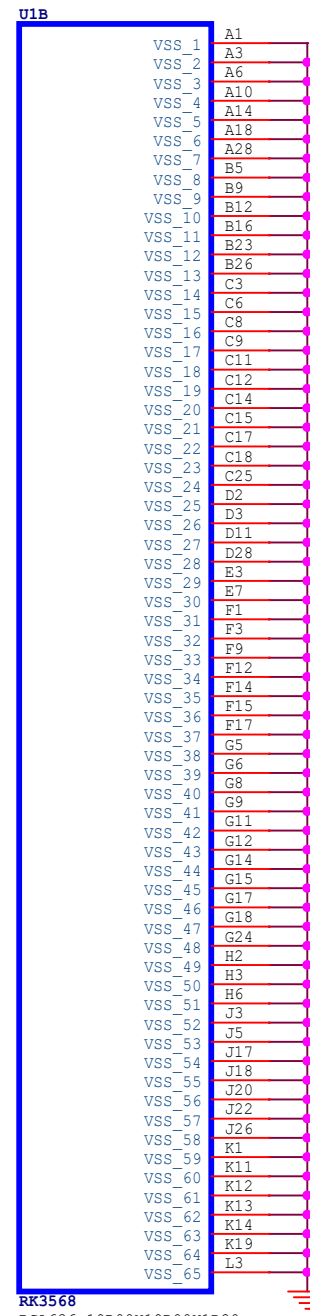
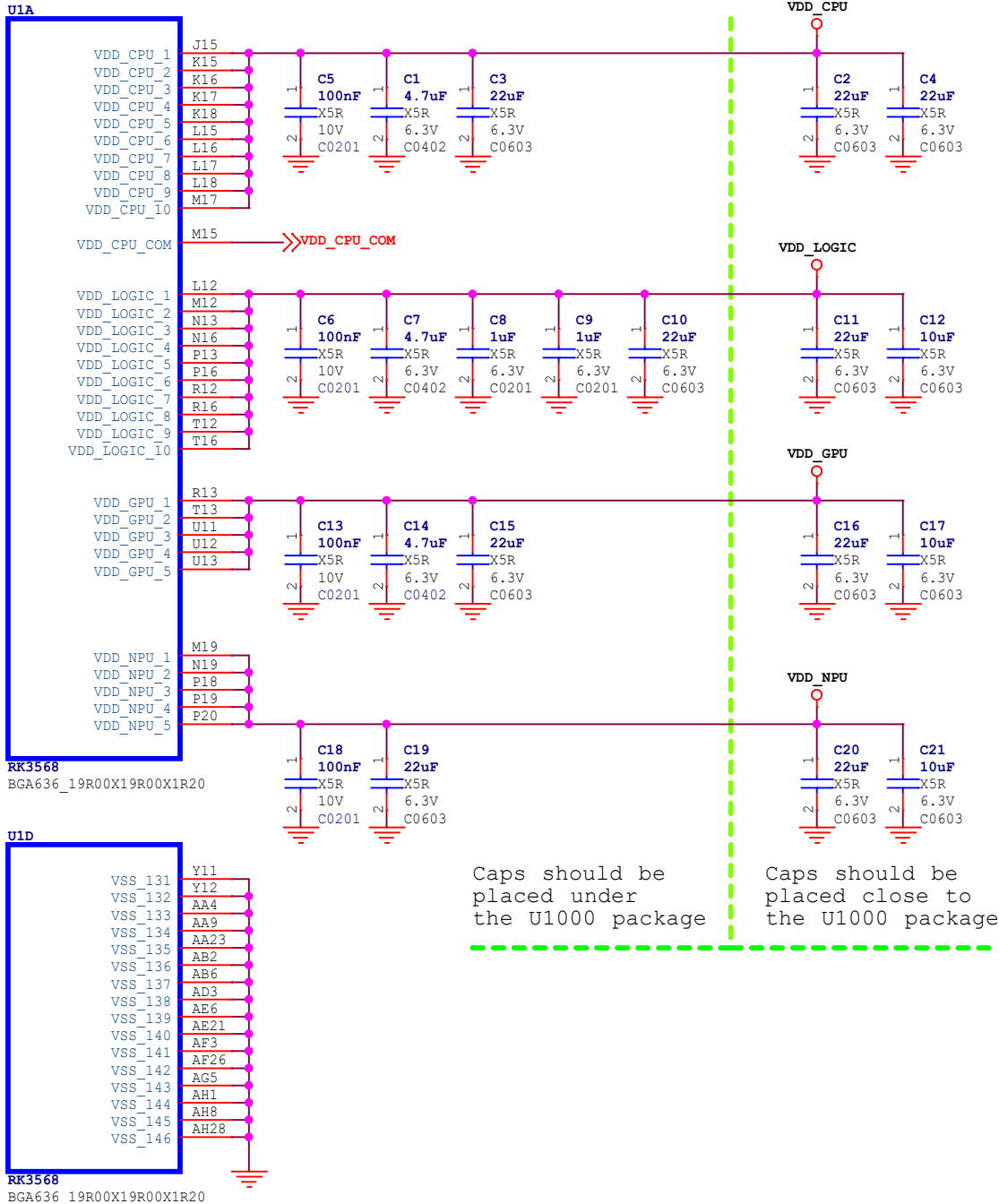
NOTE 1:
 Component parameter description
 1. DNP stands for component not mounted temporarily
 2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
 Please use our recommended components to avoid too many changes.
 For more informations about the second source,please refer to our AVL.

RK3568 Ref Block Diagram



RK3568_ABCDE (Power&Gnd)



radxa

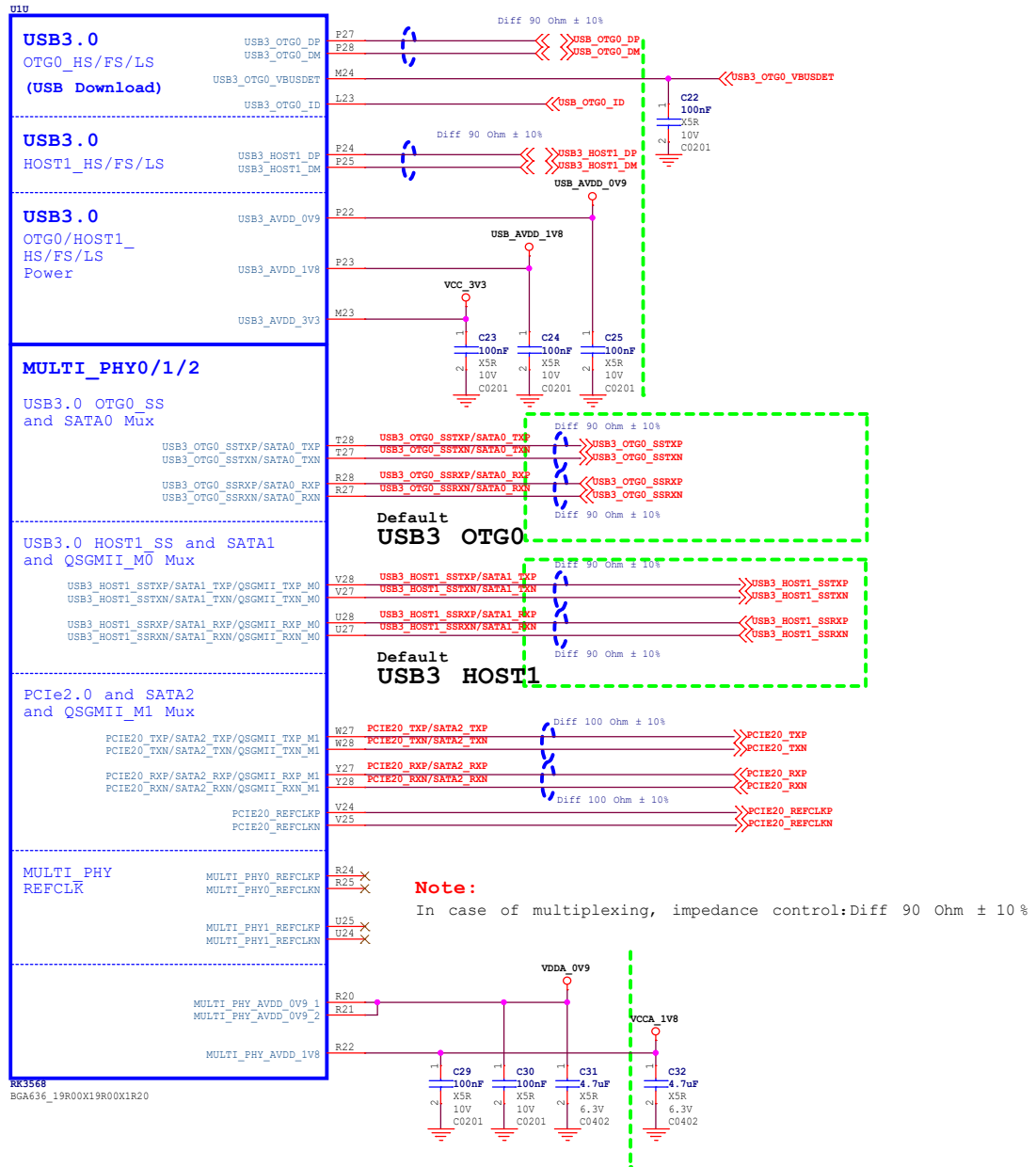
Rock 3 Compute Module Plus

Size: A4 | Title: Rock 3 Compute Module Plus | REV: V1.1

Page Name: RK3568_Power/GND

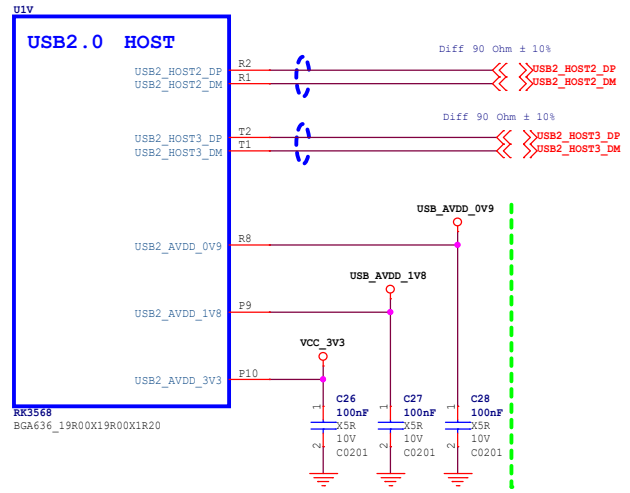
Date: Tuesday, November 16, 2021 | Sheet: 04 of 25

RK3568_U (USB3.0/SATA/QSGMII/PCIE2.0 x1)

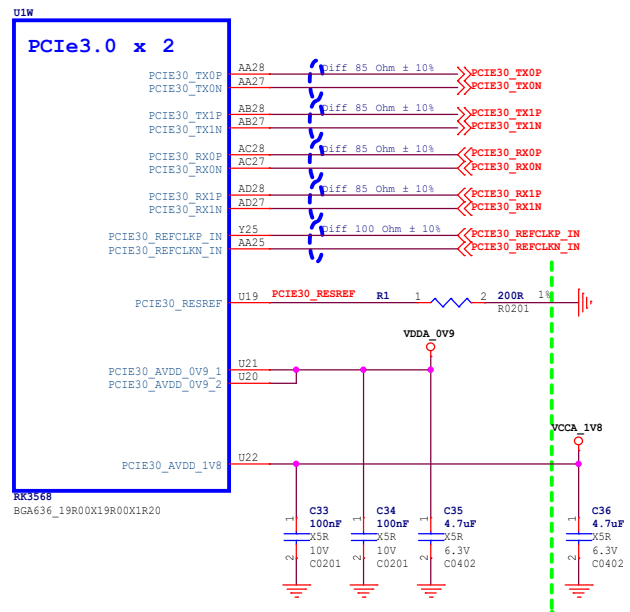


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

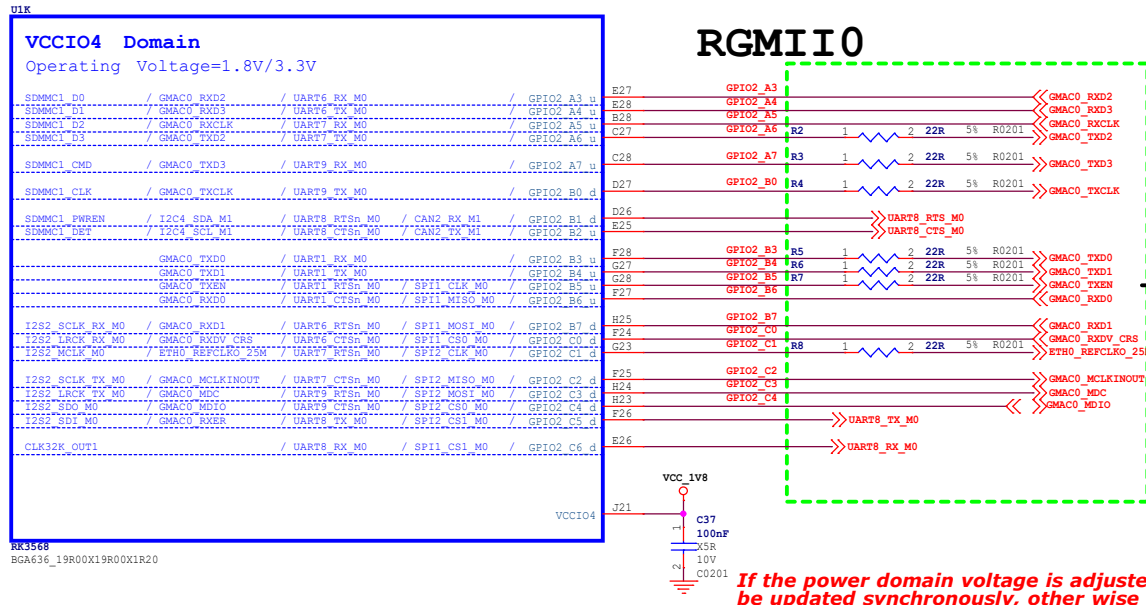
RK3568_V (USB2.0 HOST)



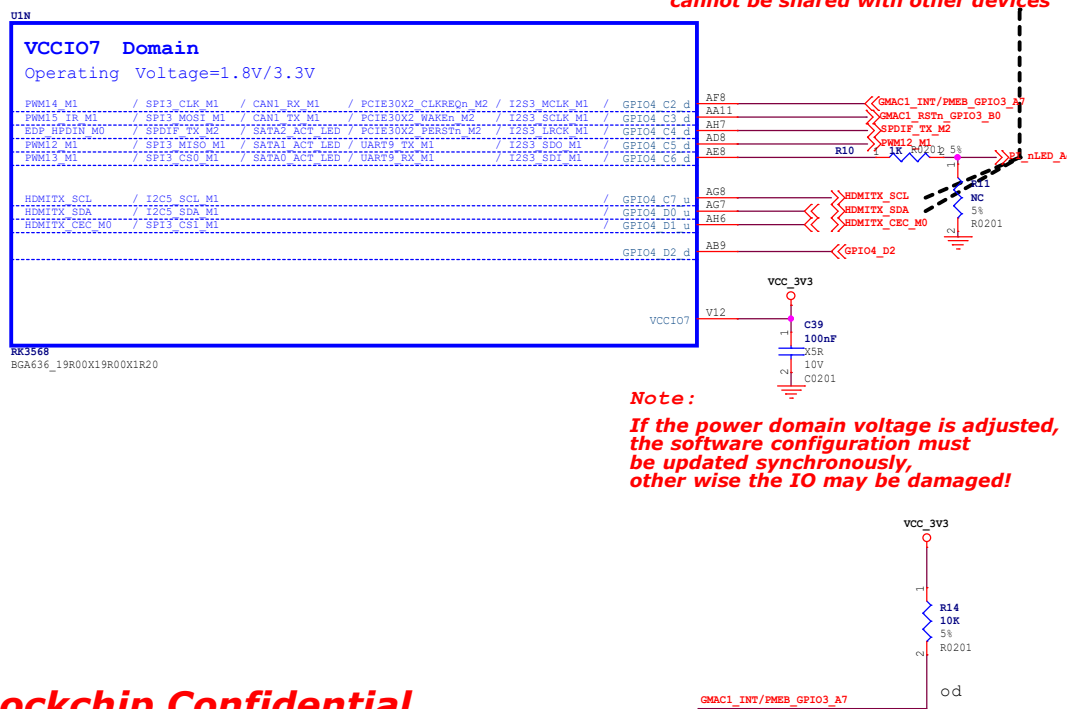
RK3568_W (PCIE3.0 x2)



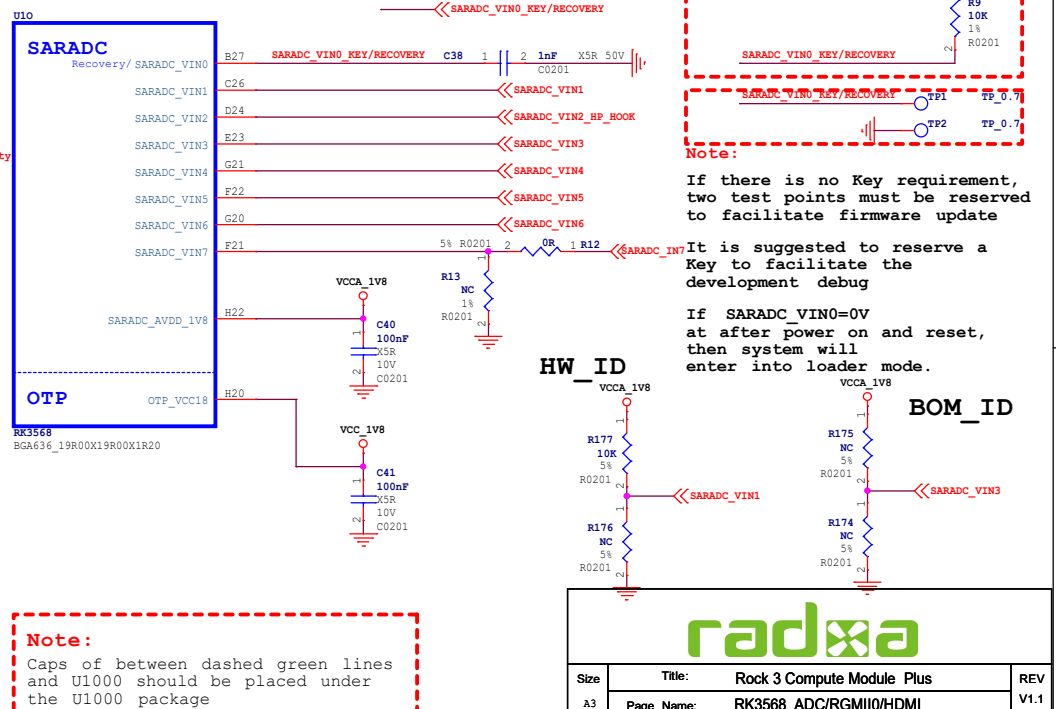
RK3568_K (VCCIO4 Domain)



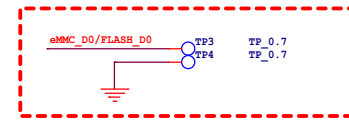
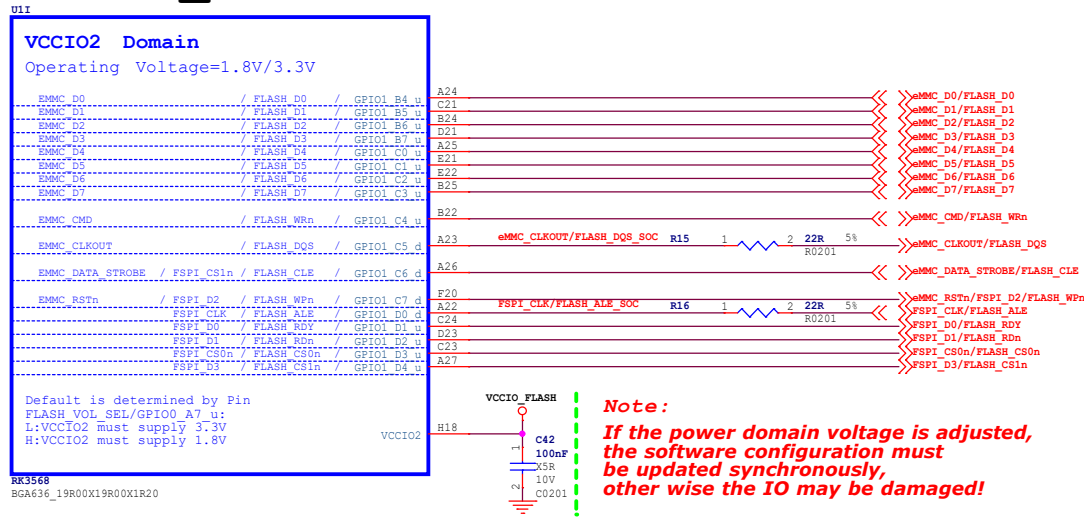
RK3568_N (VCCIO7 Domain)



RK3568_O (SARADC/OTP)



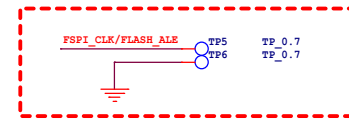
RK3568_I (VCCIO2 Domain)



Note:
For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



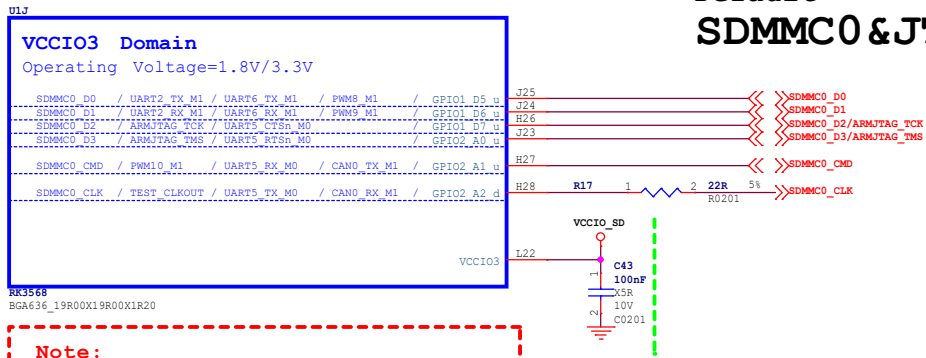
Note:
For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

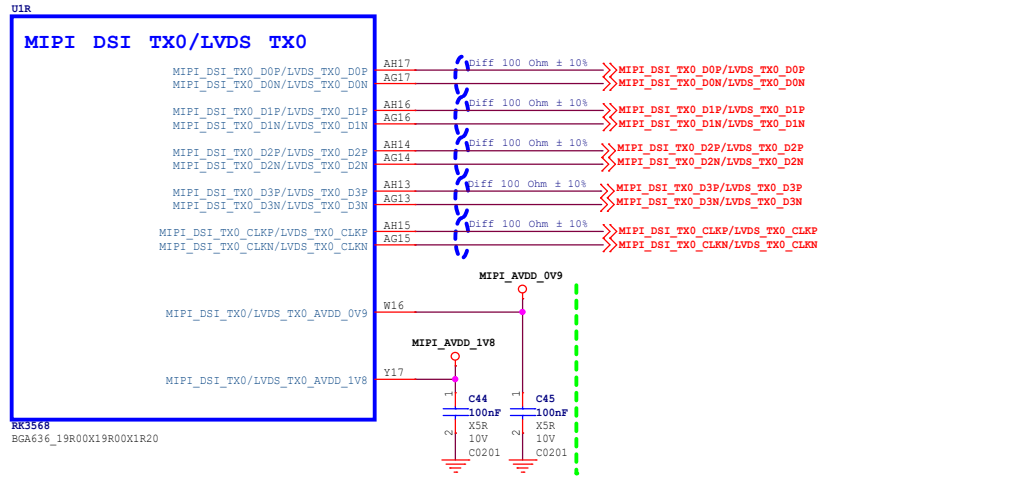
RK3568_J (VCCIO3 Domain)

Default SDMMC0 & JTAG

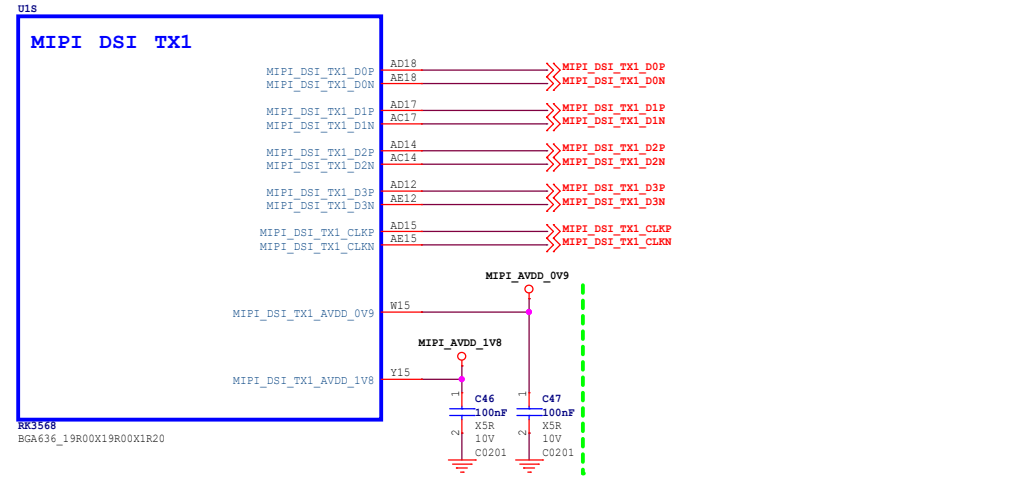


Size:	Title: Rock 3 Compute Module Plus	REV
A3	Page Name: RK3568_Flash/SD Controller	V1.1
Date: Tuesday, November 16, 2021	Sheet	07 of 25

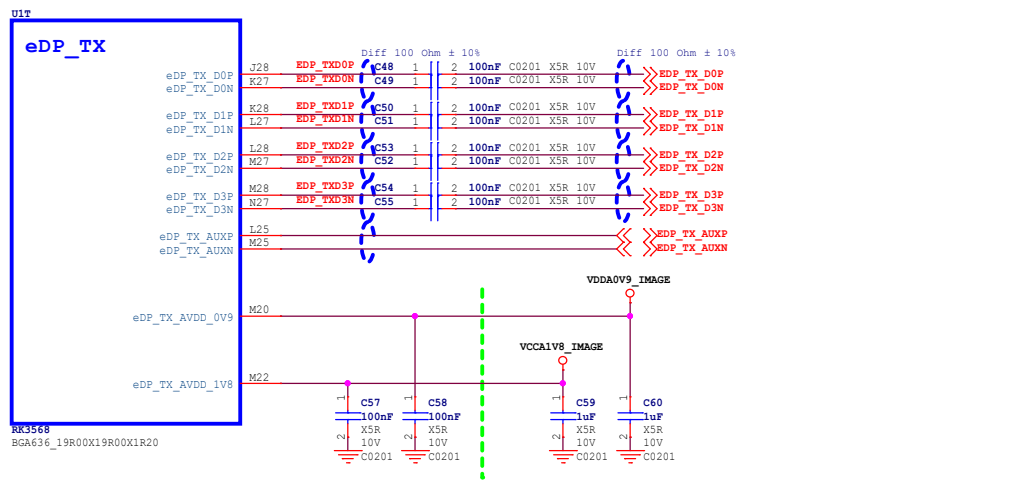
RK3568_R (MIPI_DSI_TX0/LVDS_TX0)



RK3568_S (MIPI_DSI_TX1)

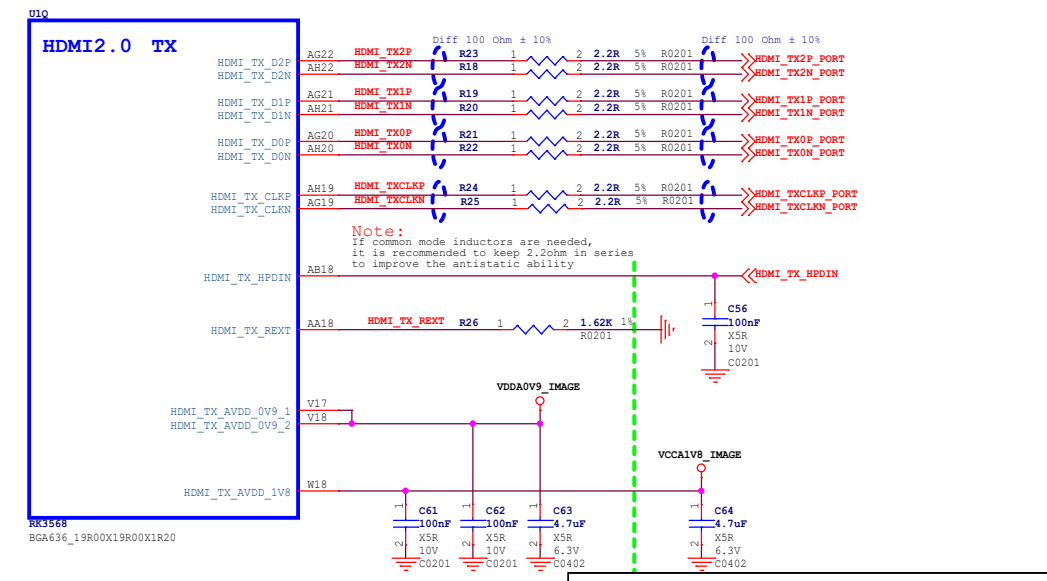


RK3568_T (eDP TX)



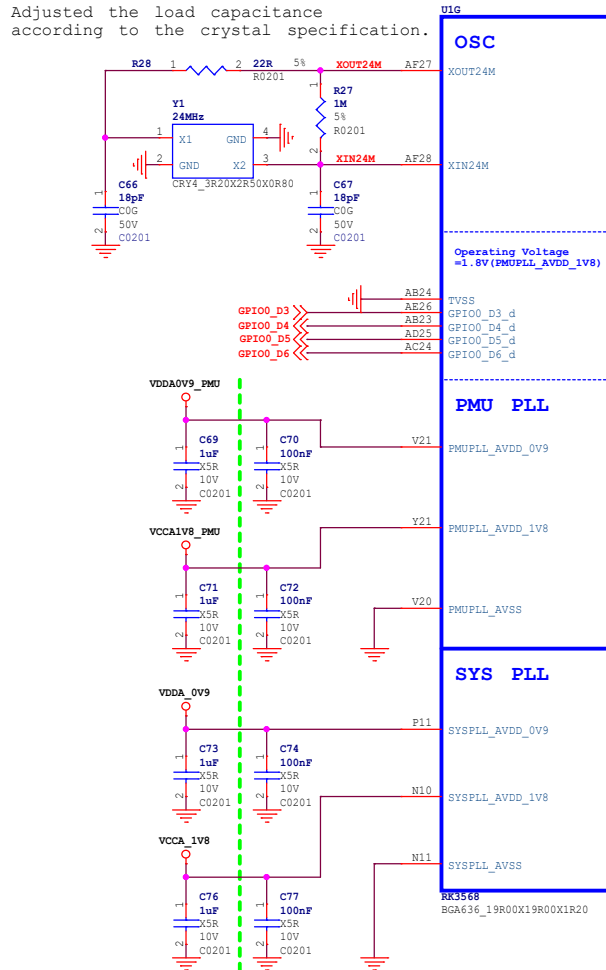
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

RK3568_Q (HDMI2.0 TX)

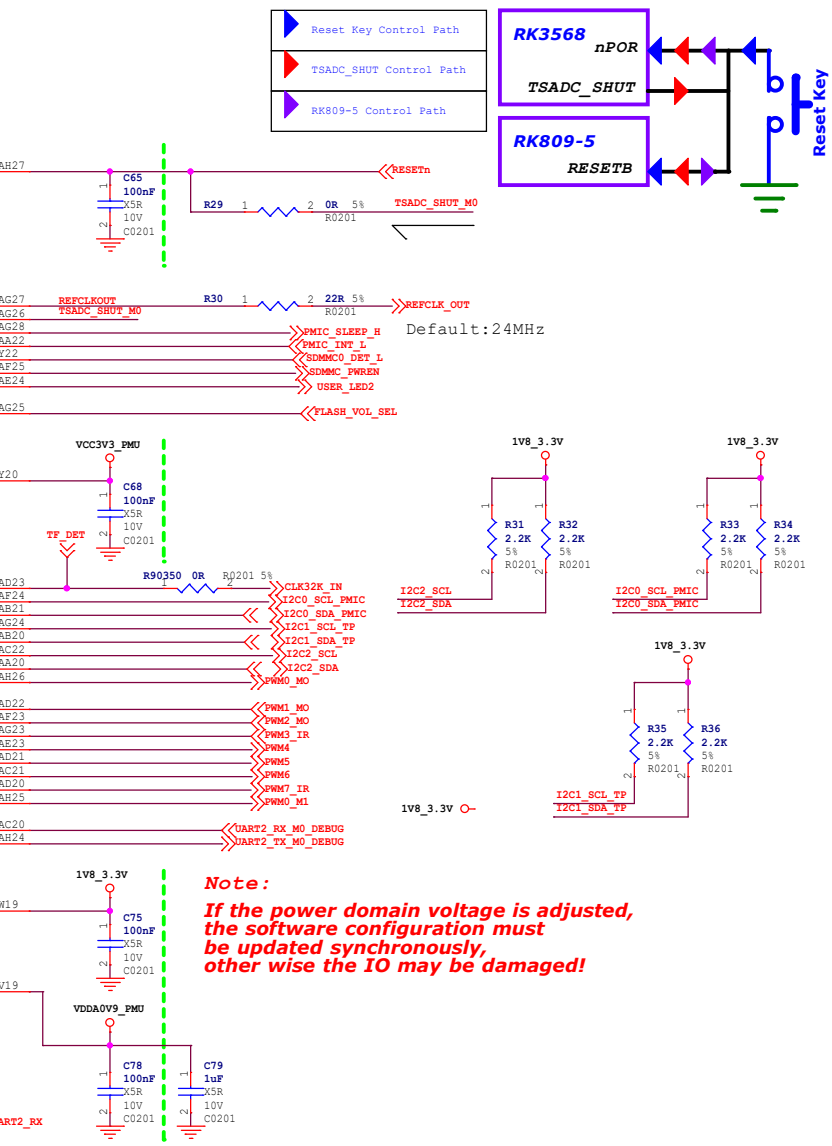
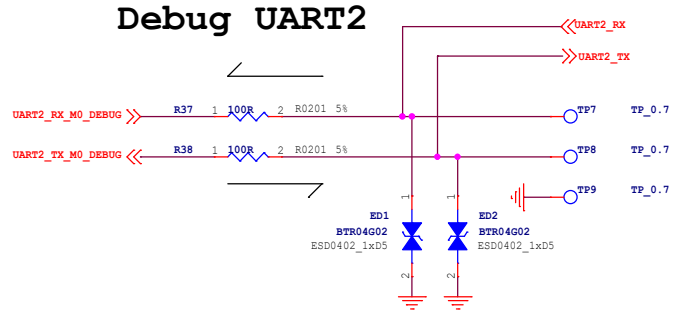
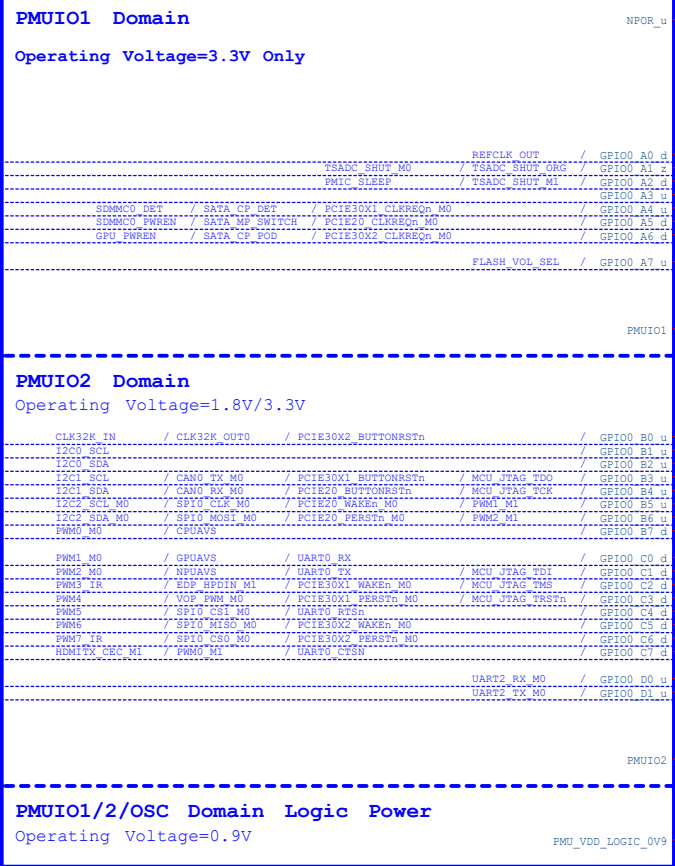


RK3568_G (OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification.



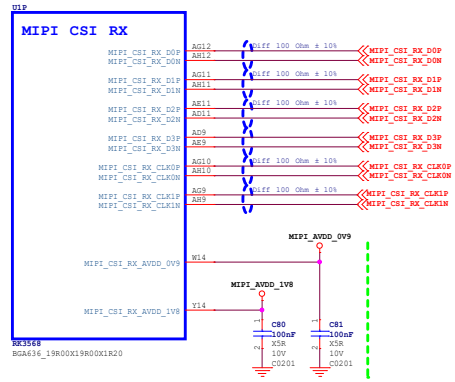
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package



Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

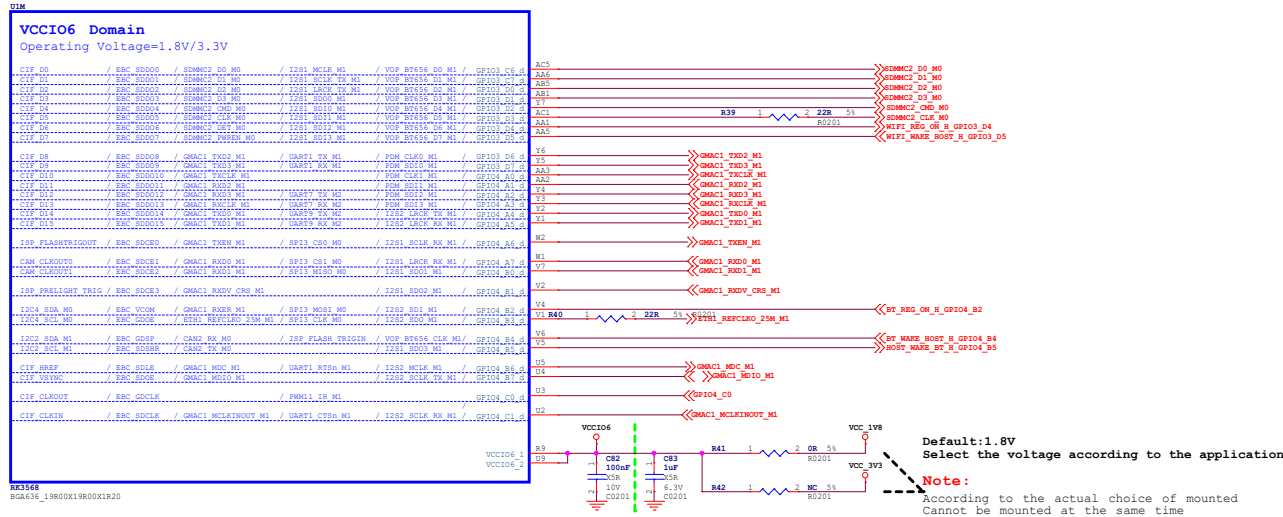
Size	Title: Rock 3 Compute Module Plus	REV
A3	Page Name: RK3568_OSC/PLL/PMUIO	V1.1
Date: Tuesday, November 16, 2021	Sheet 09	of 25

RK3568_P (MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M (VCCIO6 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Camera MCLK can select the following clock:
1: CAM_CLKOUT0
2: CAM_CLKOUT1
3: CIF_CLKOUT
4: REFCLK_OUT

Attention to the voltage matching

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input
BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7, D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7, D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	----->	PHYx_TXD0	GMACx_TXD0	----->	PHYx_TXD0
GMACx_TXD1	----->	PHYx_TXD1	GMACx_TXD1	----->	PHYx_TXD1
GMACx_TXD2	----->	PHYx_TXD2			
GMACx_TXD3	----->	PHYx_TXD3			
GMACx_TXEN	----->	PHYx_TXEN	GMACx_TXEN	----->	PHYx_TXEN
GMACx_TXCLK	----->	PHYx_TXCLK			
GMACx_RXD0	<-----	PHYx_RXD0	GMACx_RXD0	<-----	PHYx_RXD0
GMACx_RXD1	<-----	PHYx_RXD1	GMACx_RXD1	<-----	PHYx_RXD1
GMACx_RXD2	<-----	PHYx_RXD2			
GMACx_RXD3	<-----	PHYx_RXD3			
GMACx_RXDV	<-----	PHYx_RXDV	GMACx_RXDV	<-----	PHYx_RXDV
GMACx_RXCLK	<-----	PHYx_RXCLK			
GMACx_RXER	<-----		GMACx_RXER	<-----	PHYx_RXER
GMACx_MDC	----->	PHYx_MDC	GMACx_MDC	----->	PHYx_MDC
GMACx_MDIO	<-----	PHYx_MDIO	GMACx_MDIO	<-----	PHYx_MDIO
ETHx_REFCLK0_25M	----->	PHYx_XTALIN			
GMACx_MCLKINOUT	<-----	PHYx_XTALIN/REFCLK	GMACx_MCLKINOUT	<-----	PHYx_XTALIN/REFCLK
GPIO	----->	PHYx_RSTn	GPIO	----->	PHYx_RSTn
GPIO	<-----	PHYx_INT/PMBE	GPIO	<-----	PHYx_INT/PMBE

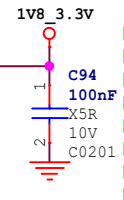
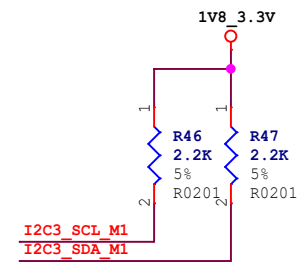
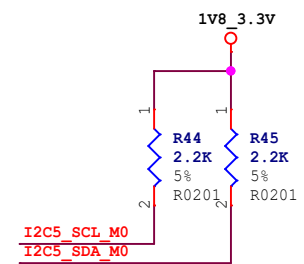
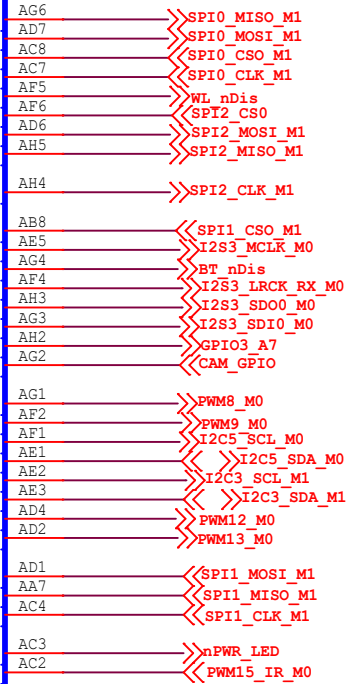
RK3568_L (VCCIO5 Domain)

U1L

VCCIO5 Domain

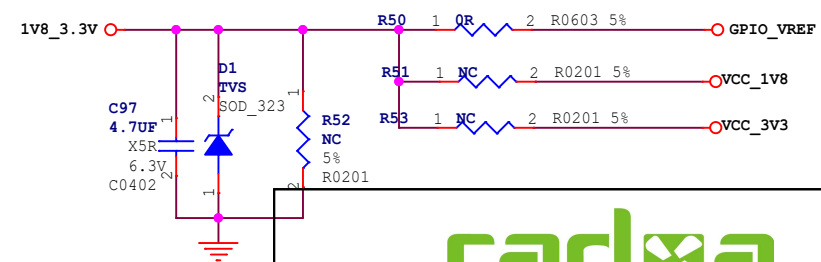
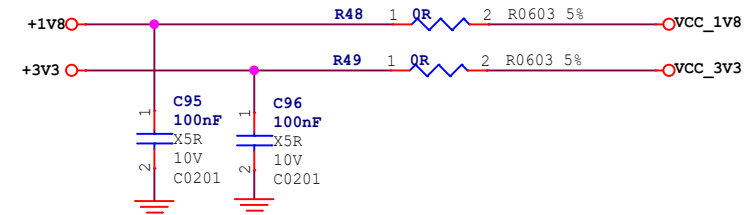
Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEN_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEN_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEN_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0	/ I2S3_SDI0_M0	/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLK0_25M_M0	/ I2S3_SDI1_M0	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART5_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART5_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPBDF_TX_M1	/ GMAC1_MDI0_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d




Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568
BGA636_19R00X19R00X1R20



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

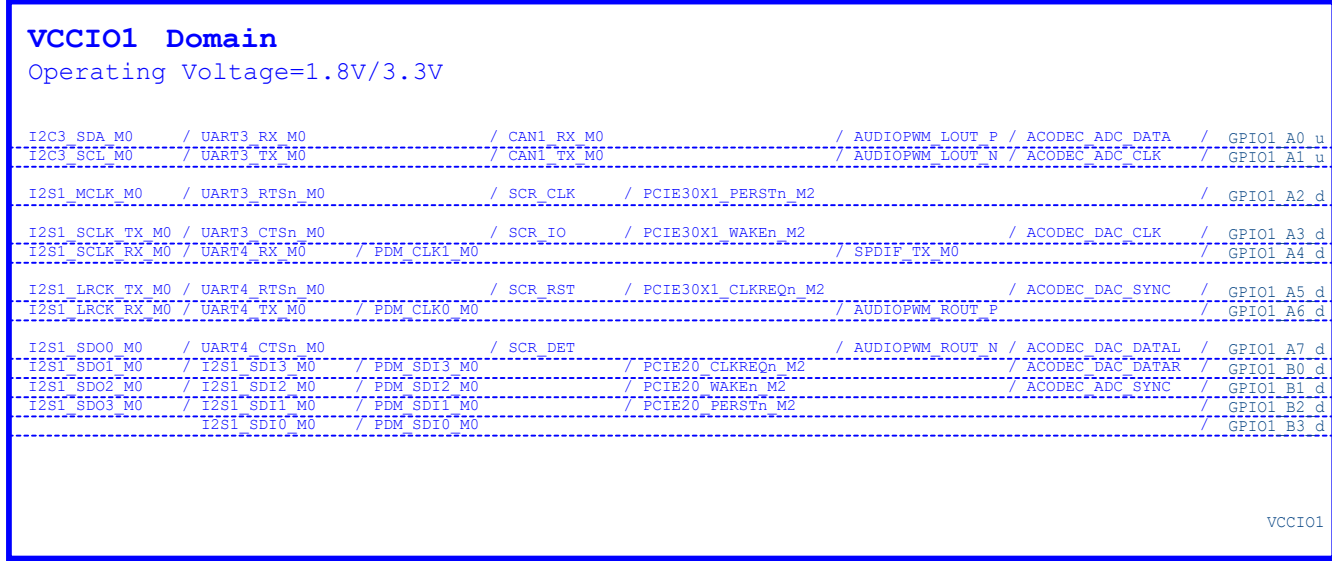
Rockchip Confidential



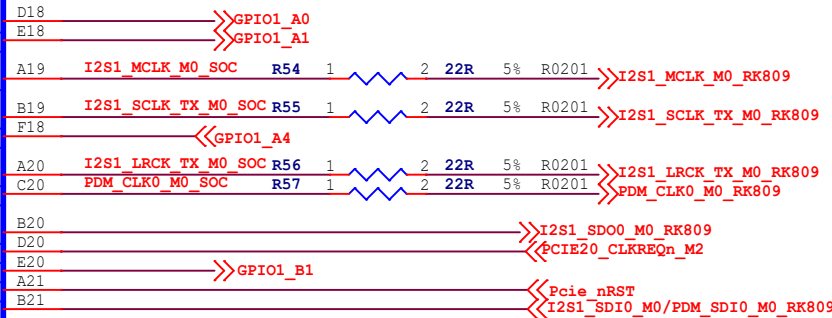
Size	Title: Rock 3 Compute Module Plus	REV
A4	Page Name: RK3568_GPIO2_GPIO3	V1.1
Date: Tuesday, November 16, 2021	Sheet 12 of 25	

RK3568_H (VCCIO1 Domain)

U1H



RK3568
BGA636_19R00X19R00X1R20




VCCIO_ACODEC Default 3.3V

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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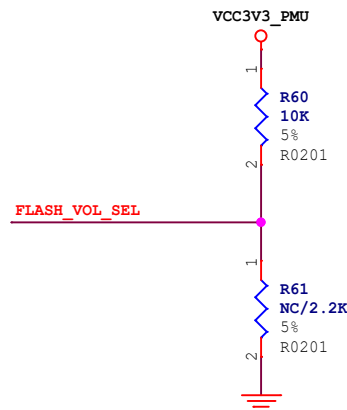
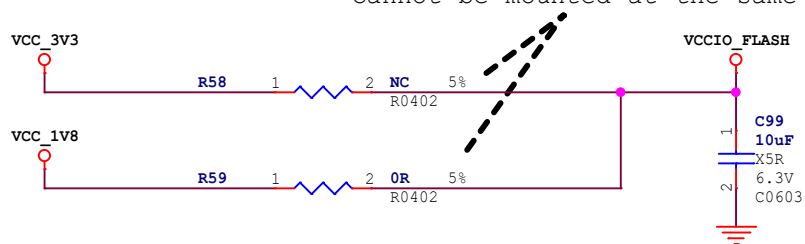
Size	Title: Rock 3 Compute Module Plus	REV
A4	Page Name: RK3568_Audio	V1.1
Date:	Tuesday, November 16, 2021	Sheet 13 of 25

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

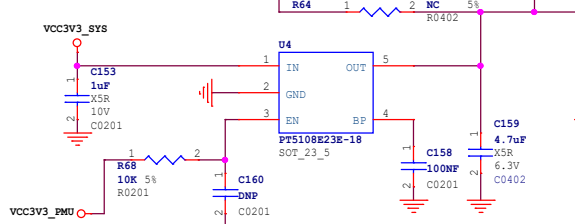
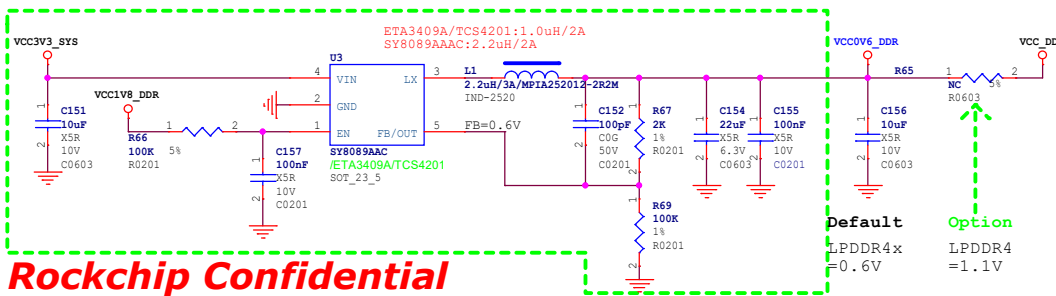
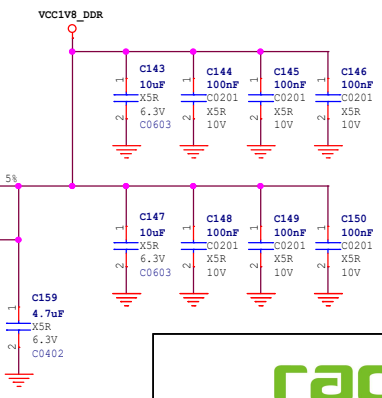
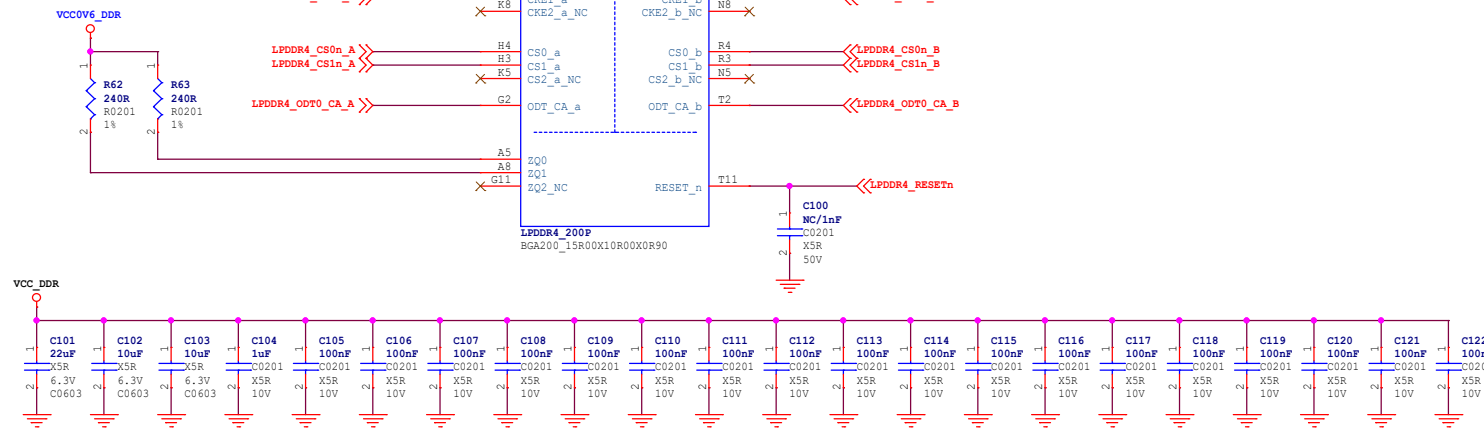
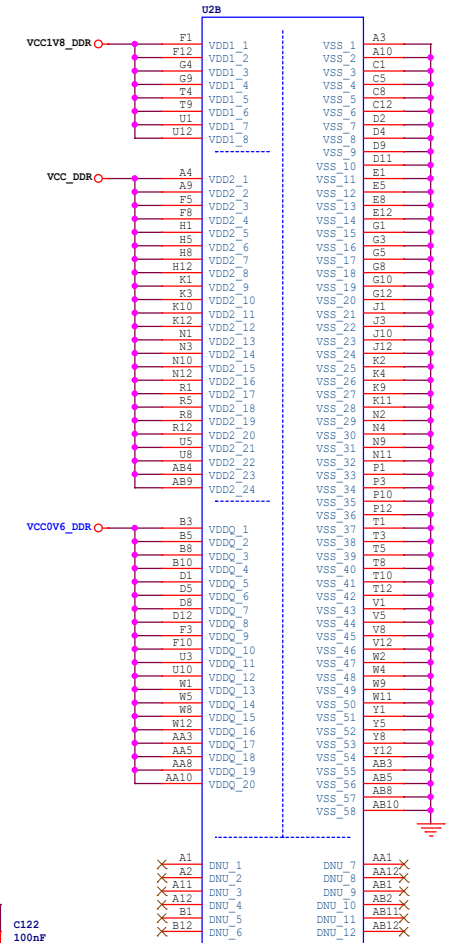
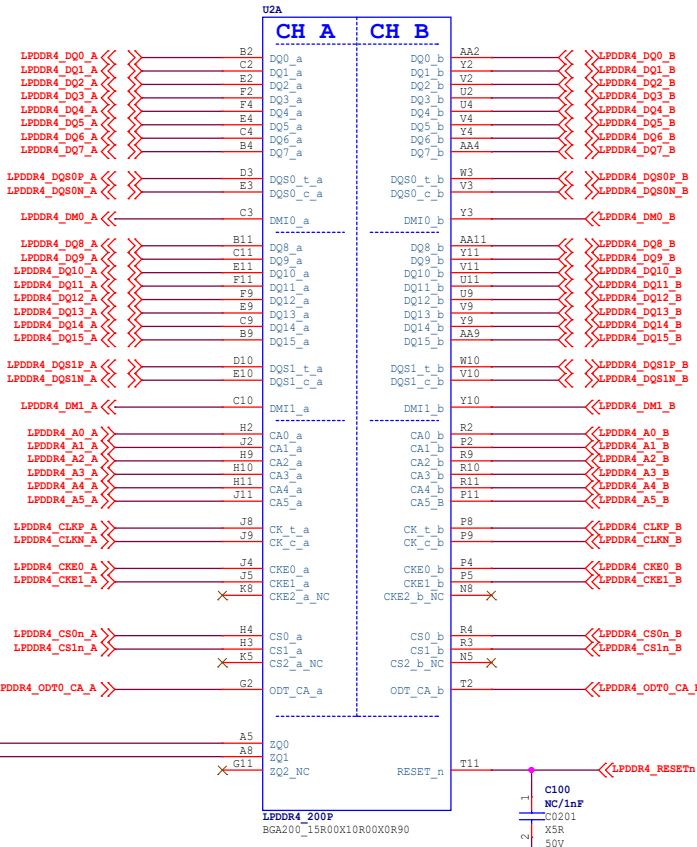
Note:

According to the actual choice of mounted
Cannot be mounted at the same time



Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven





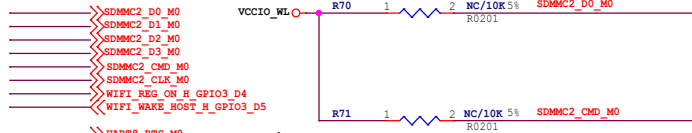
radxa

Size	Title: Rock 3 Compute Module Plus	REV
A3	Page Name: DRAM-LPDDR4X_1X32bit_200P	V1.1
Date: Tuesday, November 16, 2021	Sheet 15	of 25

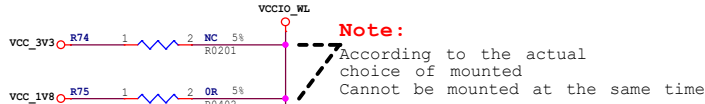
Rockchip Confidential

SDIO WIFI/BT MODULE

And Giga PHY0 Option

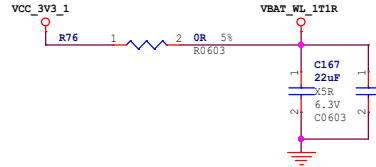


Note:
If ultra low standby power consumption is required, please contact RK to reallocate GPIO and Power

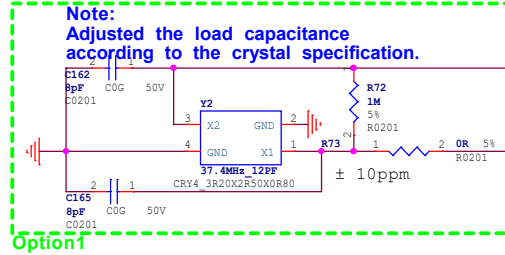


Note:
According to the actual choice of mounted Cannot be mounted at the same time

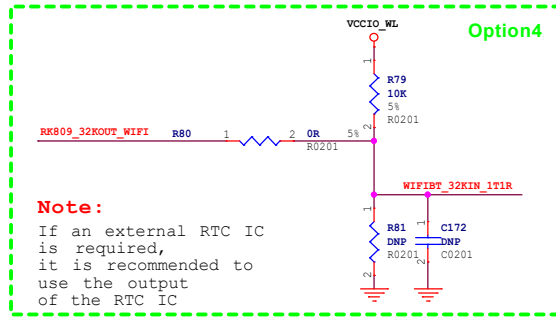
Please choose IO voltage values according to the real mounted module and modify the corresponding software configuration.



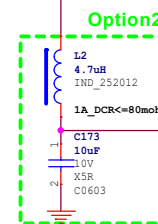
The maximum peak current is 600mA Close to WIFI module



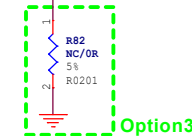
Option1



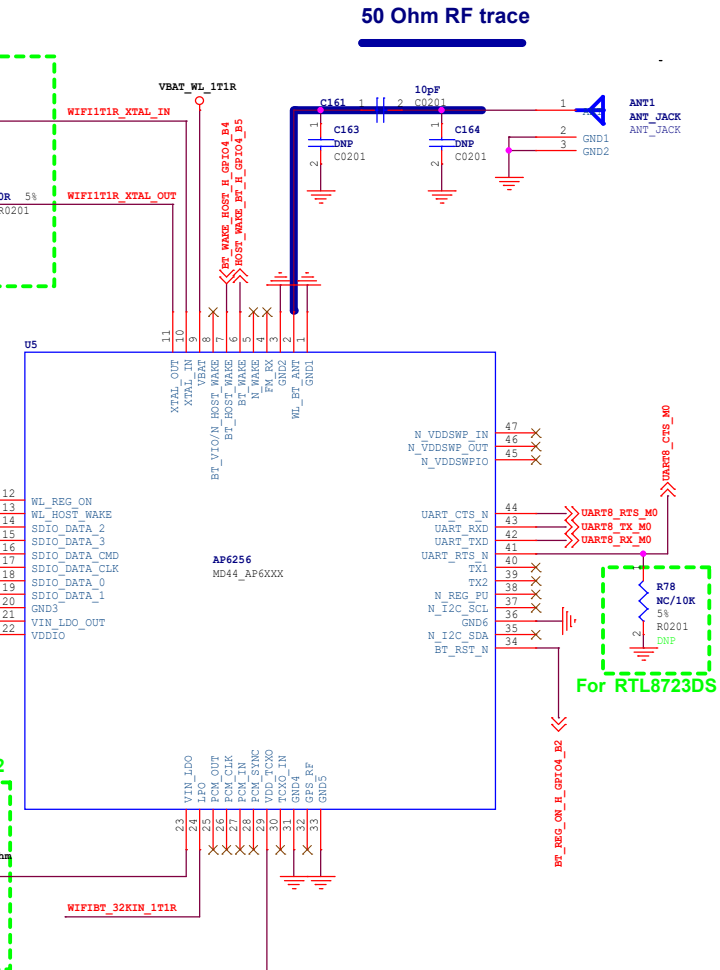
Note:
If an external RTC IC is required, it is recommended to use the output of the RTC IC



Option2



Option3



50 Ohm RF trace

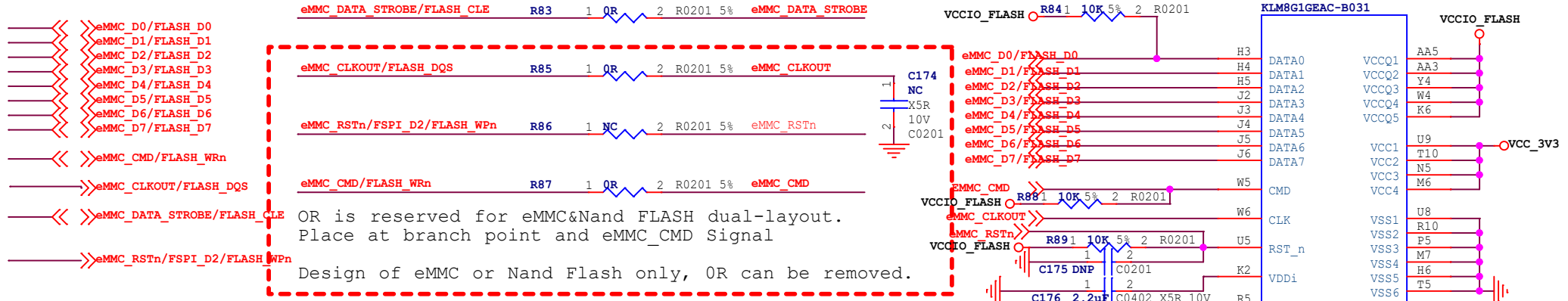
For RTL8723DS

Using RTL8189ETV/FTV modules, please notice WIFI REG ON is on pin12 or pin34, choose according to the actual condition.

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

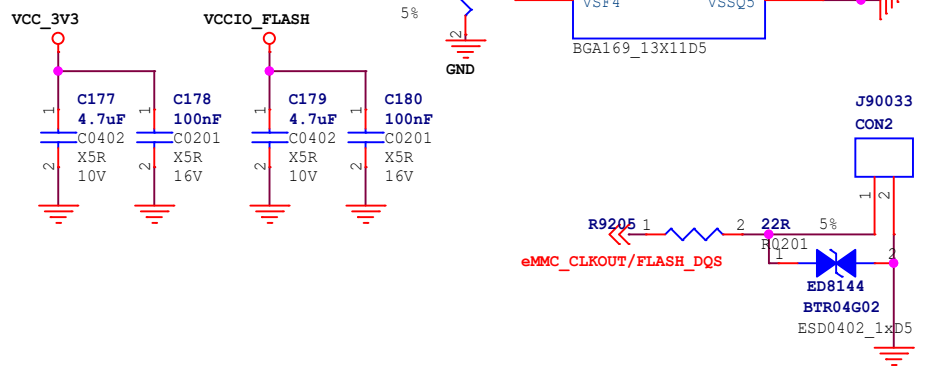
OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

eMMC FLASH



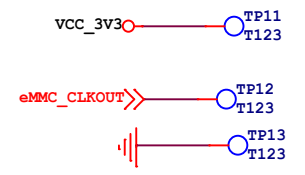
A4	NC0	AH11	NC138	NC137	AH9	NC136	NC135	AG13	NC134	AG2	NC133	AE14	NC132	AE1	AA14	NC131	AA13	NC129	AA12	NC128	AA11	NC127	AA10	NC126	AA9	NC125	AA8	NC124	AA7	NC123	AA2	NC122	AA1	Y14	NC121	Y13	NC120	Y12	NC119	Y11	NC118	Y10	NC117	Y9	NC116	Y8	NC115	Y7	NC114	Y6	NC113	Y3	NC112	Y1	NC111	Y1	NC110	W14	NC109	W13	NC108	W12	NC107	W11	NC106	W10	NC105	W9	NC104	W8	NC103	W7	NC102	W3	NC101	W2	NC100	W1	NC99	V14	NC98	V13	NC97	V12	NC96	V3	NC95	V2	NC94	V1	NC93	U14	NC92	U13	NC91	U12	NC88	U7	NC87	U6	NC85	U3	NC84	U2	NC83	T14	NC82	T13	NC81	T12	NC80	T3	NC78	T2	NC77	T1	NC76	R14	NC75	R13	NC74	R12	NC73	R3	NC71	R2	NC70	R1	NC69	R1	NC68	R1	NC67	P14	NC66	P13	NC65	P12	NC64	P10	NC63	P3	NC62	P2	NC61	P1	NC60	N14	NC59	N13	NC57	N3	NC56	N2	NC55	N1	NC54	M14	NC53	M13	NC52	M12	NC49	M8	NC48	M5	NC47	M3	NC46	M2	NC45	M1	NC44	L14	NC43	L13	NC42	L12	NC41	L3	NC40	L2	NC39	L1	NC38	K14	NC37	K13	NC36	K12	NC35	K11	NC34	K10	NC33	K9	NC32	K8	NC31	K7	NC30	K5	NC29	K3	NC28	K1	NC27	J14	NC26	J13	NC25	J12	NC24	J11	NC23	J10	NC22	J9	NC21	J8	NC20	J7	NC19	J1	NC18	H14	NC17	H13	NC16	H12	NC15	H11	NC14	H10	NC13	H9	NC12	H8	NC11	H7	NC9	H2	NC8	H1	NC7	D14	NC6	D1	B13	NC4	B2	NC3	A11	NC2	A9	NC1	A6	NC0	A4	AH11	NC34	K10	NC33	K9	NC32	K8	NC31	K7	NC30	K5	NC29	K3	NC28	K1	NC27	J14	NC26	J13	NC25	J12	NC24	J11	NC23	J10	NC22	J9	NC21	J8	NC20	J7	NC19	J1	NC18	H14	NC17	H13	NC16	H12	NC15	H11	NC14	H10	NC13	H9	NC12	H8	NC11	H7	NC9	H2	NC8	H1	NC7	D14	NC6	D1	B13	NC4	B2	NC3	A11	NC2	A9	NC1	A6	NC0	A4	AH11
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U6B
KLM8G1GEAC-B031
BGA169_13X11D5

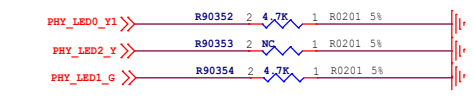
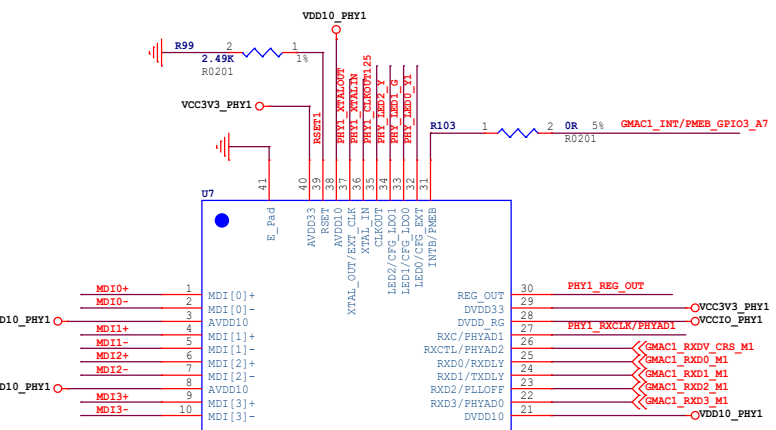
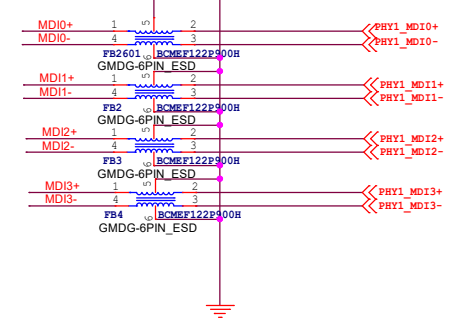
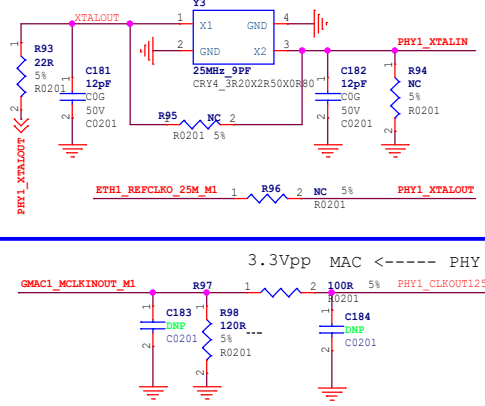
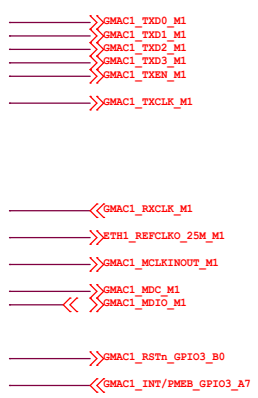


Note: All the Power filter capacitors should be placed close to the power pins of eMMC

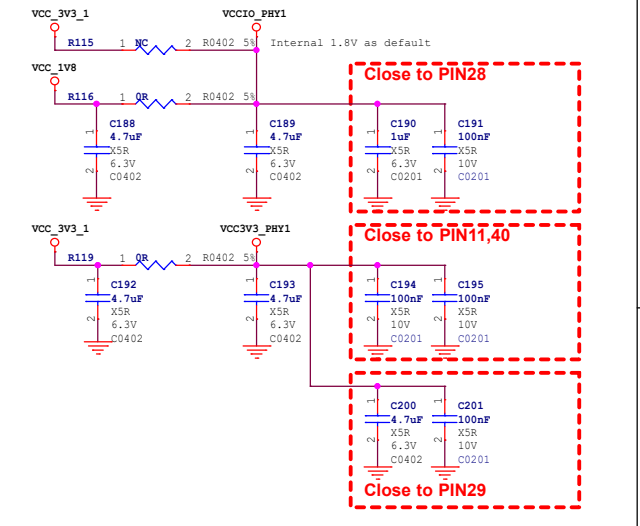
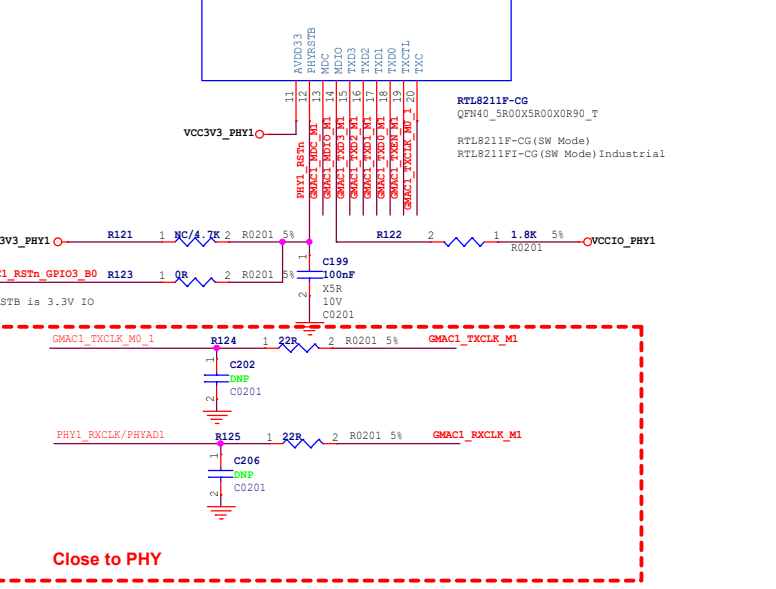
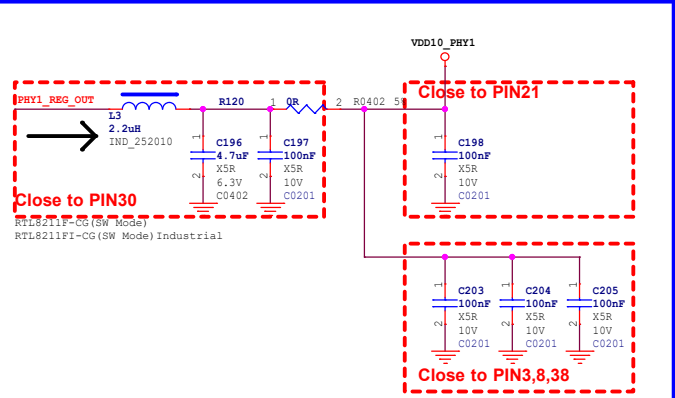
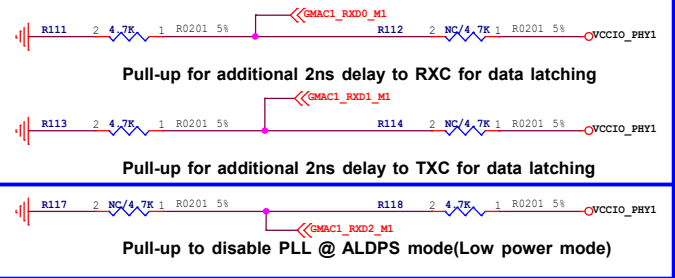
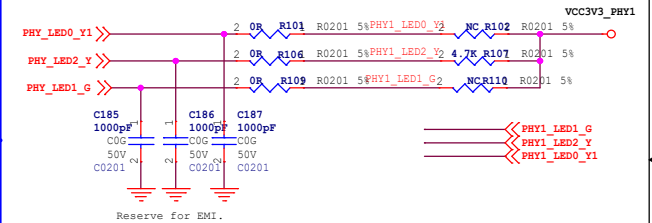
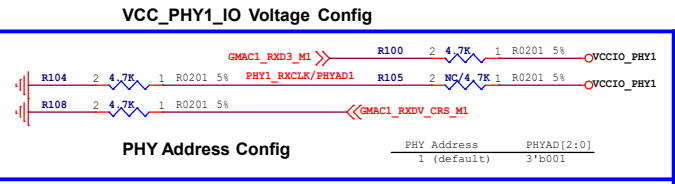
Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.




Size	Title: Rock 3 Compute Module Plus	REV
A4	Page Name: Memory-eMMC	V1.1
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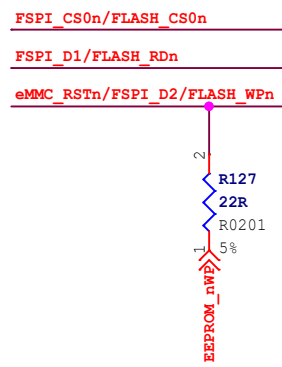
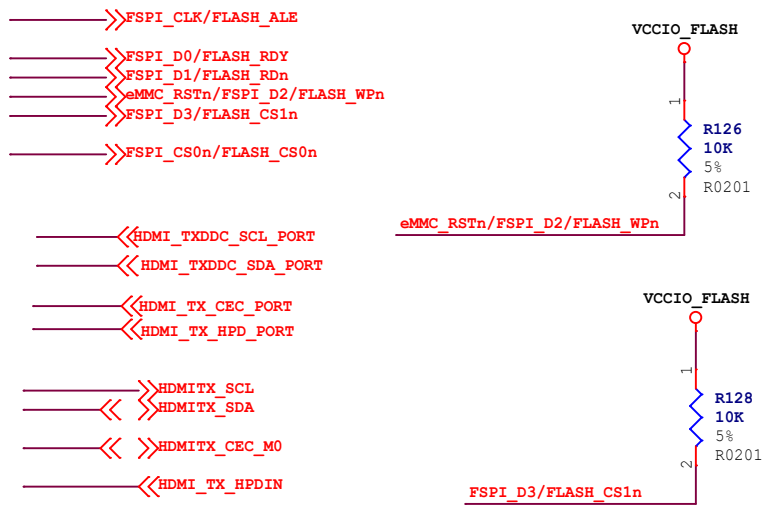


RGMI I Power Source	CFG EXT	CFG LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V(default)	1'b0	2'b10

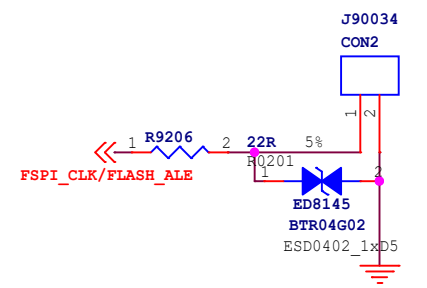
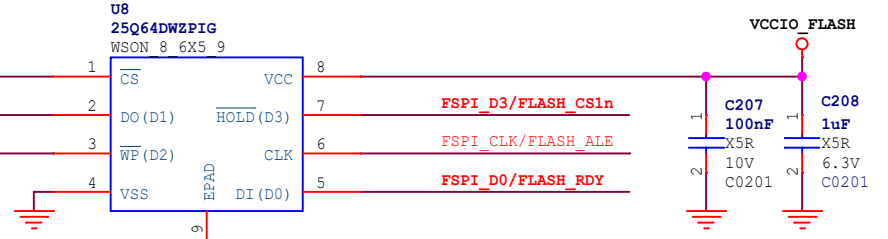




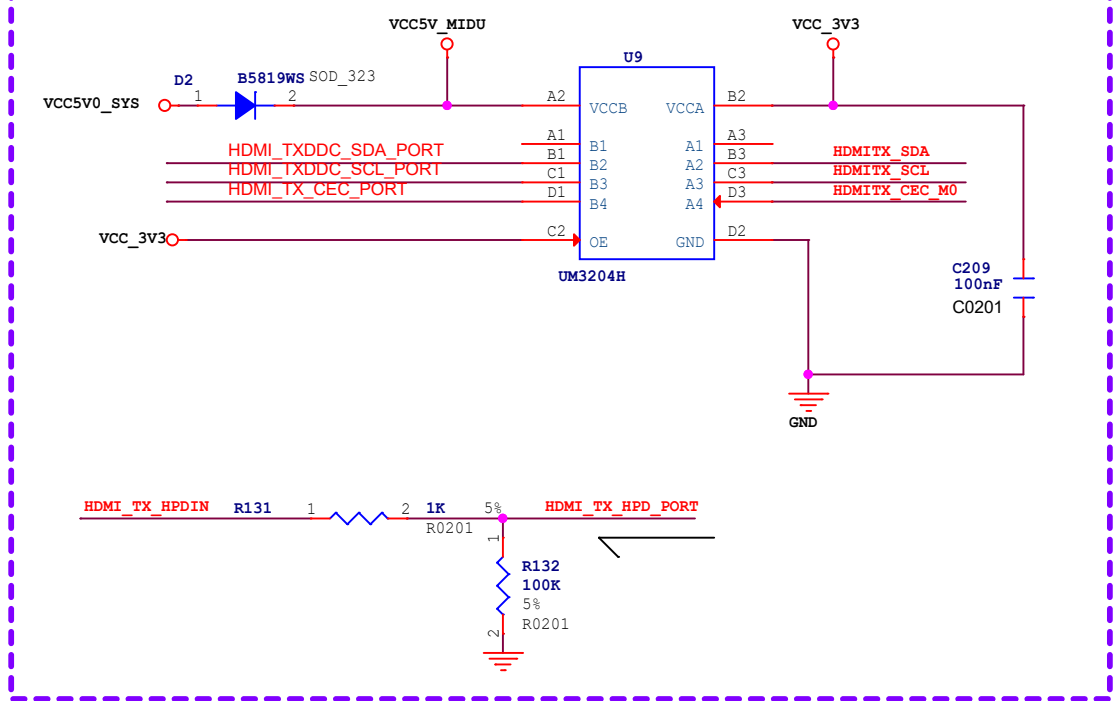
Size	Title: Rock 3 Compute Module Plus	REV
A3	Page Name: Ethernet	V1.1
Date: Tuesday, November 16, 2021	Sheet 18 of 25	



default VCC = VCCIO_FLASH 1.8V



HDMI



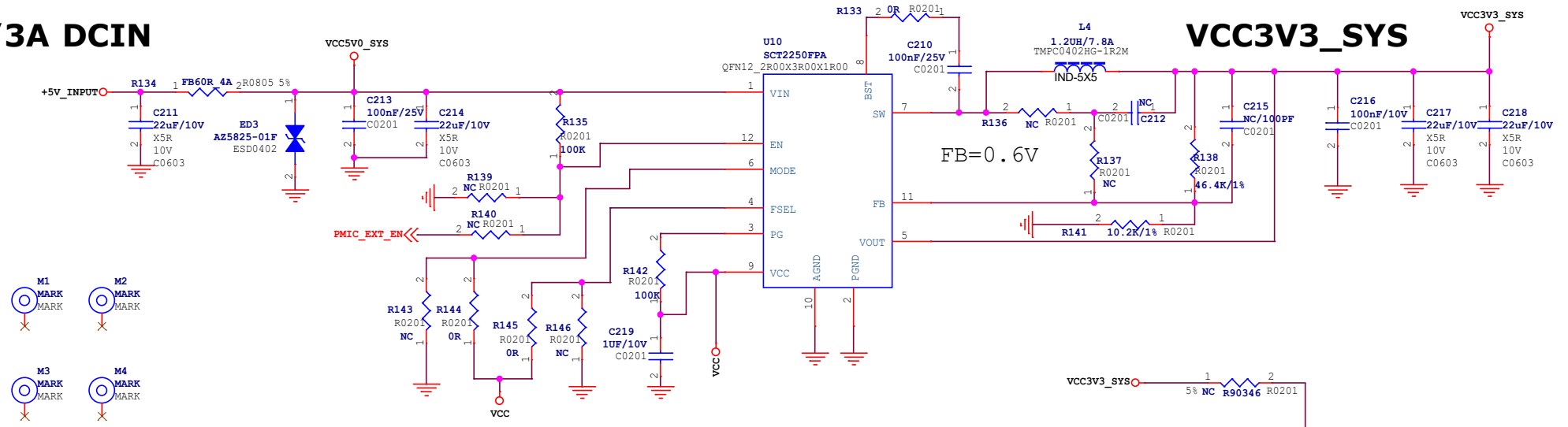
Note:

If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted, @SPI Flash is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted, @SPI Flash is not mounted when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted, @Nand is not mounted

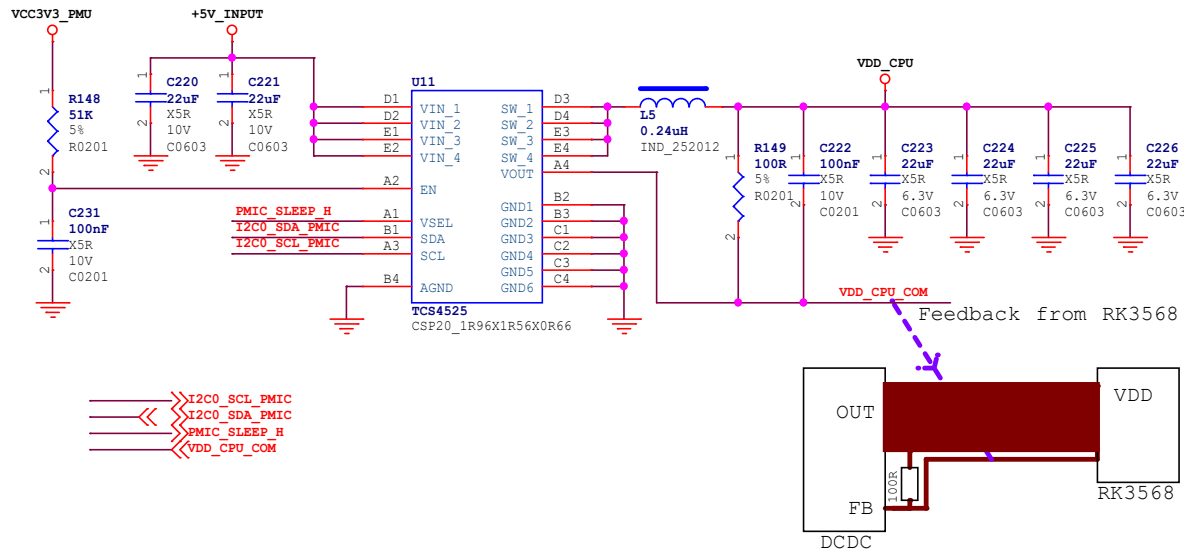


Size	Title: Rock 3 Compute Module Plus	REV
A4	Page Name: Flash-SPI-HDMI	V1.1
Date: Tuesday, November 16, 2021 Sheet 19 of 25		

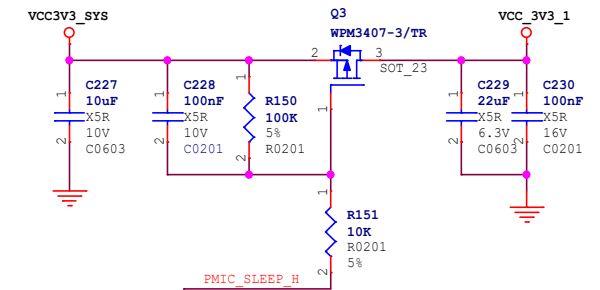
5V/3A DCIN



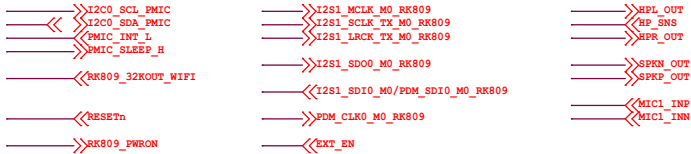
VDD_CPU



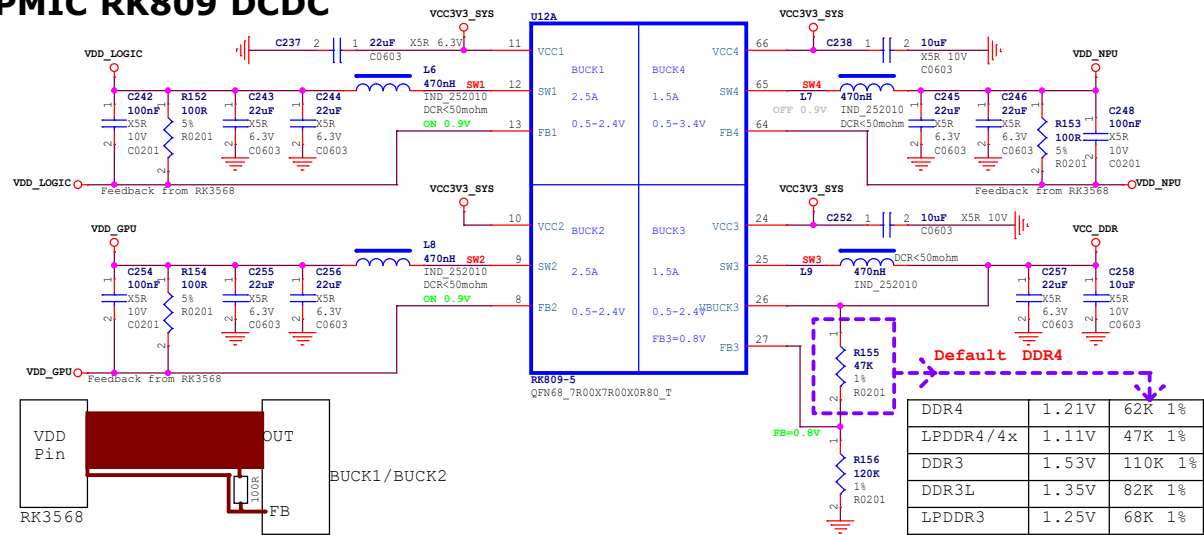
VCC_3V3 (Power OFF under SLEEP)



Size	Title: Rock 3 Compute Module Plus	REV
Custom Page Name:	Power_DC_IN	V1.1
Date: Tuesday, November 16, 2021	Sheet 20 of 25	

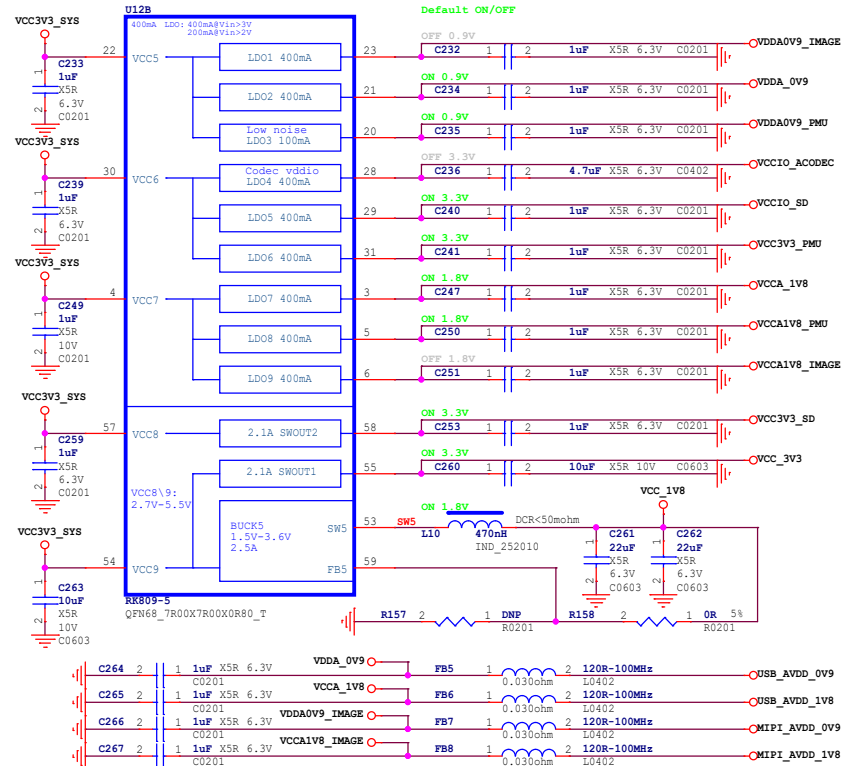


PMIC RK809 DCDC

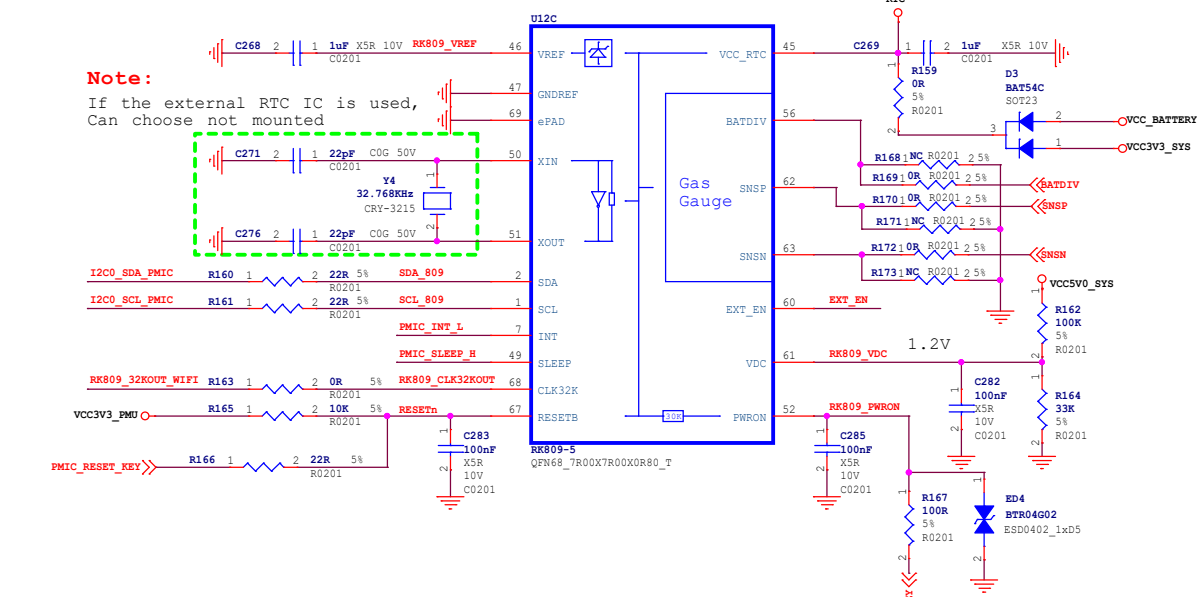


DDR4	1.21V	62K	1%
LPDDR4/4x	1.11V	47K	1%
DDR3	1.53V	110K	1%
DDR3L	1.35V	82K	1%
LPDDR3	1.25V	68K	1%

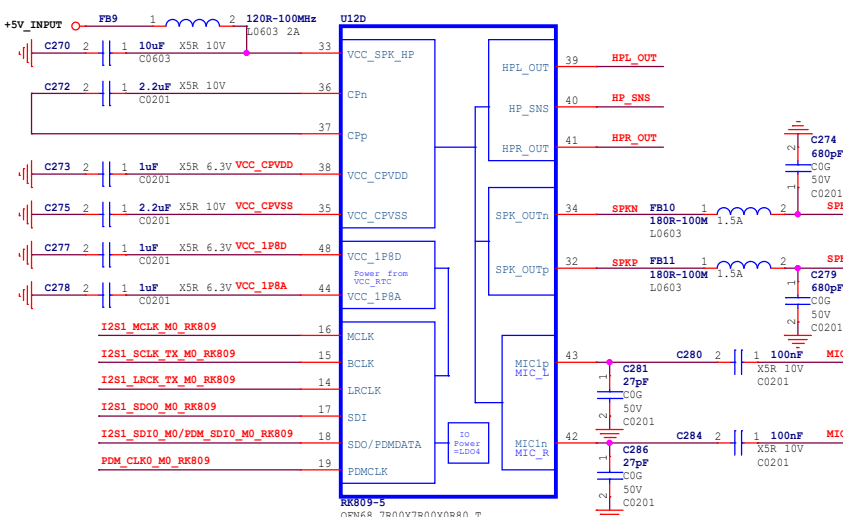
PMIC RK809 LDO

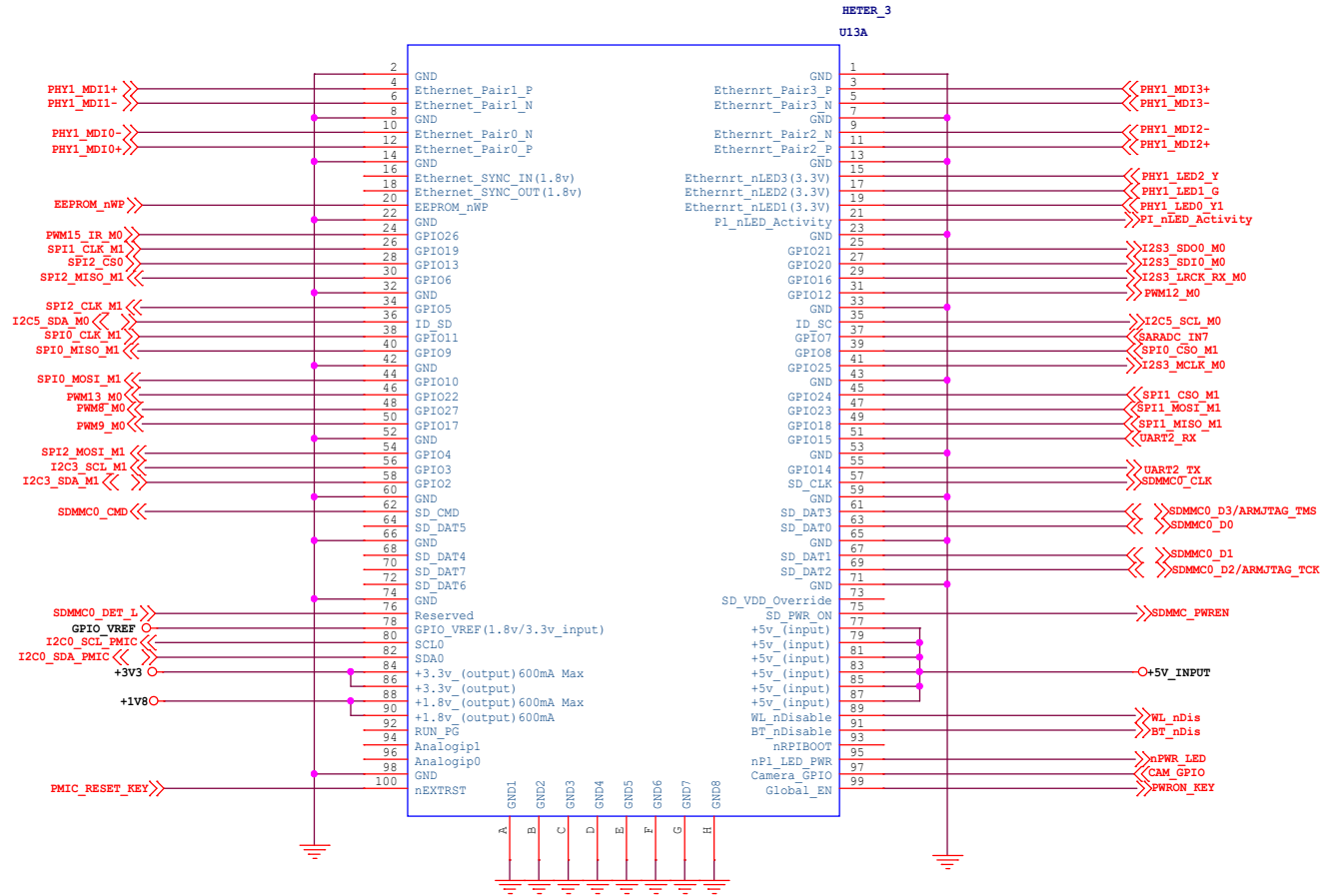


PMIC RK809 Management

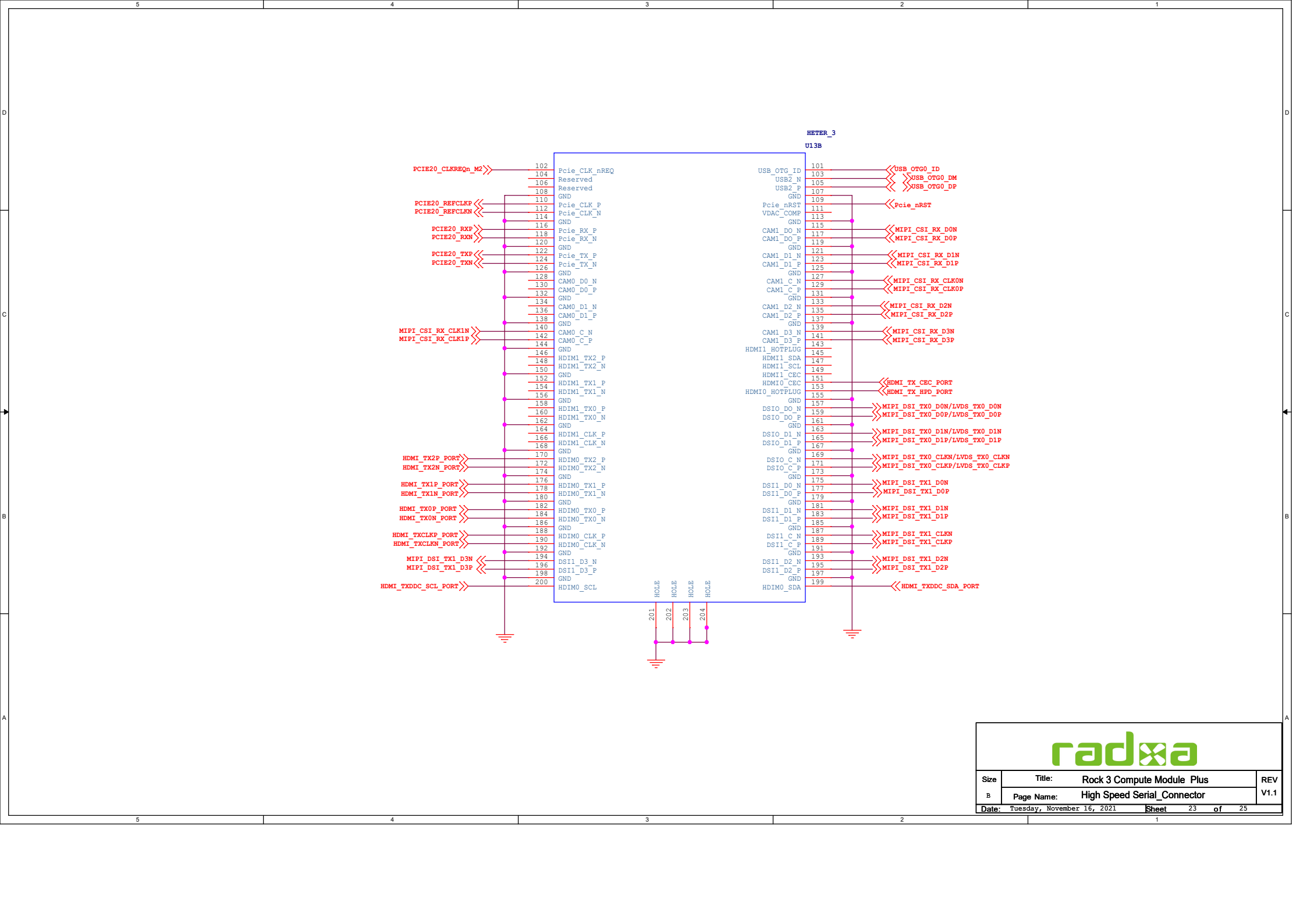


PMIC RK809 CODEC



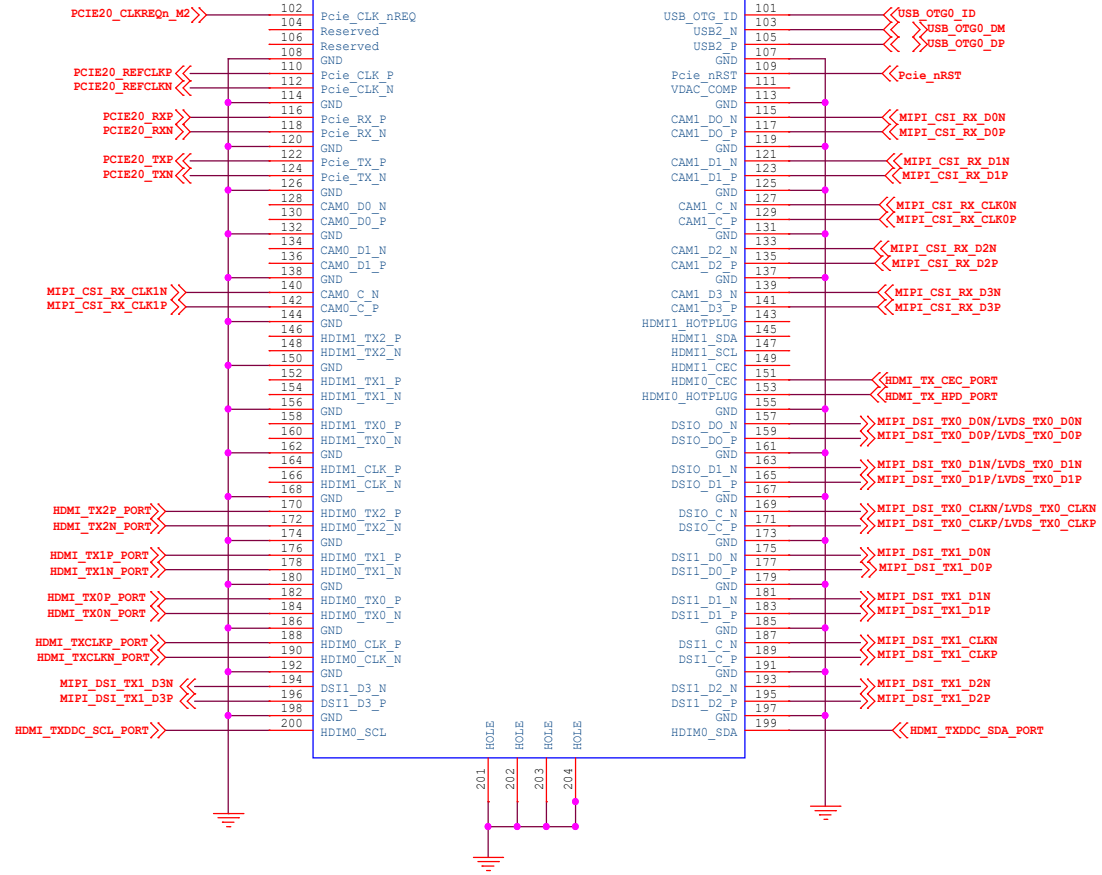


Size	Title: Rock 3 Compute Module Plus	REV
B	Page Name: GPIO+VCC_Connector	V1.1
Date:	Tuesday, November 16, 2021	Sheet 22 of 25



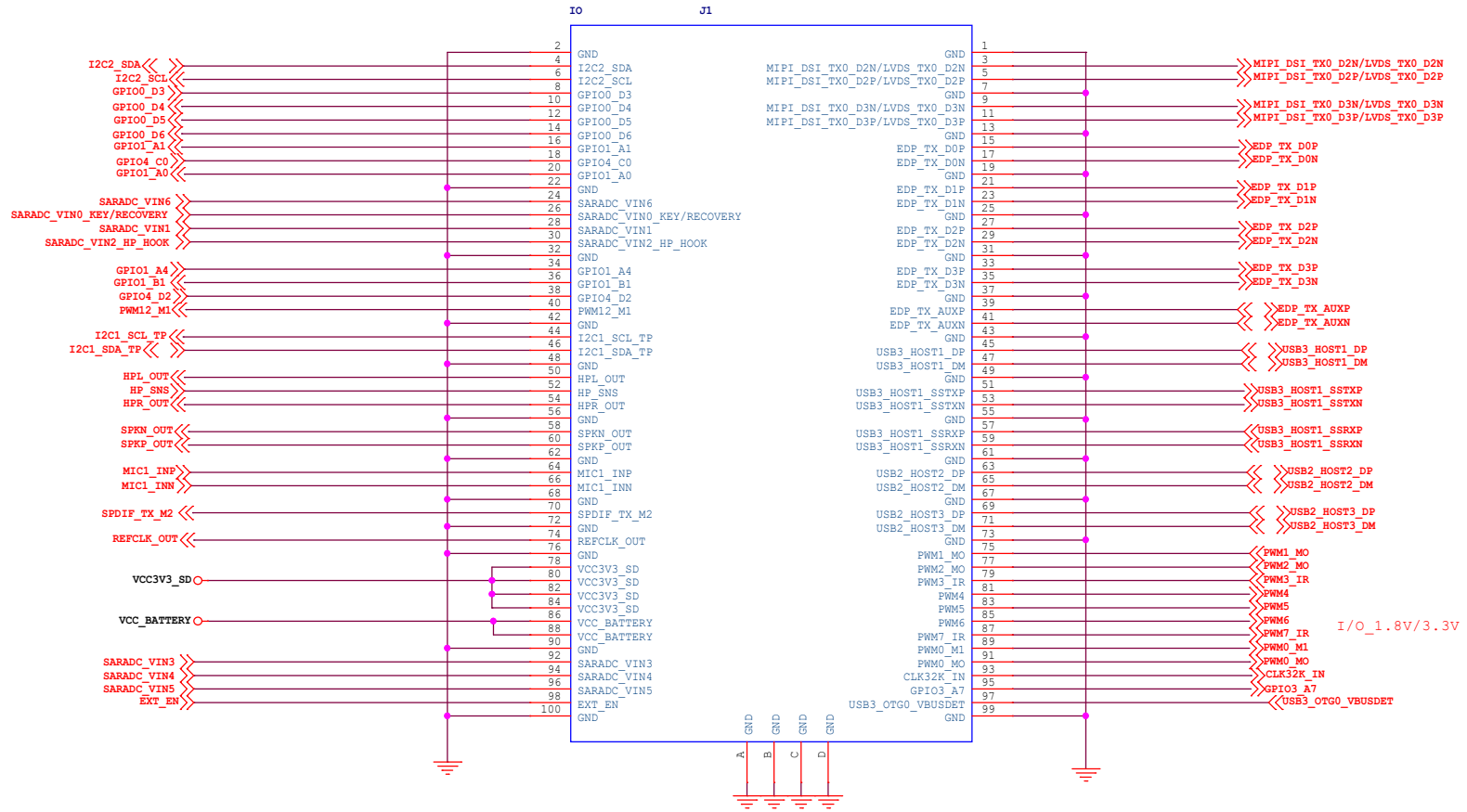
HETER_3

U13B



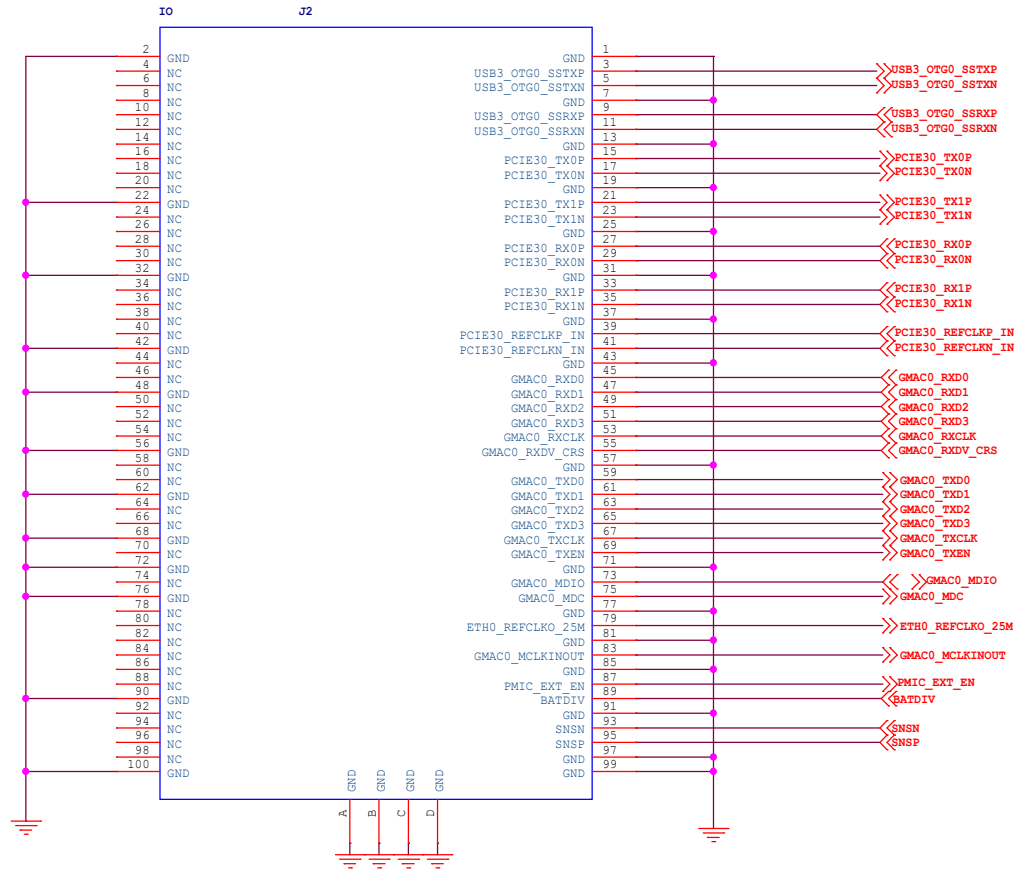
radxa

Size	Title: Rock 3 Compute Module Plus	REV
B	Page Name: High Speed Serial Connector	V1.1
Date: Tuesday, November 16, 2021		
Sheet		23 of 25



radxa

Size	Title: Rock 3 Compute Module Plus	REV
B	Page Name: IO_Connector	V1.1
Date: Tuesday, November 16, 2021		
Sheet 24 of 25		



Size	Title: Rock 3 Compute Module Plus	REV
B	Page Name: IO2_Connector	V1.1
Date: Tuesday, November 16, 2021	Sheet 25	of 25