



Radxa CM3J

Schematic

V1.2

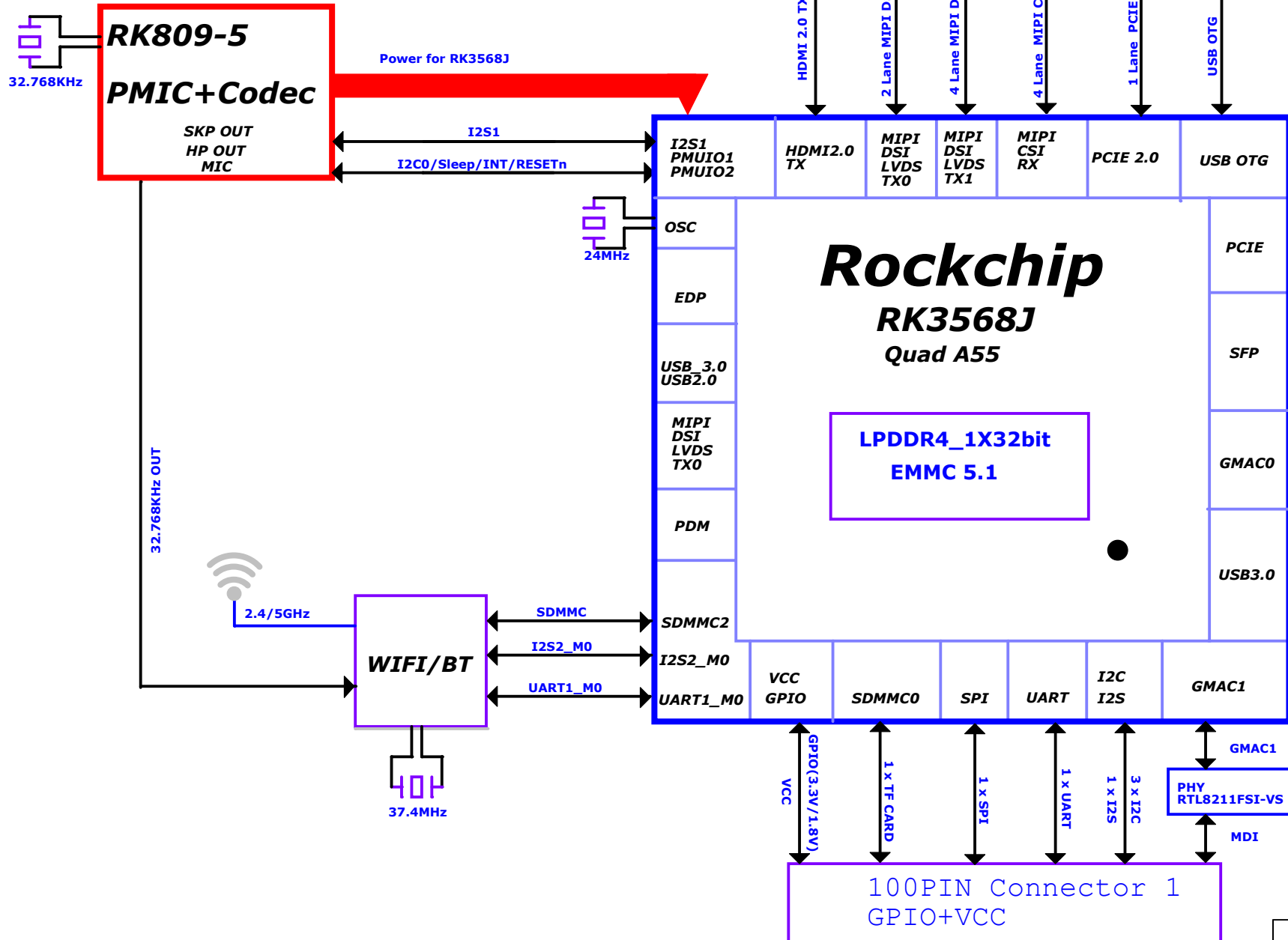
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- 15.RTL8211FS VS CG
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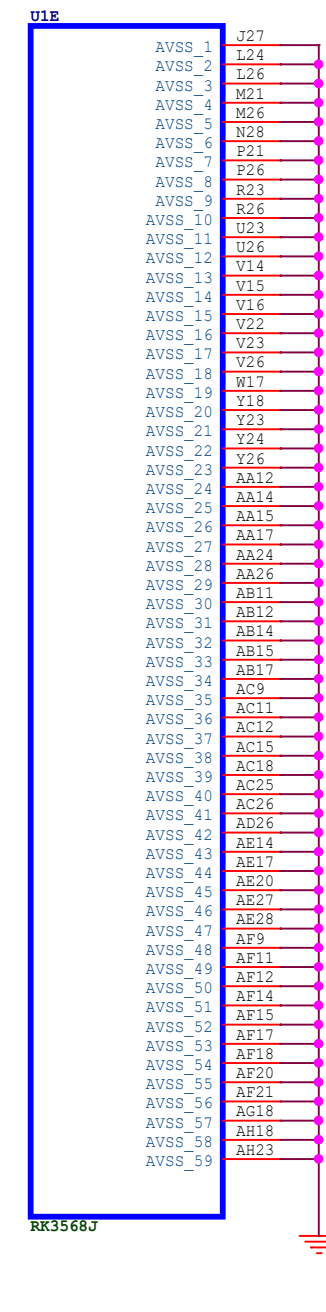
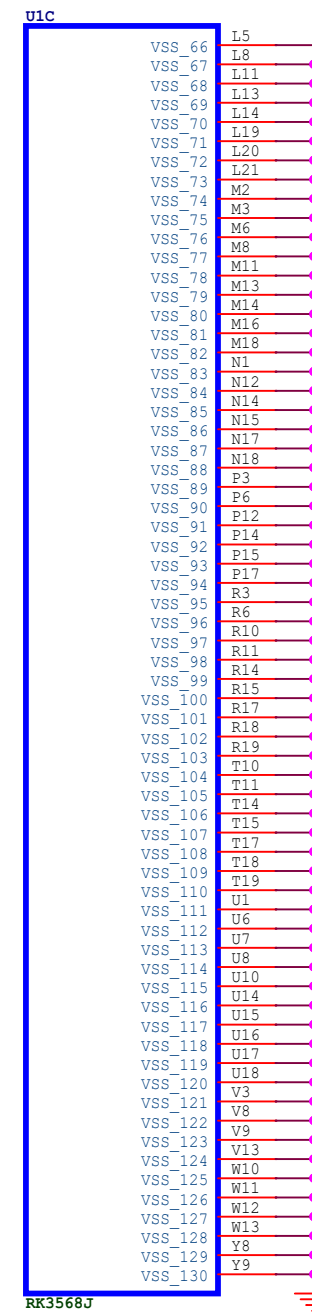
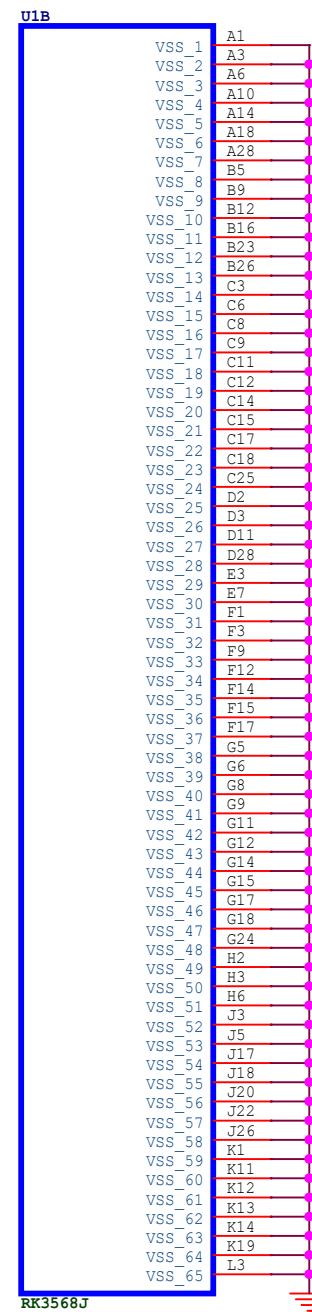
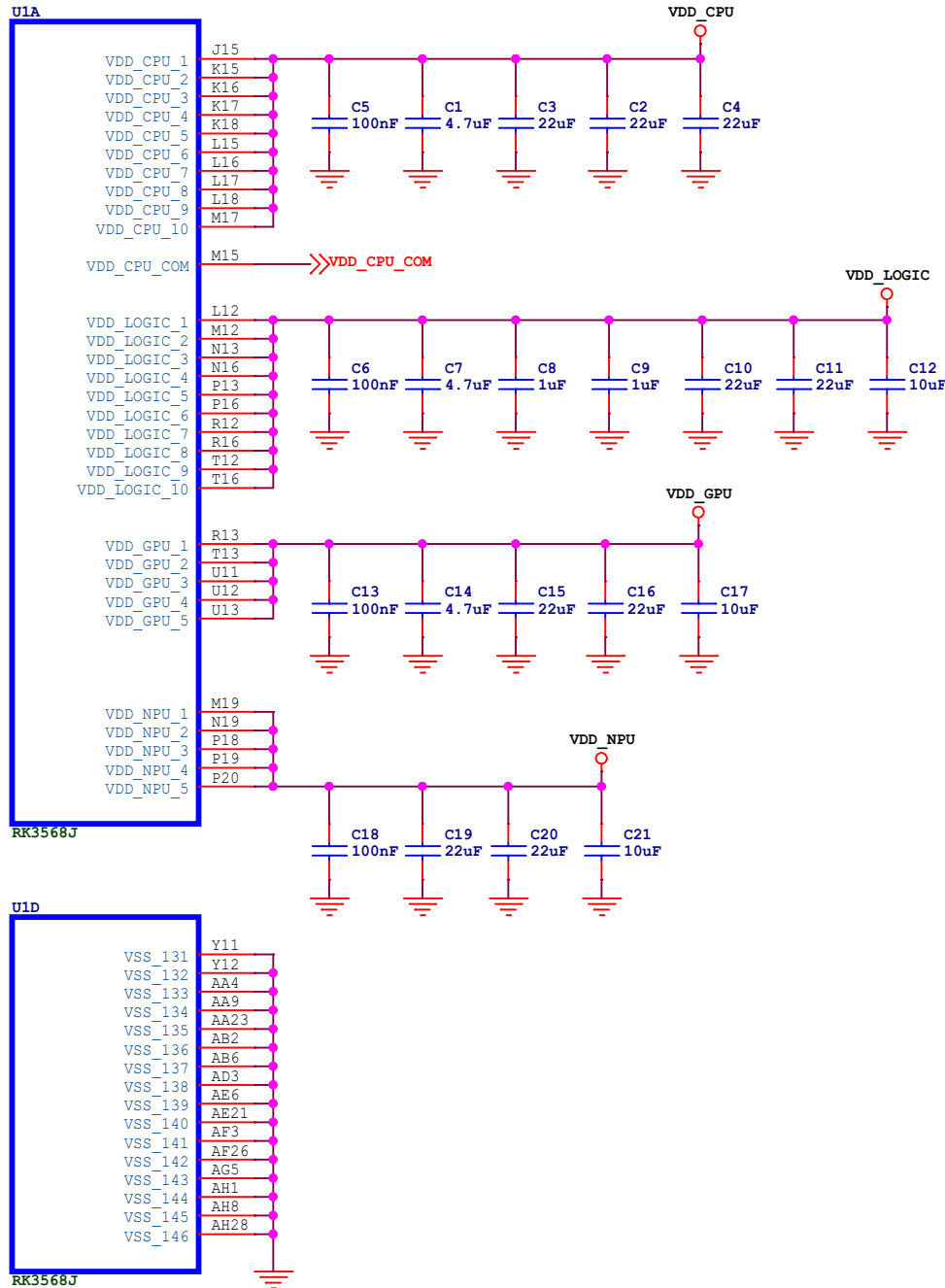


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CM3J Block Diagram

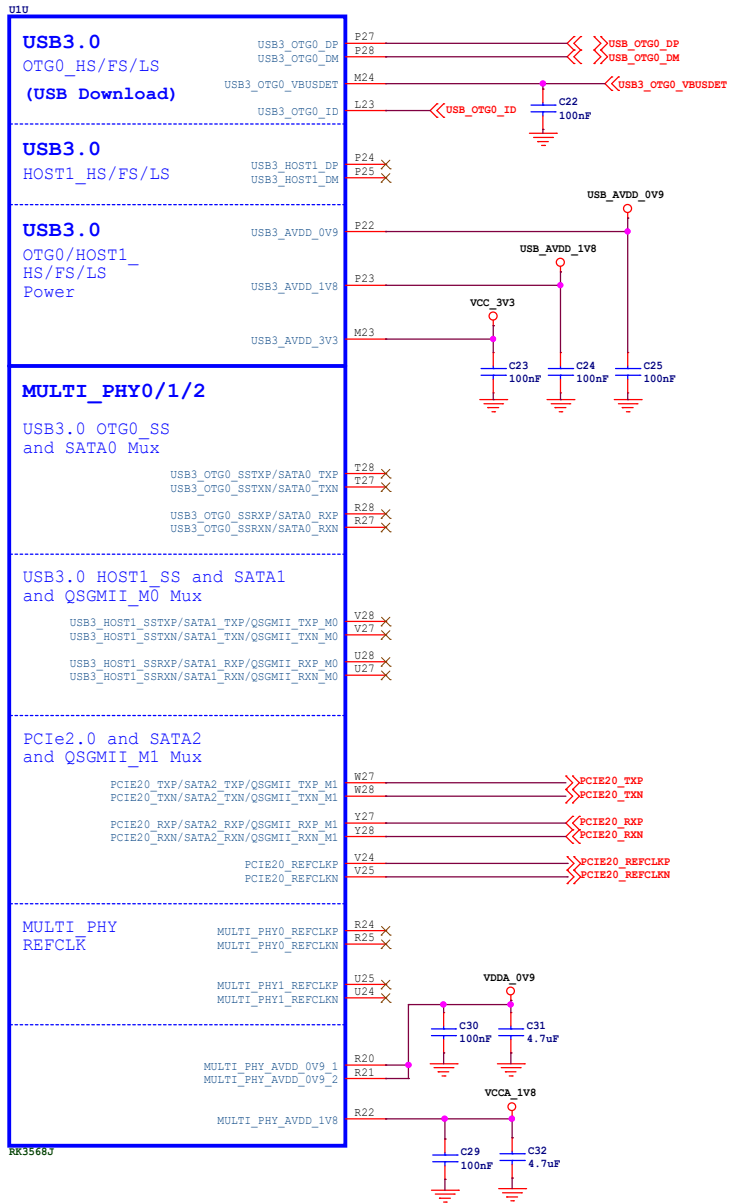


RK3568J_ABCDE (Power&Gnd)

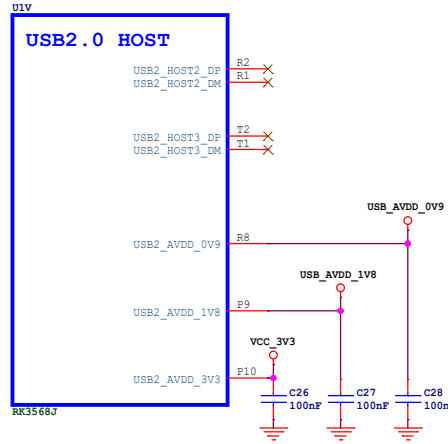


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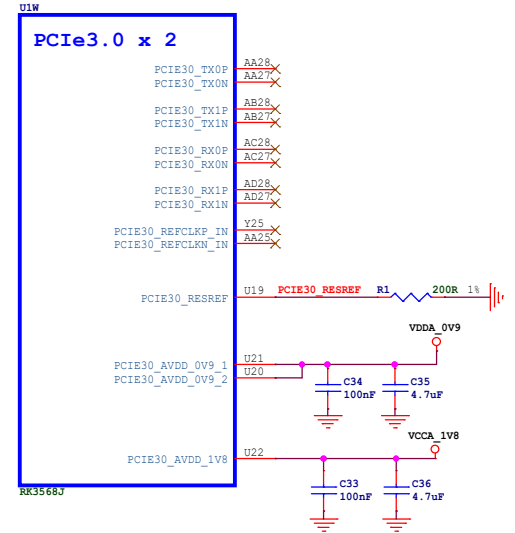
RK3568J_U (USB3.0/SATA/QSGMII/PCIe2.0 x1)



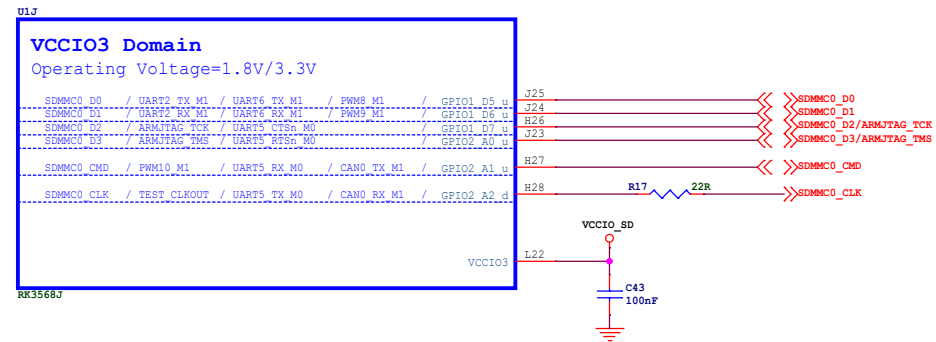
RK3568J_V (USB2.0 HOST)



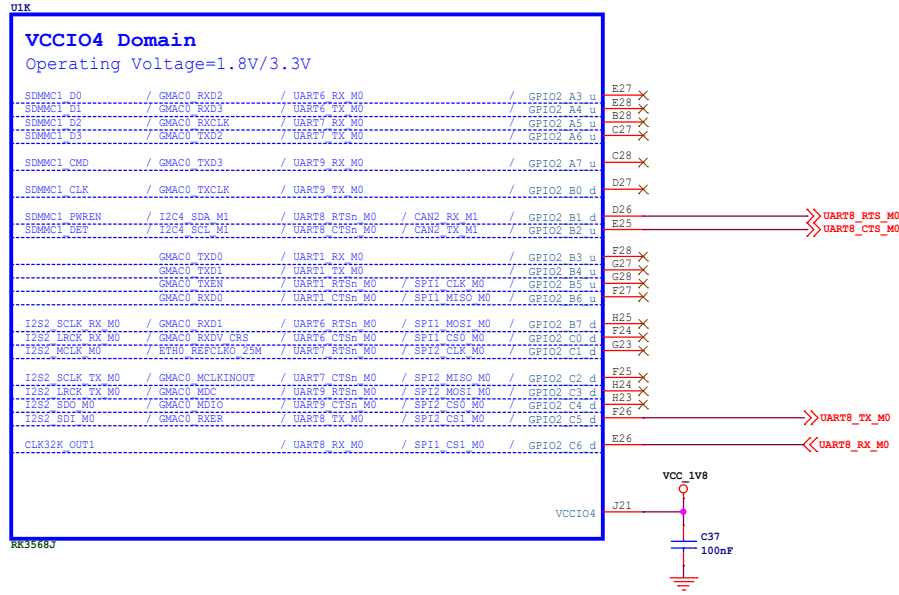
RK3568J_W (PCIe3.0 x2)



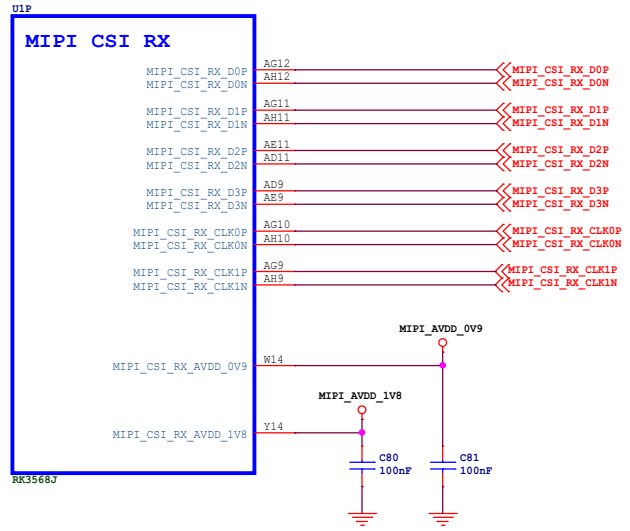
RK3568J_J (VCCIO3 Domain)



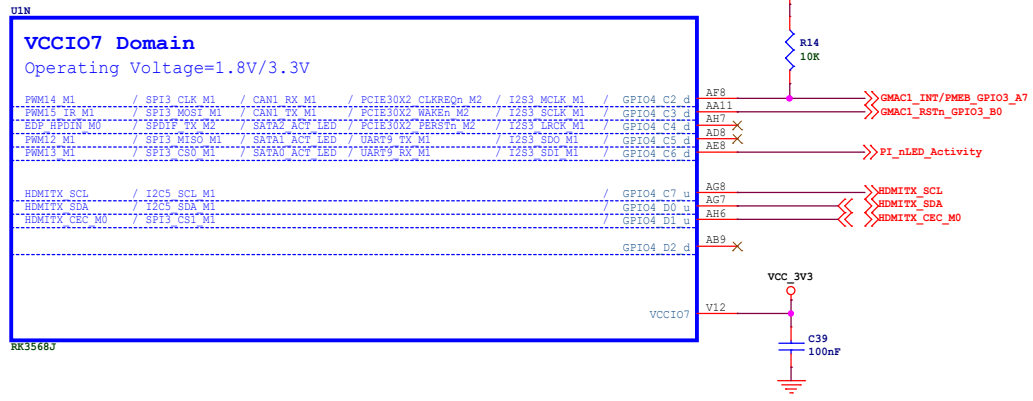
RK3568J_K (VCCIO4 Domain)



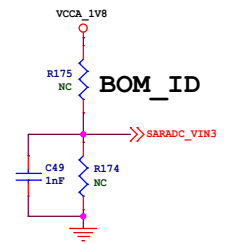
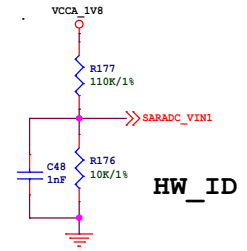
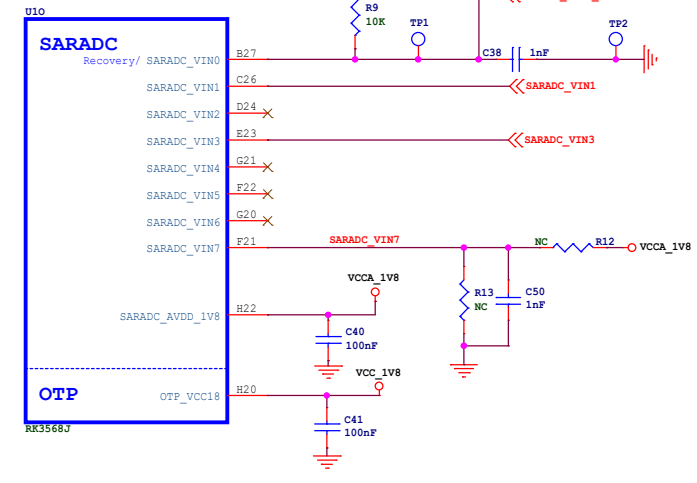
RK3568J_P (MIPI_CSI_RX)



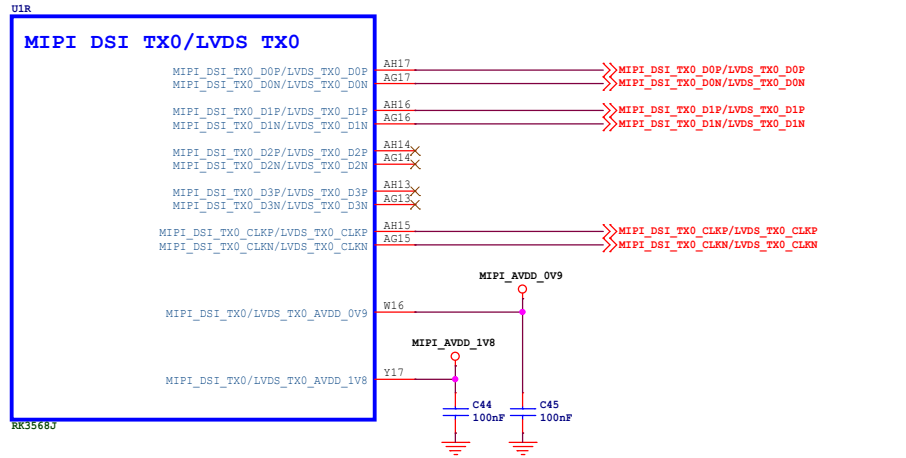
RK3568J_N (VCCIO7 Domain)



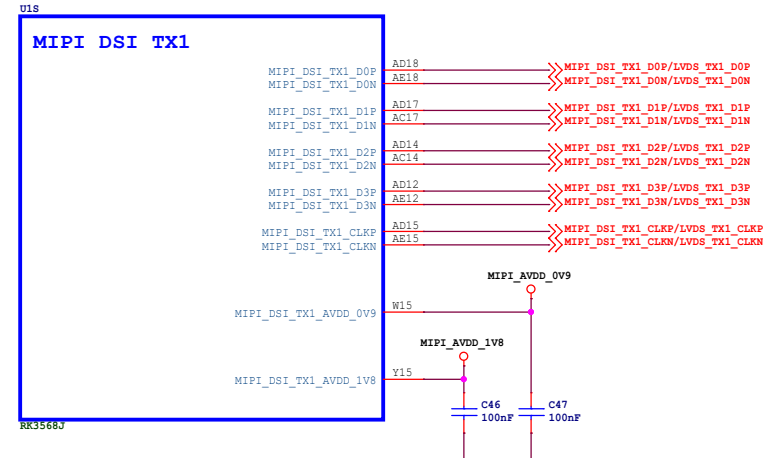
RK3568J_O (SARADC/OTP)



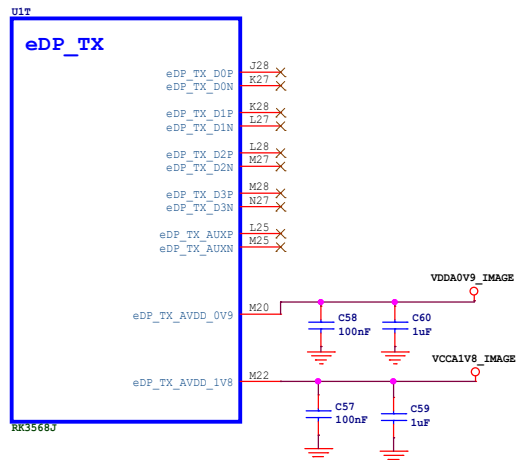
RK3568J_R (MIPI_DSI_TX0/LVDS_TX0)



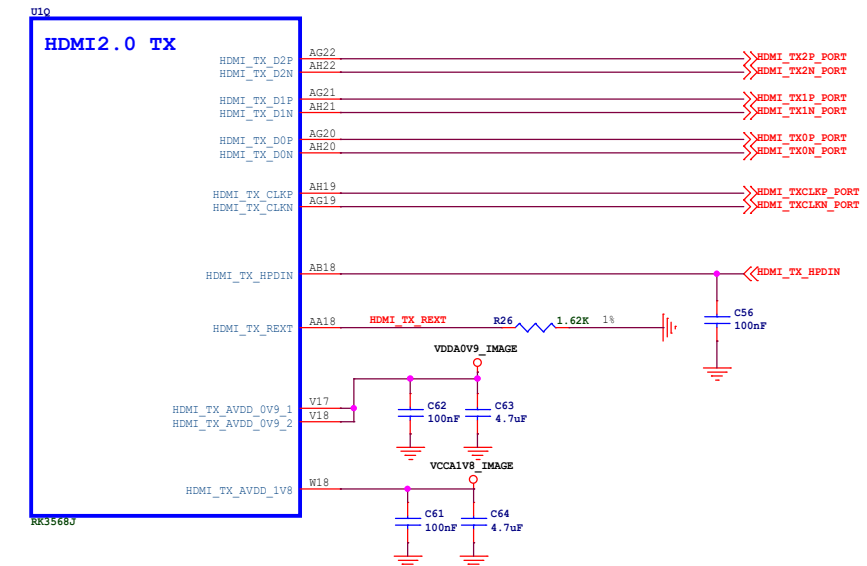
RK3568J_S (MIPI_DSI_TX1)



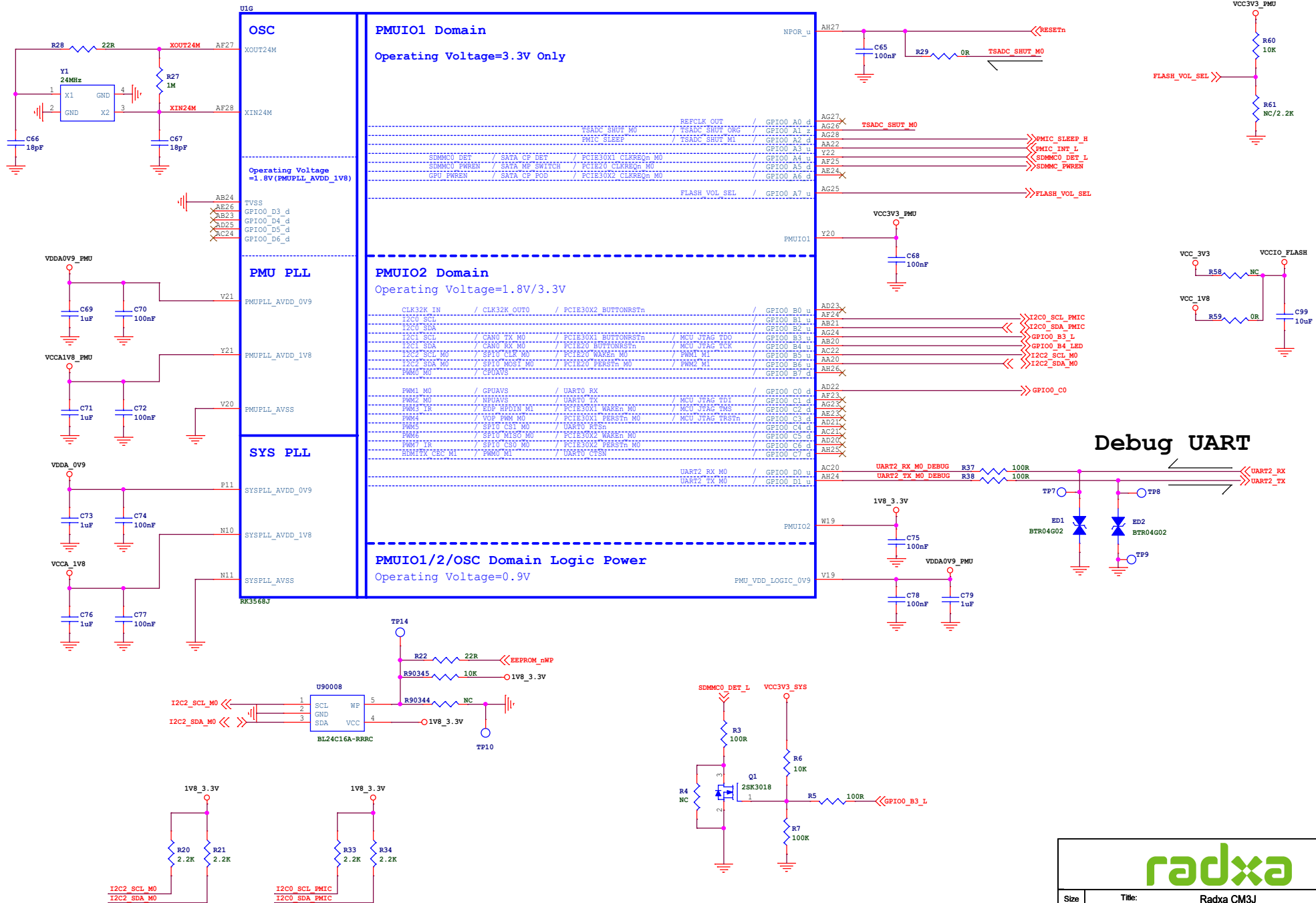
RK3568J_T (eDP TX)



RK3568J_Q (HDMI2.0 TX)

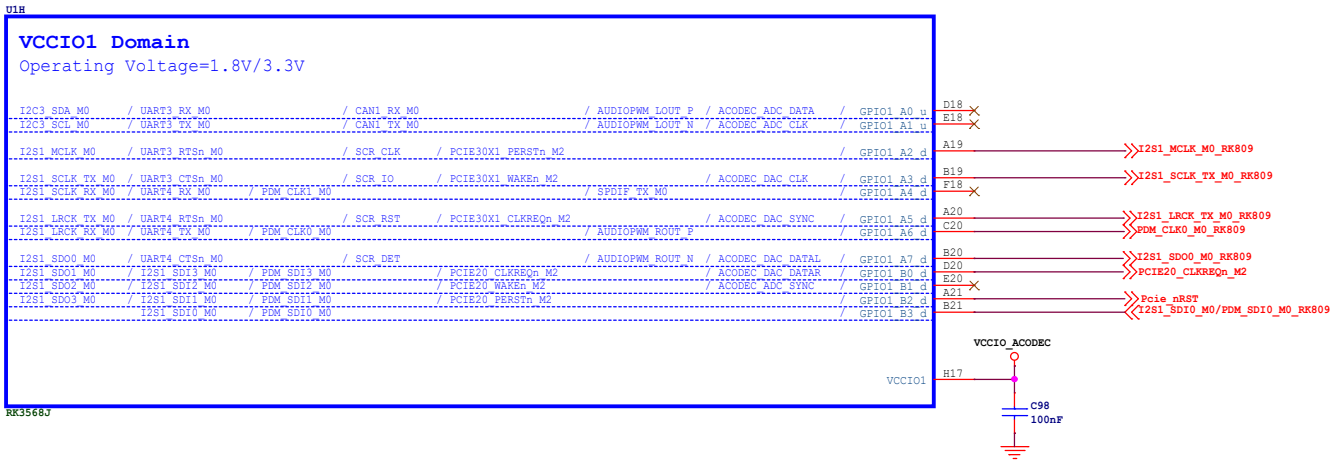


RK3568J_G (OSC/PLL/PMUIO1/2)



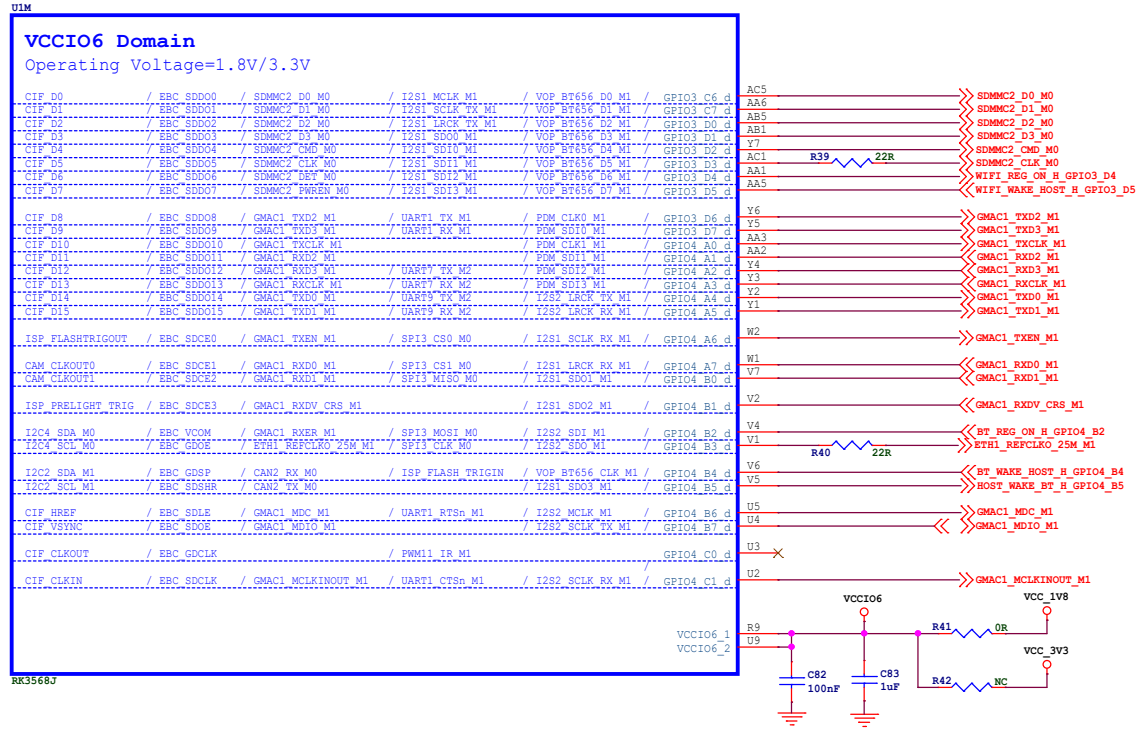
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RK3568J_H (VCCIO1 Domain)



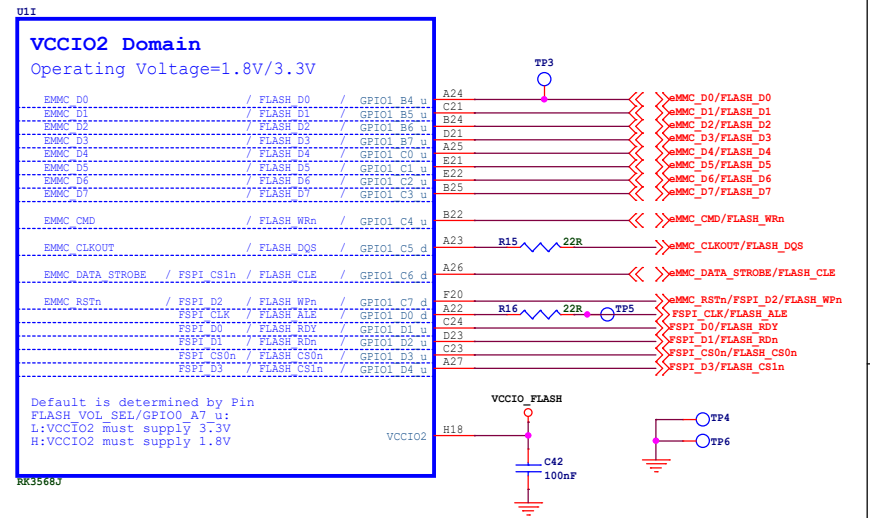
RK3568J

RK3568J_M (VCCIO6 Domain)



RK3568J

RK3568J_I (VCCIO2 Domain)



RK3568J



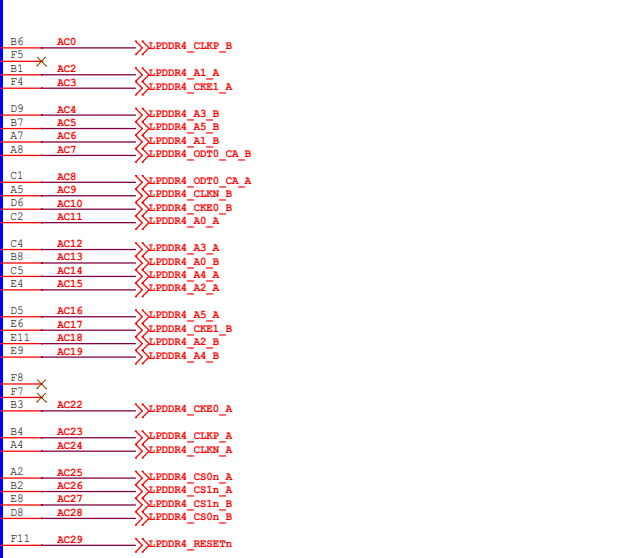
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RK3568J_F (DDR PHY)

ULP

	DDR4	LPDDR4	DDR3	LPDDR3
LPDDR4_DQ0_A <<>>	DDR DQ0 A	F2	DDR DQ0 A / DDR4 DQ0 A	LPDDR4 DQ0 A / DDR3 DQ0 / LPDDR3 DQ15
LPDDR4_DQ1_A <<>>	DDR DQ1 A	E1	DDR DQ1 A / DDR4 DQ1 A	LPDDR4 DQ1 A / DDR3 DQ1 / LPDDR3 DQ14
LPDDR4_DQ2_A <<>>	DDR DQ2 A	E2	DDR DQ2 A / DDR4 DQ2 A	LPDDR4 DQ2 A / DDR3 DQ2 / LPDDR3 DQ13
LPDDR4_DQ3_A <<>>	DDR DQ3 A	D1	DDR DQ3 A / DDR4 DQ3 A	LPDDR4 DQ3 A / DDR3 DQ3 / LPDDR3 DQ12
LPDDR4_DQ4_A <<>>	DDR DQ4 A	D1	DDR DQ4 A / DDR4 DQ4 A	LPDDR4 DQ4 A / DDR3 DQ4 / LPDDR3 DQ11
LPDDR4_DQ5_A <<>>	DDR DQ5 A	J2	DDR DQ5 A / DDR4 DQ5 A	LPDDR4 DQ5 A / DDR3 DQ5 / LPDDR3 DQ10
LPDDR4_DQ6_A <<>>	DDR DQ6 A	H1	DDR DQ6 A / DDR4 DQ6 A	LPDDR4 DQ6 A / DDR3 DQ6 / LPDDR3 DQ09
LPDDR4_DQ7_A <<>>	DDR DQ7 A	H4	DDR DQ7 A / DDR4 DQ7 A	LPDDR4 DQ7 A / DDR3 DQ7 / LPDDR3 DQ08
LPDDR4_DM0_A <<>>	DDR DM0 A	G5	DDR DM0 A / DDR4 DML A	LPDDR4 DM0 A / DDR3 DM0 / LPDDR3 DM1
LPDDR4_DQS0P_A <<>>	DDR DQS0P A	H1	DDR DQS0P A / DDR4 DQS1 P A	LPDDR4 DQS0P A / DDR3 DQS0P / LPDDR3 DQS1P
LPDDR4_DQS0N_A <<>>	DDR DQS0N A	G2	DDR DQS0N A / DDR4 DQS1 N A	LPDDR4 DQS0N A / DDR3 DQS0N / LPDDR3 DQS1N
LPDDR4_DQ8_A <<>>	DDR DQ8 A	M1	DDR DQ8 A / DDR4 DQ03 A	LPDDR4 DQ8 A / DDR3 DQ8 / LPDDR3 DQ25
LPDDR4_DQ9_A <<>>	DDR DQ9 A	N2	DDR DQ9 A / DDR4 DQ01 A	LPDDR4 DQ9 A / DDR3 DQ9 / LPDDR3 DQ24
LPDDR4_DQ10_A <<>>	DDR DQ10 A	M7	DDR DQ10 A / DDR4 DQ07 A	LPDDR4 DQ10 A / DDR3 DQ10 / LPDDR3 DQ23
LPDDR4_DQ11_A <<>>	DDR DQ11 A	L6	DDR DQ11 A / DDR4 DQ05 A	LPDDR4 DQ11 A / DDR3 DQ11 / LPDDR3 DQ22
LPDDR4_DQ12_A <<>>	DDR DQ12 A	K2	DDR DQ12 A / DDR4 DQ03 A	LPDDR4 DQ12 A / DDR3 DQ12 / LPDDR3 DQ21
LPDDR4_DQ13_A <<>>	DDR DQ13 A	J6	DDR DQ13 A / DDR4 DQ01 A	LPDDR4 DQ13 A / DDR3 DQ13 / LPDDR3 DQ20
LPDDR4_DQ14_A <<>>	DDR DQ14 A	L7	DDR DQ14 A / DDR4 DQ06 A	LPDDR4 DQ14 A / DDR3 DQ14 / LPDDR3 DQ19
LPDDR4_DQ15_A <<>>	DDR DQ15 A	A4	DDR DQ15 A / DDR4 DQ04 A	LPDDR4 DQ15 A / DDR3 DQ15 / LPDDR3 DQ18
LPDDR4_DM1_A <<>>	DDR DM1 A	J4	DDR DM1 A / DDR4 DM0 A	LPDDR4 DM1 A / DDR3 DM1 / LPDDR3 DM3
LPDDR4_DQS1P_A <<>>	DDR DQS1P A	L2	DDR DQS1P A / DDR4 DQS1 P A	LPDDR4 DQS1P A / DDR3 DQS1P / LPDDR3 DQS1P
LPDDR4_DQS1N_A <<>>	DDR DQS1N A	L1	DDR DQS1N A / DDR4 DQS1 N A	LPDDR4 DQS1N A / DDR3 DQS1N / LPDDR3 DQS1N
LPDDR4_DQ0_B <<>>	DDR DQ0 B	B10	DDR DQ0 B / DDR4 DQ07 B	LPDDR4 DQ0 B / DDR3 DQ16 / LPDDR3 DQ1
LPDDR4_DQ1_B <<>>	DDR DQ1 B	A9	DDR DQ1 B / DDR4 DQ05 B	LPDDR4 DQ1 B / DDR3 DQ17 / LPDDR3 DQ05
LPDDR4_DQ2_B <<>>	DDR DQ2 B	D12	DDR DQ2 B / DDR4 DQ03 B	LPDDR4 DQ2 B / DDR3 DQ18 / LPDDR3 DQ06
LPDDR4_DQ3_B <<>>	DDR DQ3 B	E12	DDR DQ3 B / DDR4 DQ01 B	LPDDR4 DQ3 B / DDR3 DQ19 / LPDDR3 DQ07
LPDDR4_DQ4_B <<>>	DDR DQ4 B	A12	DDR DQ4 B / DDR4 DQ06 B	LPDDR4 DQ4 B / DDR3 DQ20 / LPDDR3 DQ08
LPDDR4_DQ5_B <<>>	DDR DQ5 B	D15	DDR DQ5 B / DDR4 DQ04 B	LPDDR4 DQ5 B / DDR3 DQ21 / LPDDR3 DQ09
LPDDR4_DQ6_B <<>>	DDR DQ6 B	B15	DDR DQ6 B / DDR4 DQ02 B	LPDDR4 DQ6 B / DDR3 DQ22 / LPDDR3 DQ10
LPDDR4_DQ7_B <<>>	DDR DQ7 B	B15	DDR DQ7 B / DDR4 DQ02 B	LPDDR4 DQ7 B / DDR3 DQ23 / LPDDR3 DQ11
LPDDR4_DM0_B <<>>	DDR DM0 B	D14	DDR DM0 B / DDR4 DM0 B	LPDDR4 DM0 B / DDR3 DM2 / LPDDR3 DM0
LPDDR4_DQS0P_B <<>>	DDR DQS0P B	A11	DDR DQS0P B / DDR4 DQS0 P B	LPDDR4 DQS0P B / DDR3 DQS2P / LPDDR3 DQS0P
LPDDR4_DQS0N_B <<>>	DDR DQS0N B	B11	DDR DQS0N B / DDR4 DQS0 N B	LPDDR4 DQS0N B / DDR3 DQS2N / LPDDR3 DQS0N
LPDDR4_DQ8_B <<>>	DDR DQ8 B	A16	DDR DQ8 B / DDR4 DQ10 B	LPDDR4 DQ8 B / DDR3 DQ24 / LPDDR3 DQ18
LPDDR4_DQ9_B <<>>	DDR DQ9 B	B17	DDR DQ9 B / DDR4 DQ08 B	LPDDR4 DQ9 B / DDR3 DQ25 / LPDDR3 DQ19
LPDDR4_DQ10_B <<>>	DDR DQ10 B	A17	DDR DQ10 B / DDR4 DQ06 B	LPDDR4 DQ10 B / DDR3 DQ26 / LPDDR3 DQ20
LPDDR4_DQ11_B <<>>	DDR DQ11 B	B18	DDR DQ11 B / DDR4 DQ04 B	LPDDR4 DQ11 B / DDR3 DQ27 / LPDDR3 DQ21
LPDDR4_DQ12_B <<>>	DDR DQ12 B	B13	DDR DQ12 B / DDR4 DQ03 B	LPDDR4 DQ12 B / DDR3 DQ28 / LPDDR3 DQ22
LPDDR4_DQ13_B <<>>	DDR DQ13 B	A13	DDR DQ13 B / DDR4 DQ01 B	LPDDR4 DQ13 B / DDR3 DQ29 / LPDDR3 DQ23
LPDDR4_DQ14_B <<>>	DDR DQ14 B	D17	DDR DQ14 B / DDR4 DQ06 B	LPDDR4 DQ14 B / DDR3 DQ30 / LPDDR3 DQ24
LPDDR4_DQ15_B <<>>	DDR DQ15 B	B14	DDR DQ15 B / DDR4 DQ04 B	LPDDR4 DQ15 B / DDR3 DQ31 / LPDDR3 DQ25
LPDDR4_DM1_B <<>>	DDR DM1 B	E17	DDR DM1 B / DDR4 DML B	LPDDR4 DM1 B / DDR3 DM3 / LPDDR3 DM2
LPDDR4_DQS1P_B <<>>	DDR DQS1P B	B15	DDR DQS1P B / DDR4 DQS1 P B	LPDDR4 DQS1P B / DDR3 DQS3P / LPDDR3 DQS2P
LPDDR4_DQS1N_B <<>>	DDR DQS1N B	A15	DDR DQS1N B / DDR4 DQS1 N B	LPDDR4 DQS1N B / DDR3 DQS3N / LPDDR3 DQS2N
LPDDR4_ECC_DQ0 <<>>	DDR ECC DQ0	P5	DDR ECC DQ0 / DDR4 ECC DQ7	DDR3 ECC DQ0
LPDDR4_ECC_DQ1 <<>>	DDR ECC DQ1	M5	DDR ECC DQ1 / DDR4 ECC DQ8	DDR3 ECC DQ1
LPDDR4_ECC_DQ2 <<>>	DDR ECC DQ2	B5	DDR ECC DQ2 / DDR4 ECC DQ9	DDR3 ECC DQ2
LPDDR4_ECC_DQ3 <<>>	DDR ECC DQ3	M7	DDR ECC DQ3 / DDR4 ECC DQ6	DDR3 ECC DQ3
LPDDR4_ECC_DQ4 <<>>	DDR ECC DQ4	B7	DDR ECC DQ4 / DDR4 ECC DQ8	DDR3 ECC DQ4
LPDDR4_ECC_DQ5 <<>>	DDR ECC DQ5	P4	DDR ECC DQ5 / DDR4 ECC DQ9	DDR3 ECC DQ5
LPDDR4_ECC_DQ6 <<>>	DDR ECC DQ6	R4	DDR ECC DQ6 / DDR4 ECC DQ5	DDR3 ECC DQ6
LPDDR4_ECC_DM <<>>	DDR ECC DM	P7	DDR ECC DM / DDR4 ECC DM	DDR3 ECC DM
LPDDR4_ECC_DQ8_P <<>>	DDR ECC DQ8 P	P1	DDR ECC DQ8 P / DDR4 ECC DQ8 P	DDR3 ECC DQ8 P
LPDDR4_ECC_DQ8_N <<>>	DDR ECC DQ8 N	P2	DDR ECC DQ8 N / DDR4 ECC DQ8 N	DDR3 ECC DQ8 N

DDR4	LPDDR4	DDR3	LPDDR3
DDR4 A0	LPDDR4 CLKP B	DDR3 A9	---
DDR4 A1	---	DDR3 A8	---
DDR4 A2	---	DDR3 A7	---
DDR4 A3	LPDDR4 CKEL A	DDR3 A5	---
DDR4 A4	LPDDR4 A3 B	DDR3 BA1	LPDDR3 A3
DDR4 A5	LPDDR4 A1 B	DDR3 A11	LPDDR3 A1
DDR4 A6	LPDDR4 A2 B	DDR3 A10	LPDDR3 A2
DDR4 A7	LPDDR4 ODTO CA B	DDR3 A8	---
DDR4 A8	LPDDR4 ODTO CA A	DDR3 A6	LPDDR3 A9
DDR4 A9	LPDDR4 CLKN B	DDR3 A5	---
DDR4 A10	LPDDR4 CKEL B	DDR3 A10	---
DDR4 A11	LPDDR4 A0 A	DDR3 A9	LPDDR3 A8
DDR4 A12	LPDDR4 A3 A	DDR3 BA2	---
DDR4 A13	LPDDR4 A0 B	DDR3 A14	LPDDR3 A0
DDR4 A14 WE#	LPDDR4 A4 A	DDR3 A15	LPDDR3 A5
DDR4 A15 CAS#	LPDDR4 A2 A	DDR3 A0	---
DDR4 A16 RAS#	LPDDR4 A5 A	DDR3 RAS#	LPDDR3 A7
DDR4 A17	LPDDR4 CKEL B	DDR3 CKAS#	---
DDR4 A18	LPDDR4 A2 B	DDR3 A1	---
DDR4 BA1	LPDDR4 A4 B	DDR3 A12	LPDDR3 A4
DDR4 B0	LPDDR4 ODTO CA B	DDR3 WE#	---
DDR4 B1	LPDDR4 ODTO CA A	DDR3 BA0	---
DDR4 CKE	LPDDR4 CKEL A	DDR3 CKE	---
DDR4 CLKP	LPDDR4 CLKP A	DDR3 CLKP	LPDDR3 CLKP
DDR4 CLKN	LPDDR4 CLKN A	DDR3 CLKN	LPDDR3 CLKN
DDR4 CS0n	LPDDR4 CS0n A	DDR3 ODT1	LPDDR3 ODTO
DDR4 CS1n	LPDDR4 CS1n A	DDR3 ODT2	LPDDR3 ODT1
DDR4 CS2n	LPDDR4 CS2n A	DDR3 ODT3	LPDDR3 CS1n
DDR4 CS3n	LPDDR4 CS3n A	DDR3 ODT4	LPDDR3 CS2n
DDR4 CS4n	LPDDR4 CS4n A	DDR3 CS0n	LPDDR3 CS0n
DDR4 RESETn	LPDDR4 RESETn	DDR3 RESETn	---

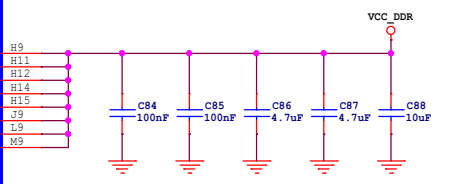


Note: Sequences can not be swap

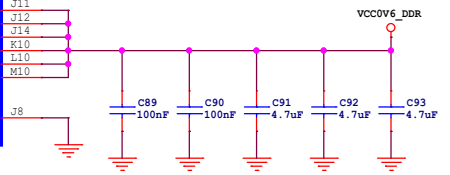


DDR_VREFOUT

DDR3L	=1.35V	DDRRHY_VDDQ_1	H9
DDR3	=1.5V	DDRRHY_VDDQ_2	H11
DDR4	=1.2V	DDRRHY_VDDQ_3	H12
LPDDR3	=1.2V	DDRRHY_VDDQ_4	H14
LPDDR4	=1.1V	DDRRHY_VDDQ_5	H15
LPDDR4x	=1.1V	DDRRHY_VDDQ_6	J9
		DDRRHY_VDDQ_7	L9
		DDRRHY_VDDQ_8	M9



DDR3L	=1.35V	DDRRHY_VDDQL_1	J11
DDR3	=1.5V	DDRRHY_VDDQL_2	J12
DDR4	=1.2V	DDRRHY_VDDQL_3	J14
LPDDR3	=1.2V	DDRRHY_VDDQL_4	K10
LPDDR4	=1.1V	DDRRHY_VDDQL_5	L10
LPDDR4x	=0.6V	DDRRHY_VDDQL_6	M10



Note: Except DDR3, other DQ sequences can not be swap

RK3568J

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RK3568J_L (VCCIO5 Domain)

U1L

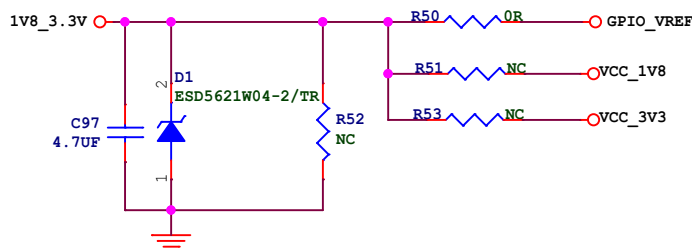
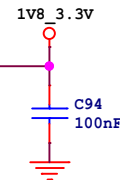
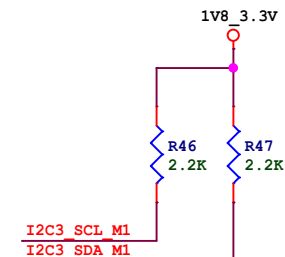
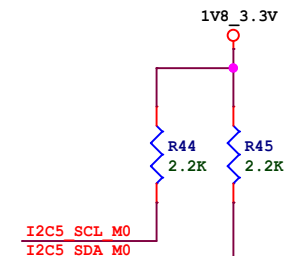
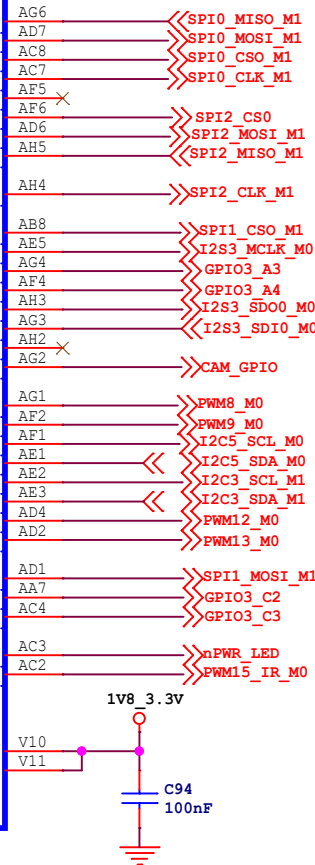
VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREOn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREOn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREOn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERStn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERStn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLR M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 D5	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D6	/ GMAC1 RXCLK M0	/ I2S3 SDI M0	/ SDMMC2 DET M1	/ GPIO3 A7 d
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 25M M0	/ I2S3 SDI M0	/ SDMMC2 PWREn M1	/ GPIO3 B0 d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERStn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d

VCCIO5_1
VCCIO5_2

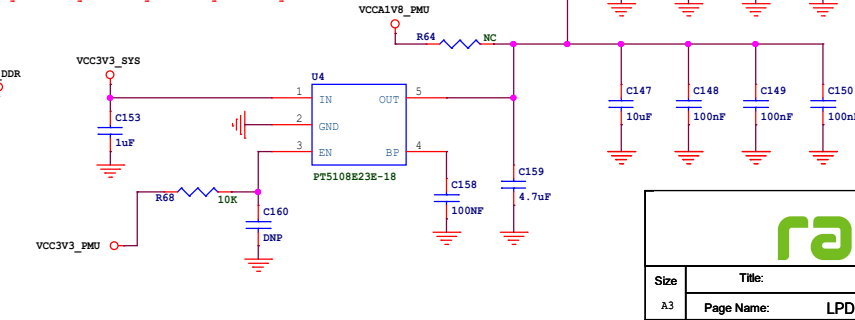
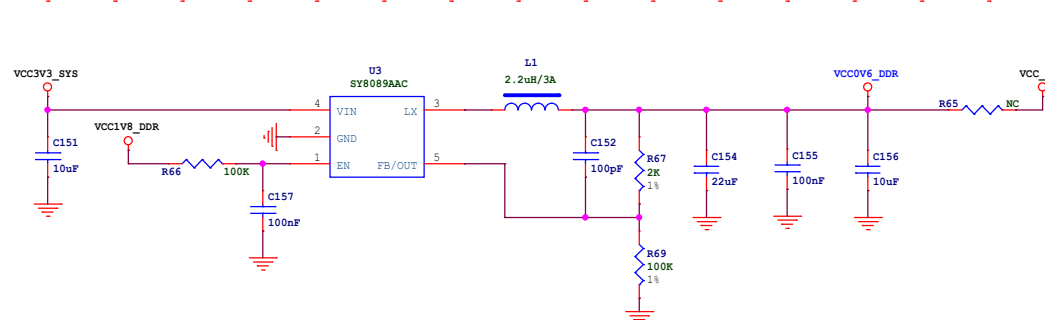
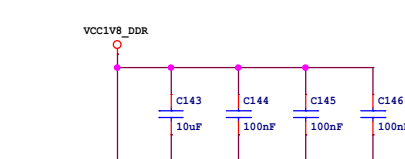
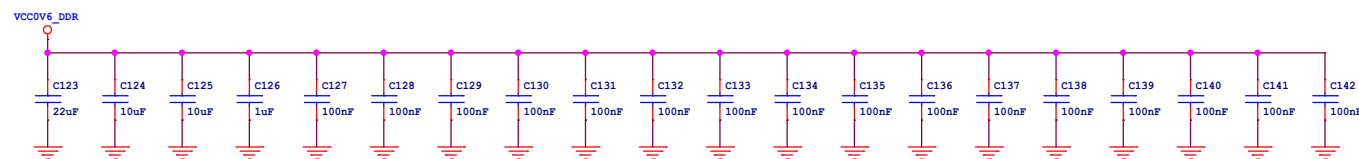
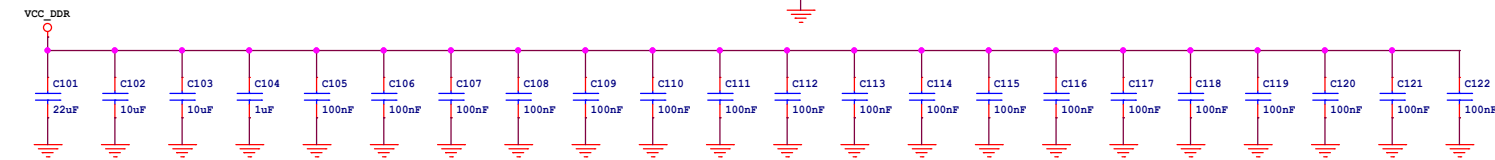
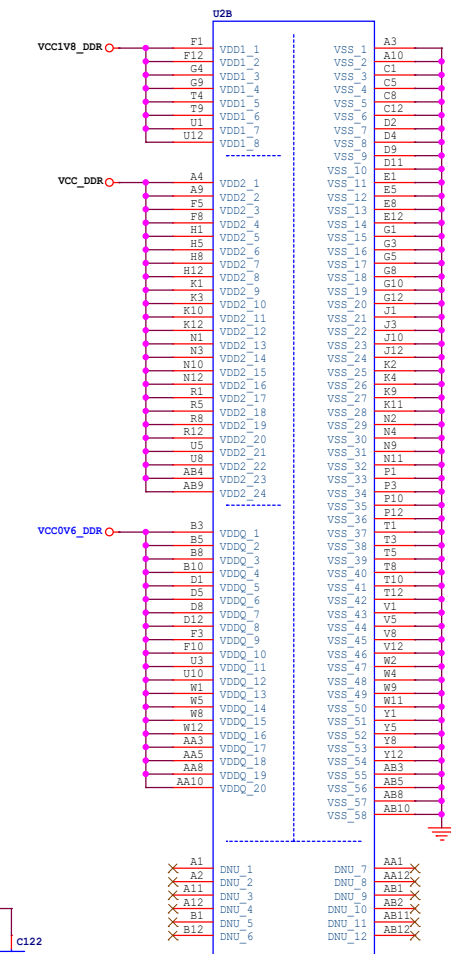
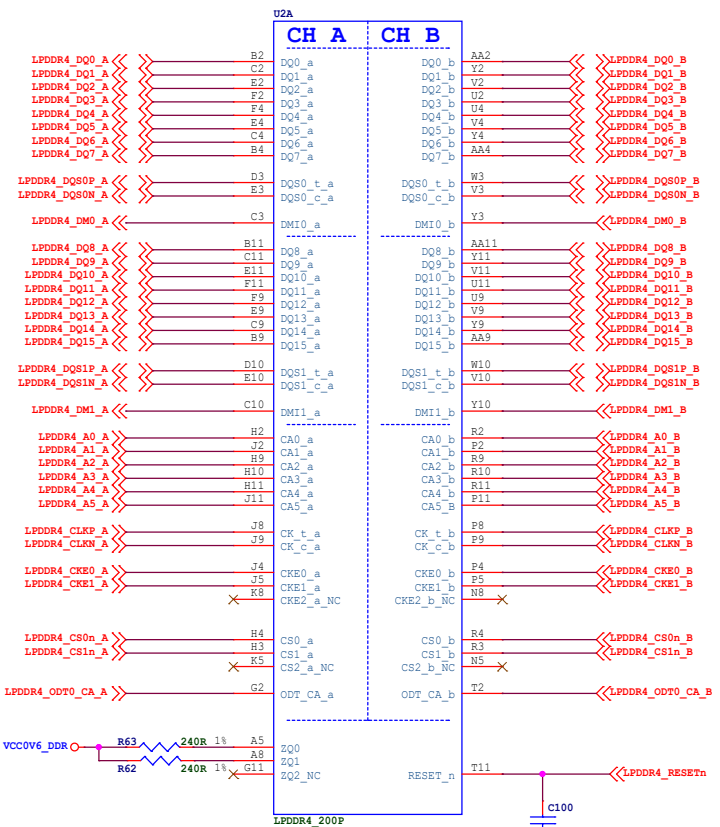
RK3568J



radxa

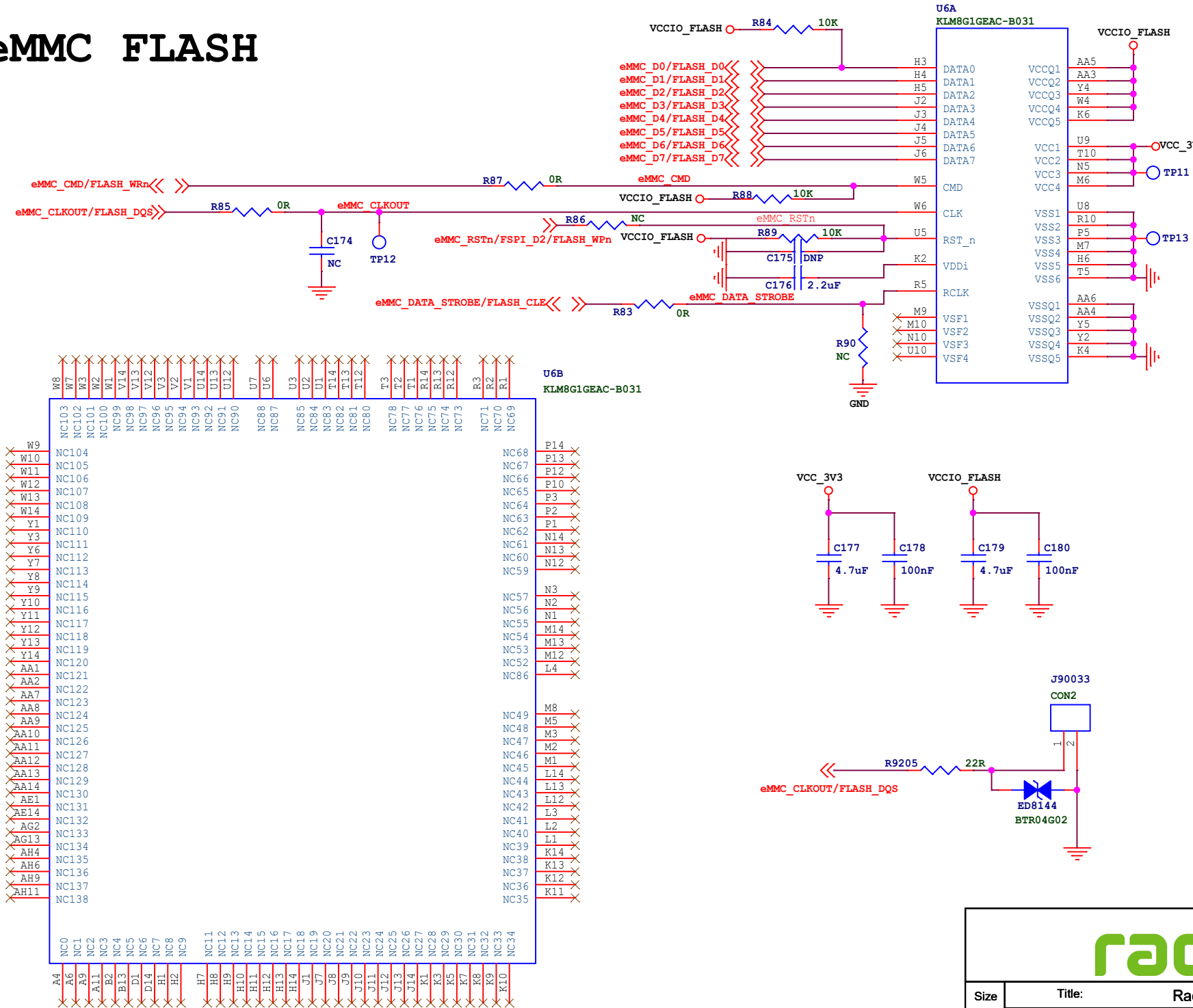
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Date:	Friday, January 10, 2025	Sheet	11 of 20

LPDDR4



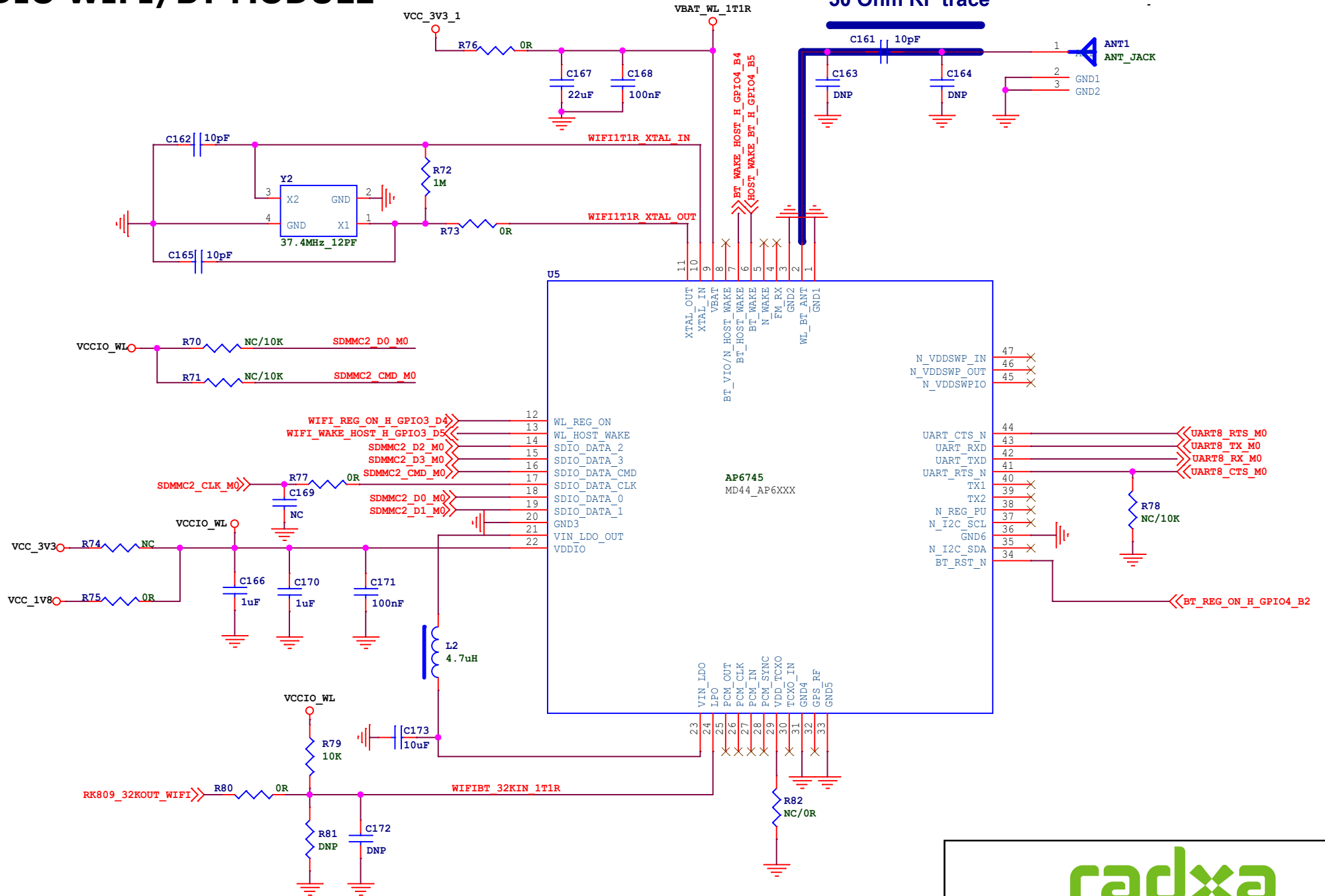
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Date:	Friday, January 10, 2025	Sheet	12 of 20


eMMC FLASH



Size	Title:	Radxa CM3J	REV
A4	Page Name:	eMMC	V1.2
Date:	Friday, January 10, 2025		Sheet 13 of 20

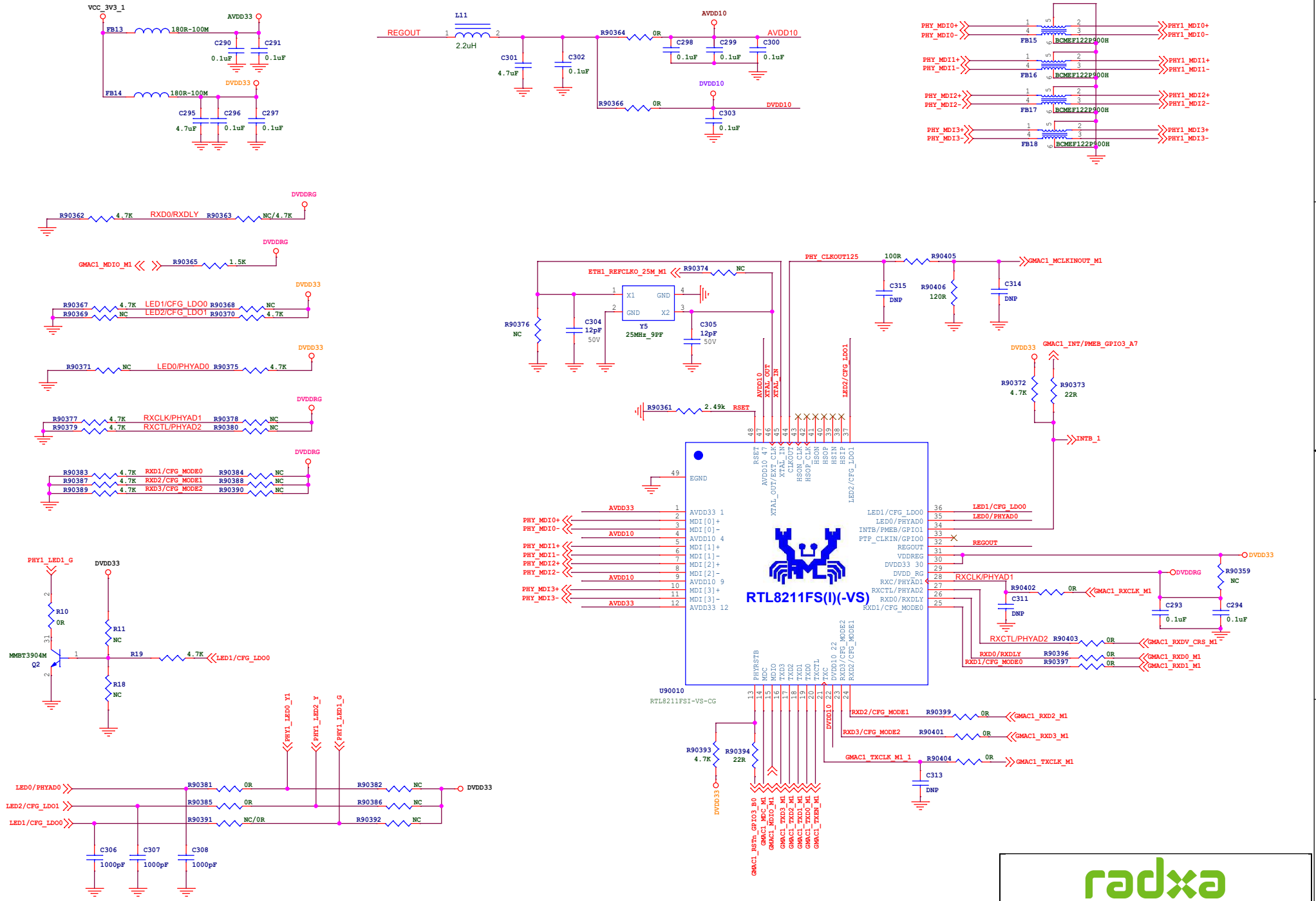
SDIO WIFI/BT MODULE






Size	Title: Radxa CM3J	REV
A4	Page Name: WIFI/BT	V1.2
Date: Friday, January 10, 2025		
Sheet 14 of 20		

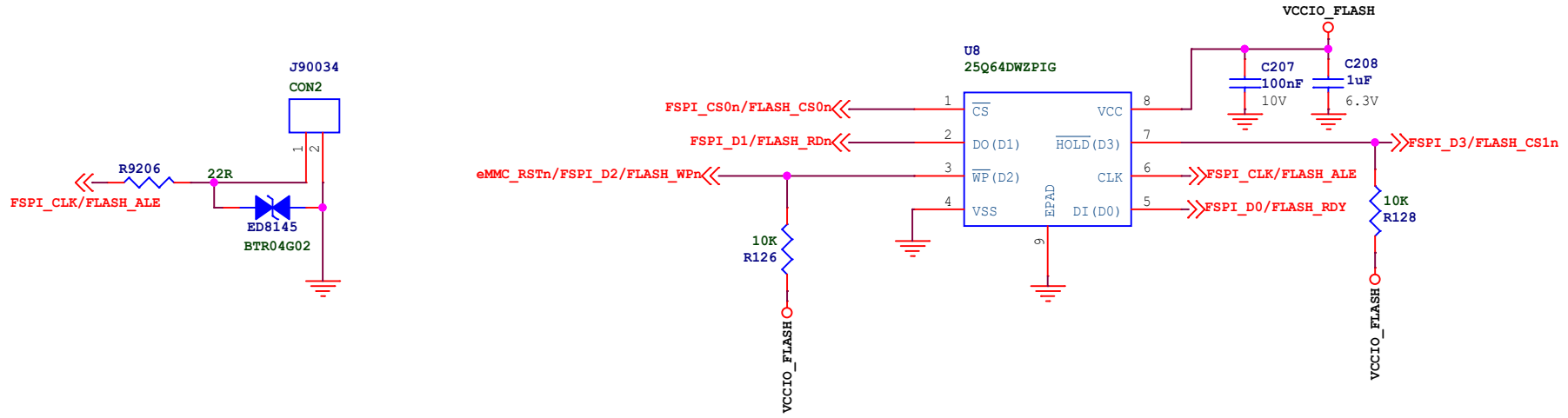
Ethernet



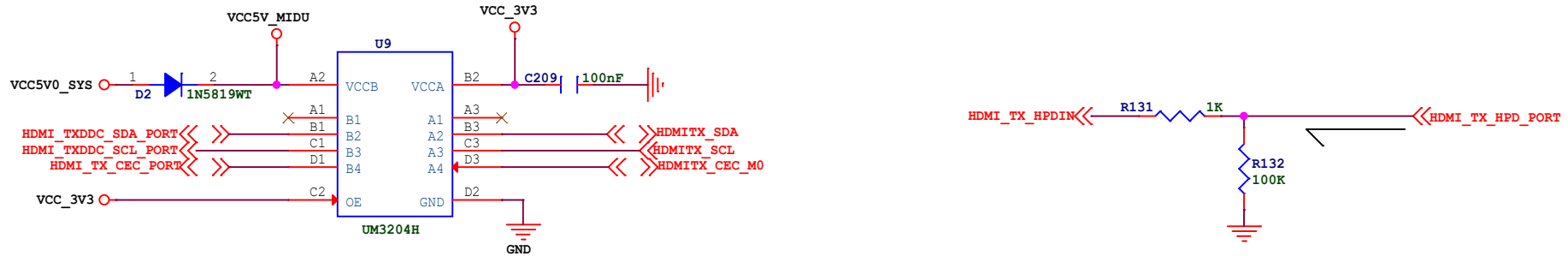


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Date:	Friday, January 10, 2025	Sheet 15 of 20

SPI FLASH

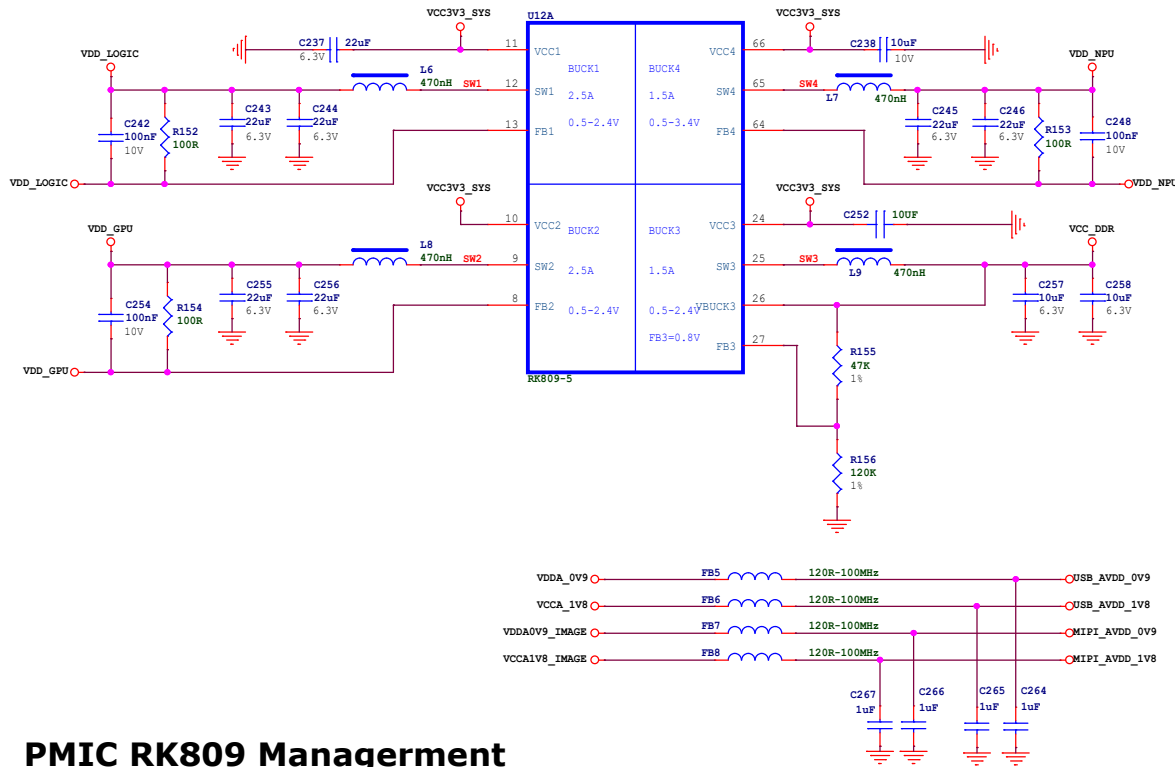


HDMI

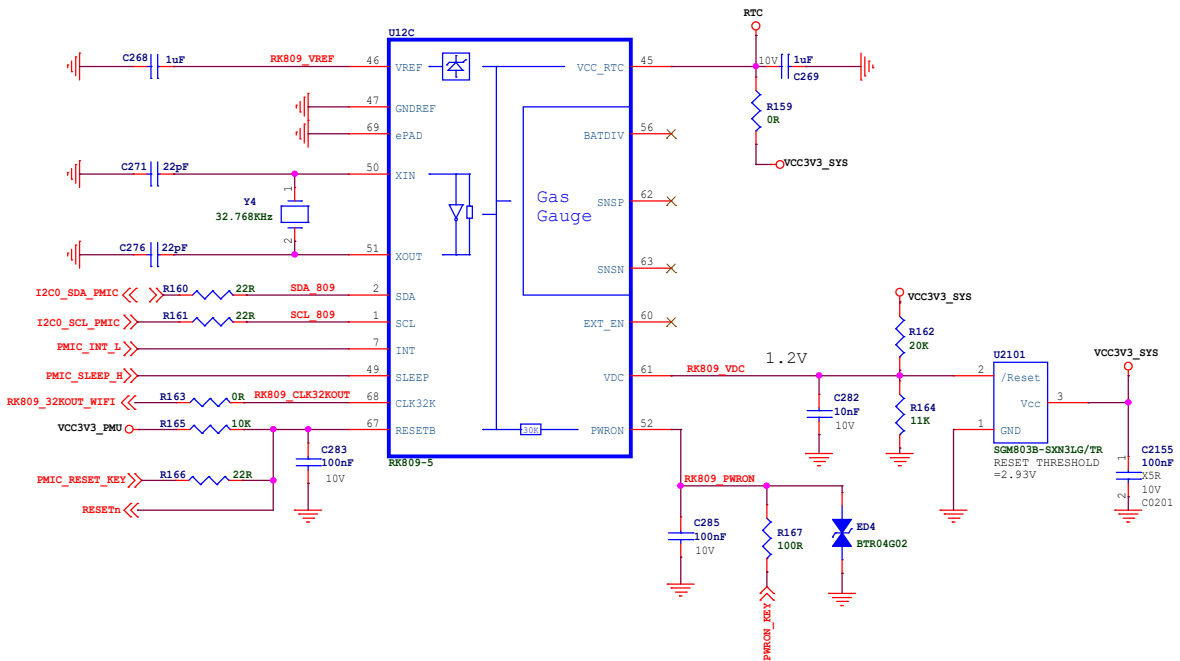


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A4	Page Name: Flash-SPI/HDMI	V1.2
Date: Friday, January 10, 2025	Sheet 16 of 20	

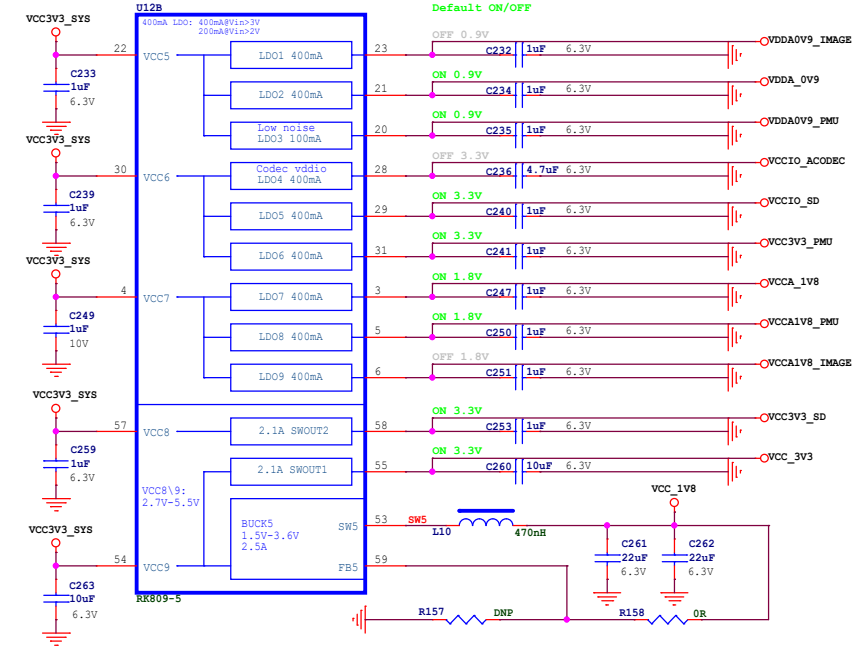
PMIC RK809 DCDC



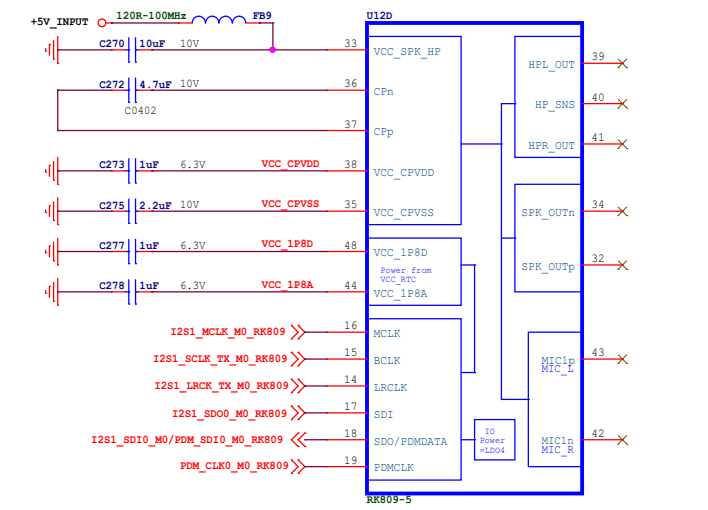
PMIC RK809 Management



PMIC RK809 LDO

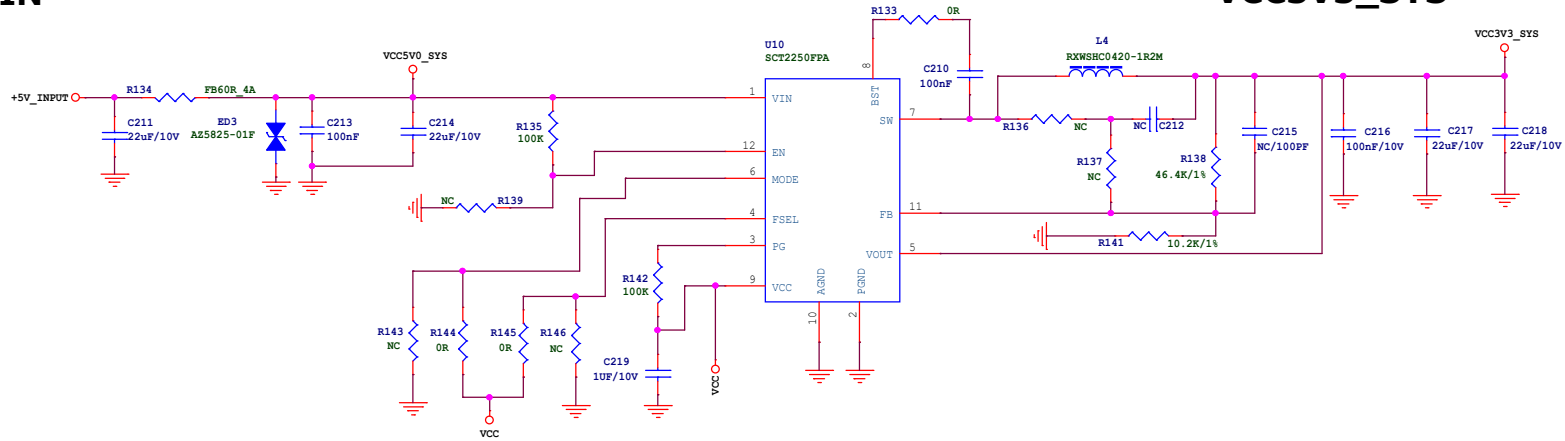


PMIC RK809 CODEC



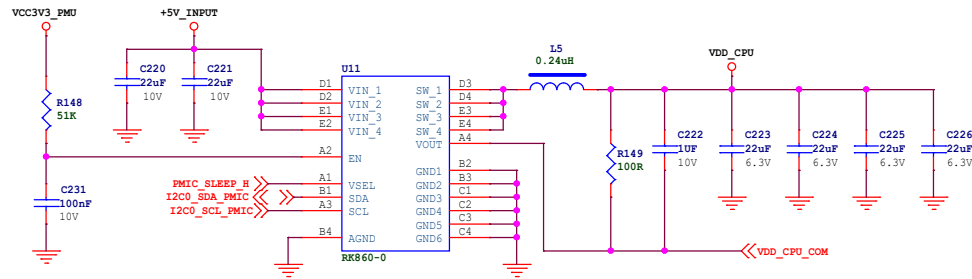
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Date:	Friday, January 10, 2025	Sheet 17	of 20

5V/3A DCIN

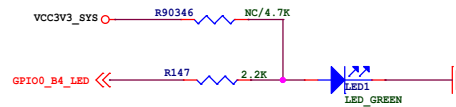
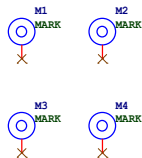
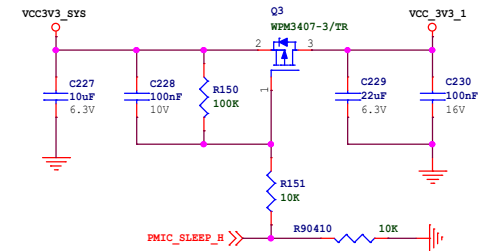


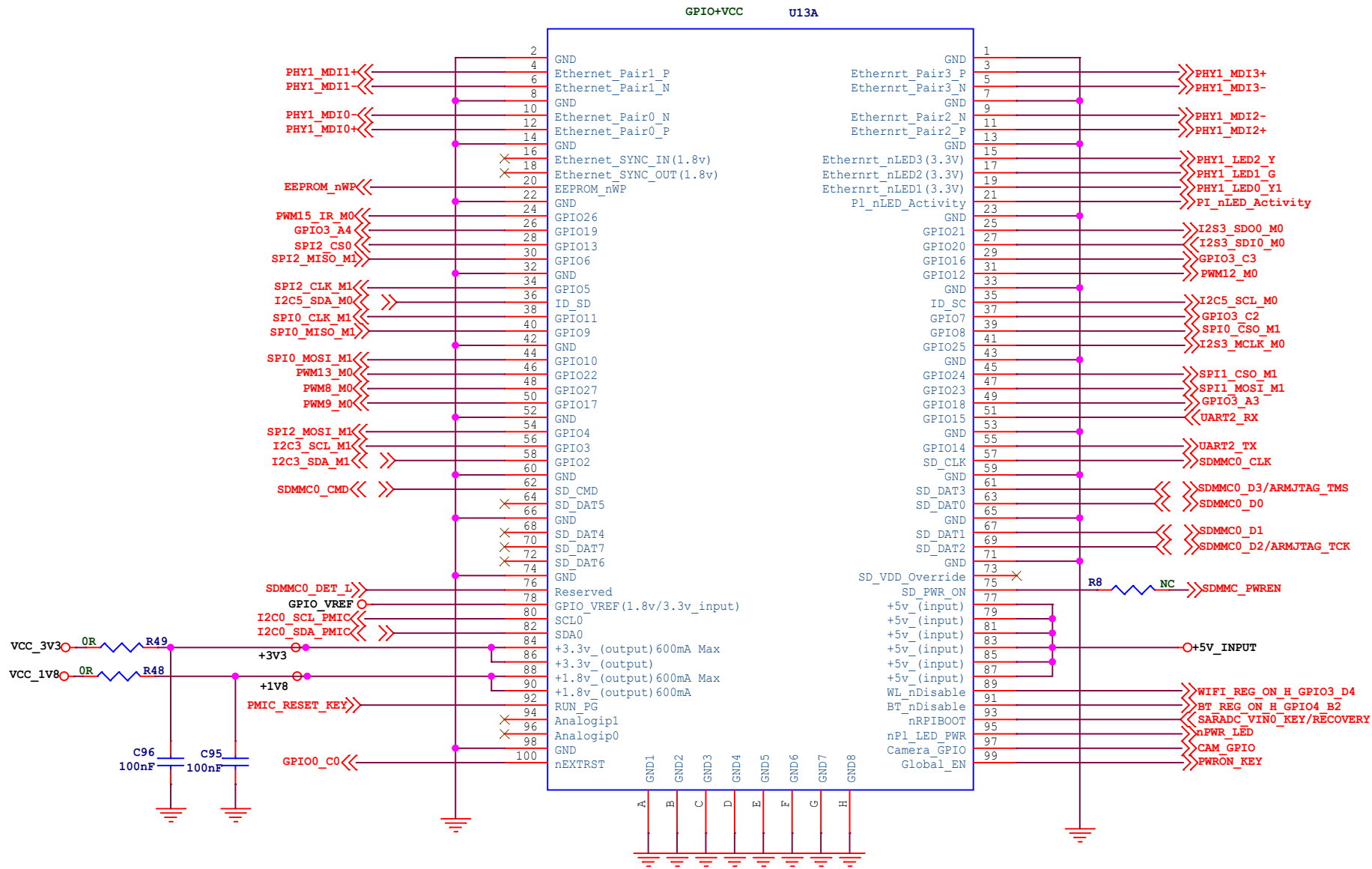
VCC3V3_SYS

VDD_CPU



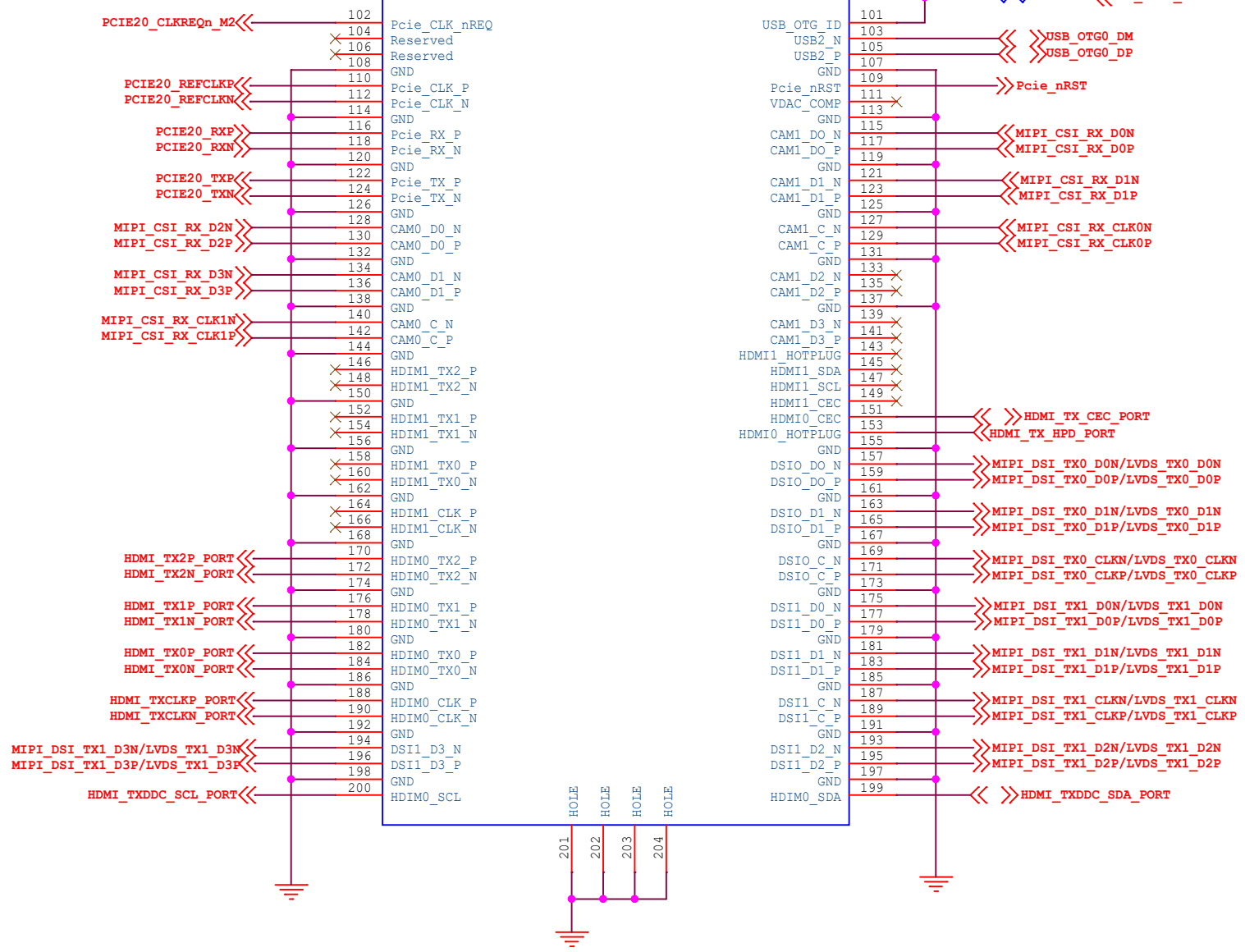
VCC_3V3 (Power OFF under SLEEP)





Size	Title: Radxa CM3J	REV
A4	Page Name: GPIO+VCC_Connector	V1.2
Date: Friday, January 10, 2025	Sheet	19 of 20

High Speed Serial U13B



Size	Title: Radxa CM3J	REV
A4	Page Name: High Speed Serial_Connector	V1.2
Date: Friday, January 10, 2025	Sheet 20 of 20	