Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Size: A3	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: Index and Notes	
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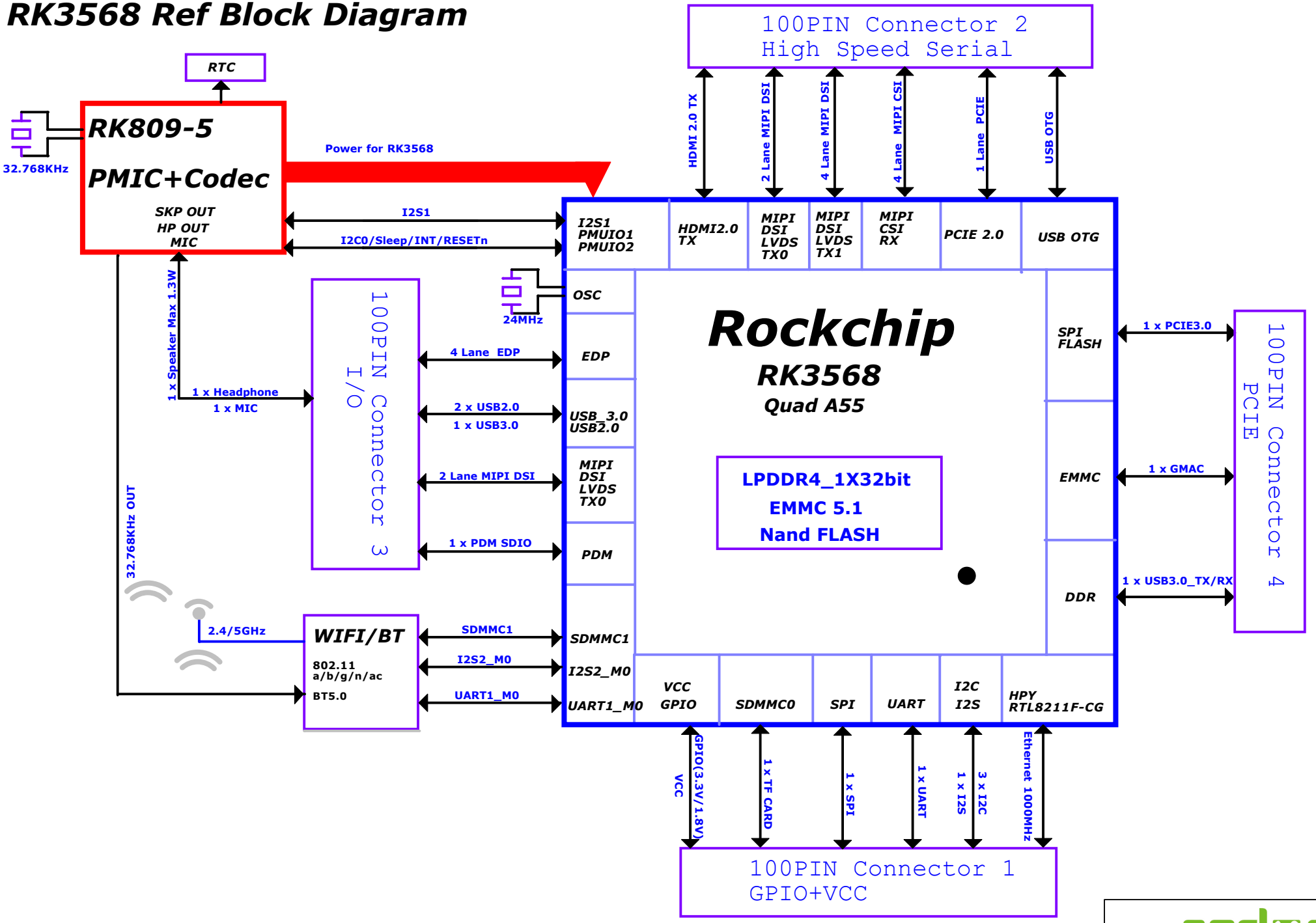
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-04-10		1:Revision preliminary version	
V1.1	2021-10-29			

RK3568 Ref Block Diagram



Size A3	Title: Rock 3 Compute Module Plus	REV V1.1
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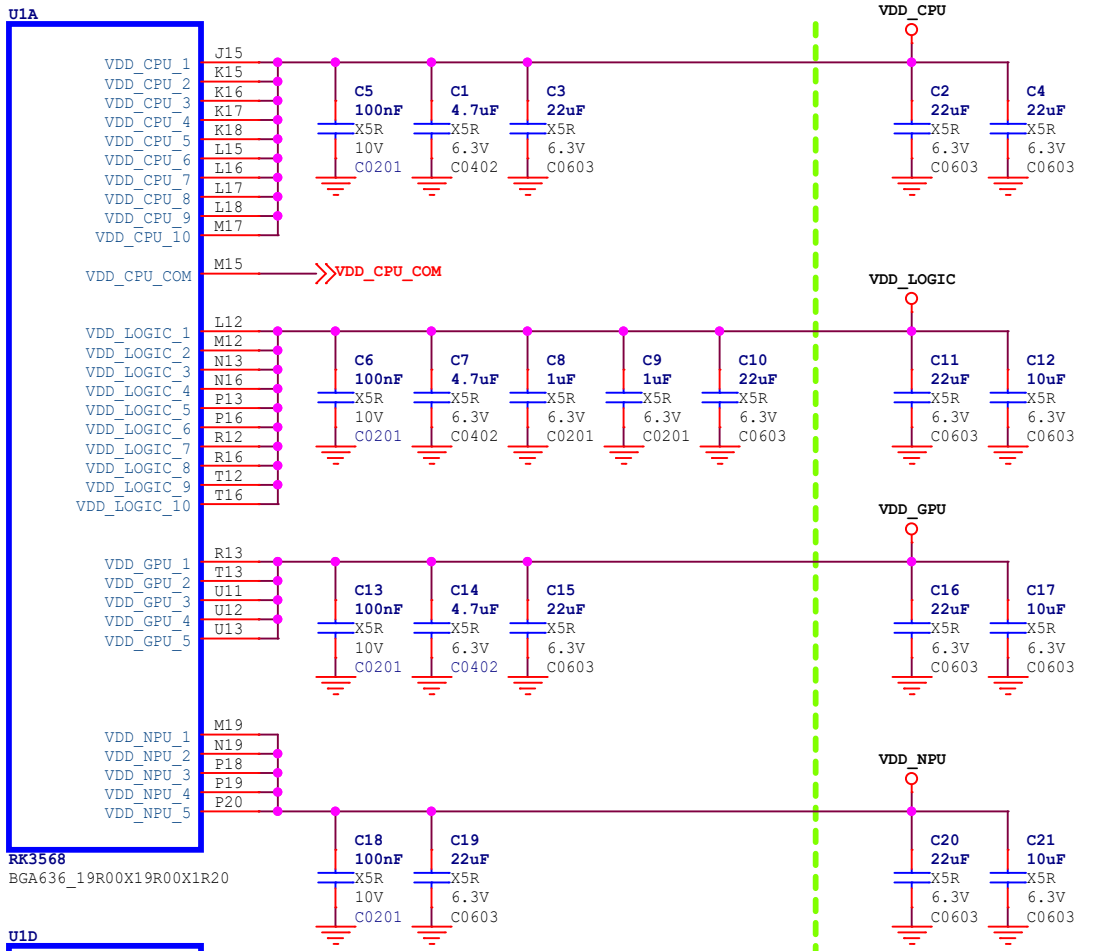
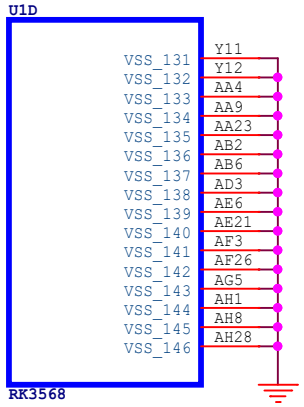
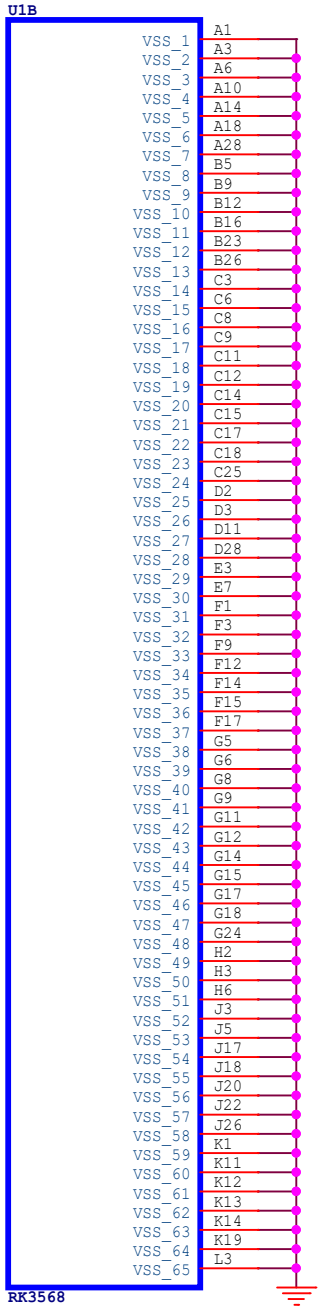
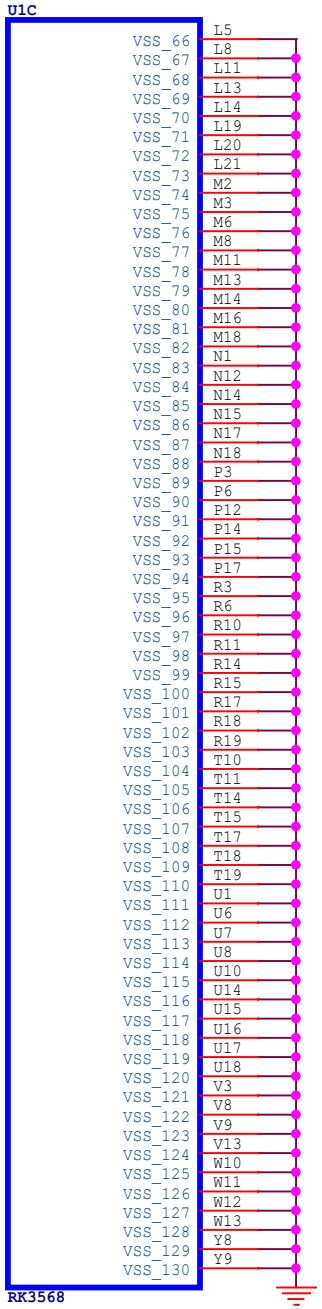
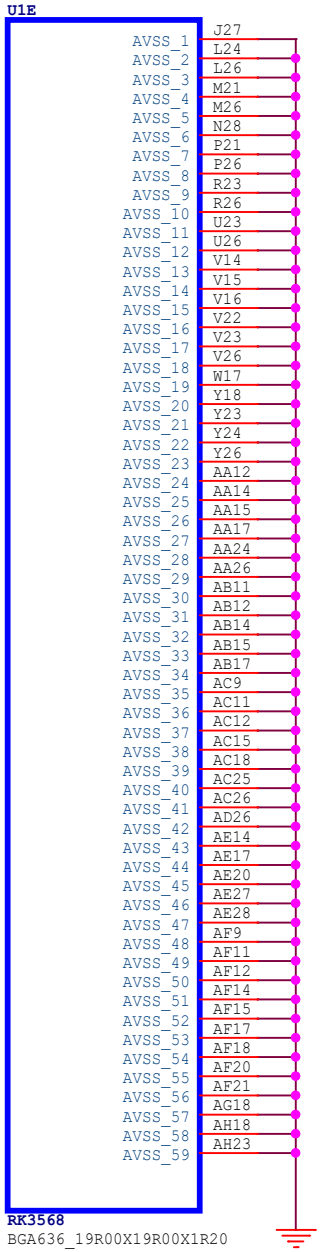
RK3568_ABCDE (Power&Gnd)











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Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	RK3568_Power/GND	V1.1
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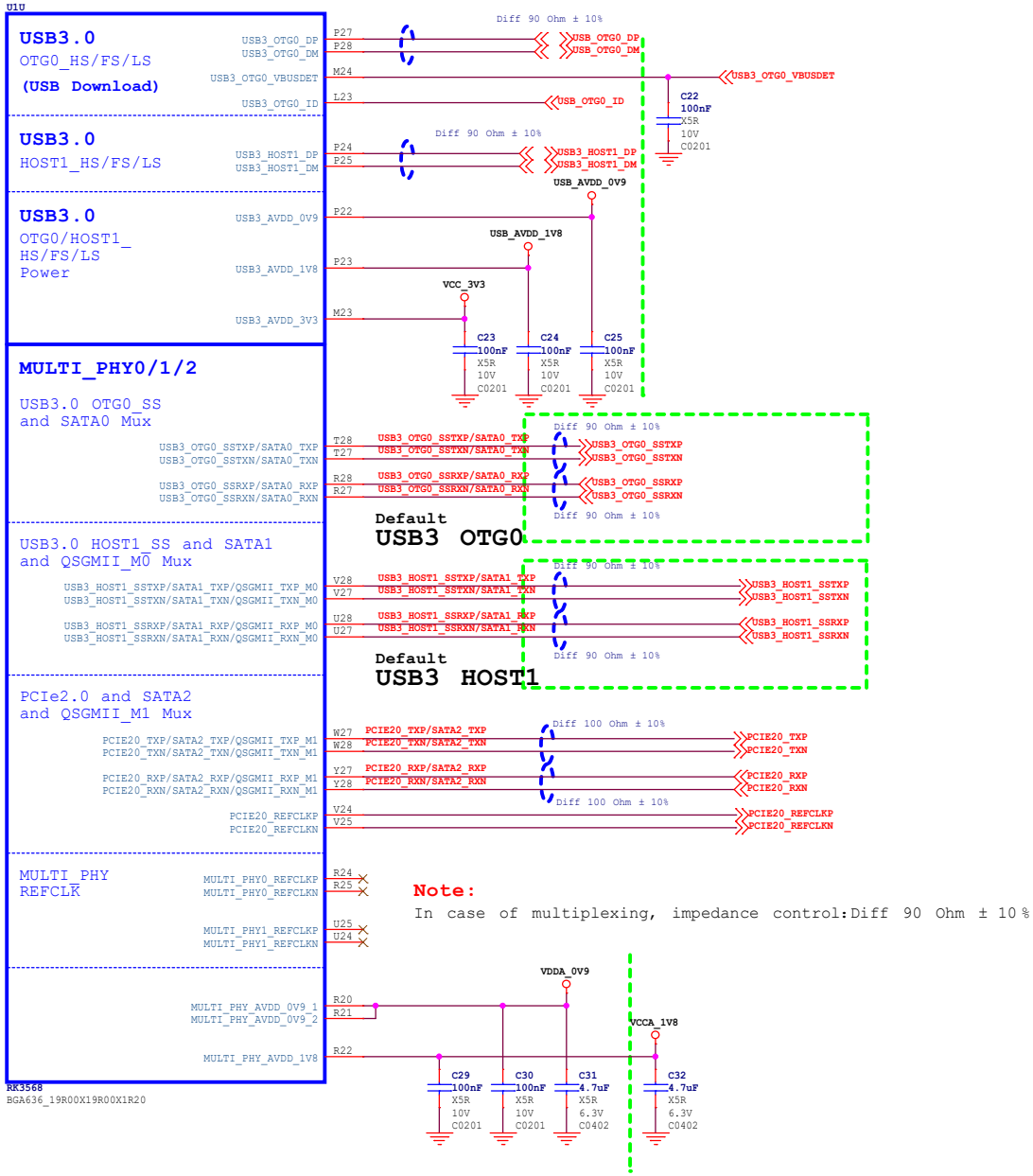
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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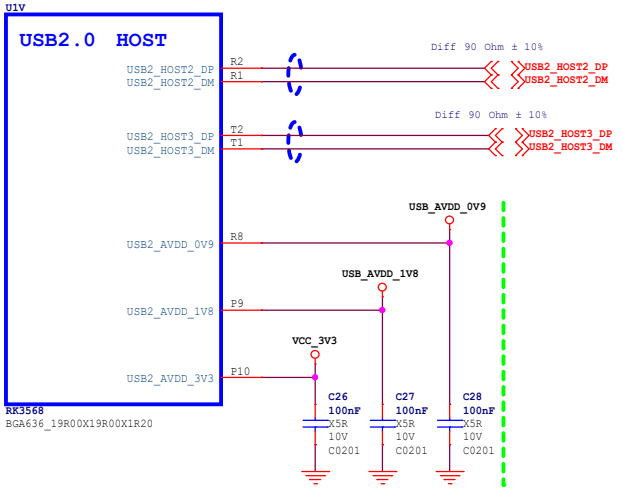
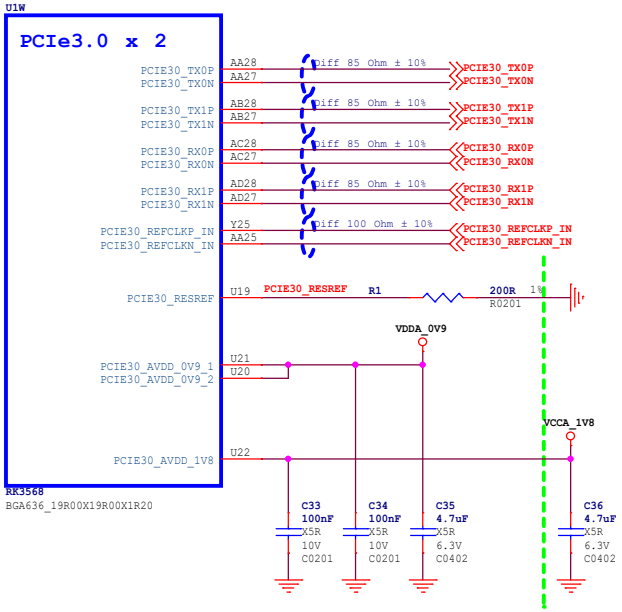
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Size A3	Title: Rock 3 Compute Module Plus		REV V1.1
	Page Name: RK3568_USB/PCIe/SATA PHY		
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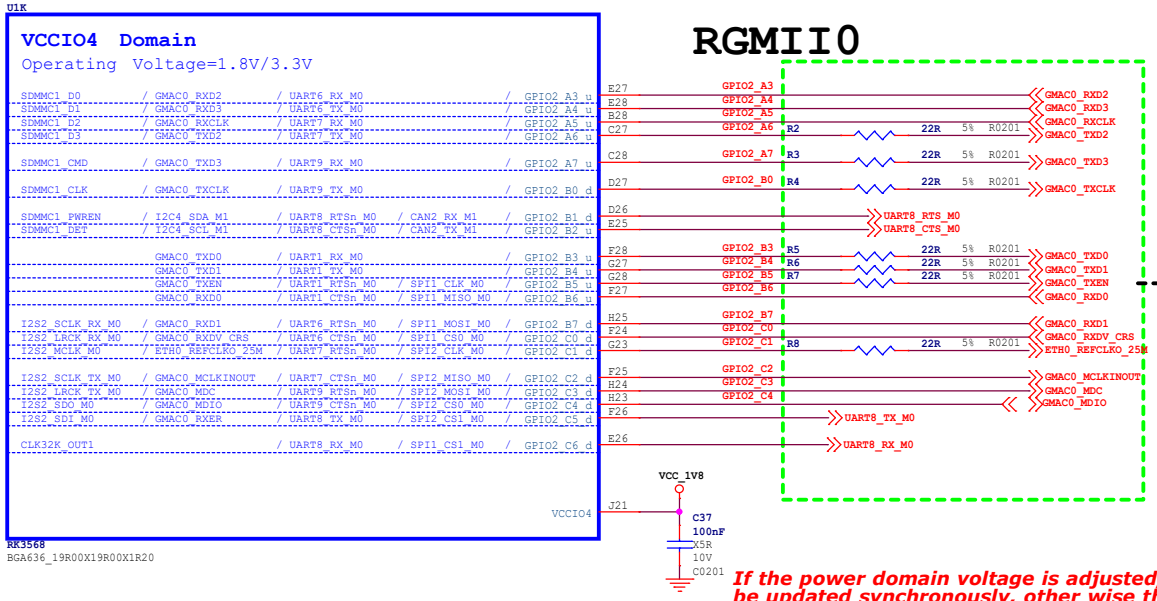
RK3568_K(VCCIO4 Domain)



RGMII0

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

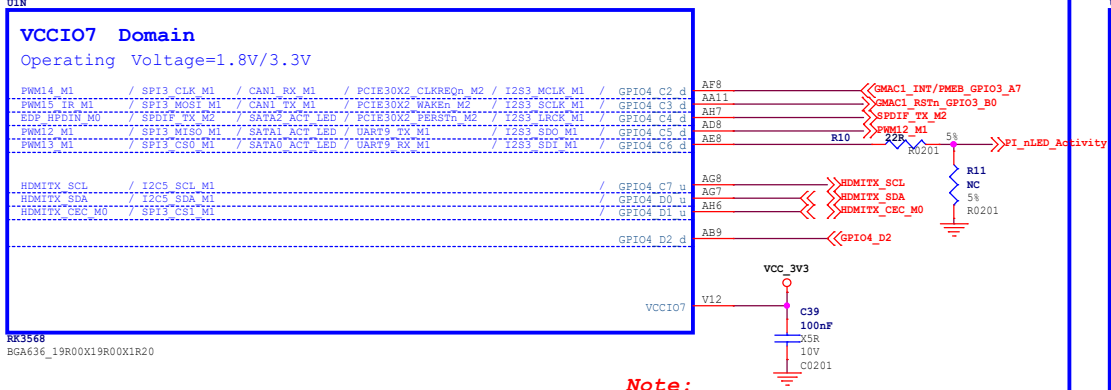
According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

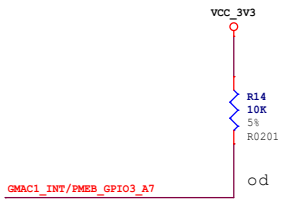
Note:

When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

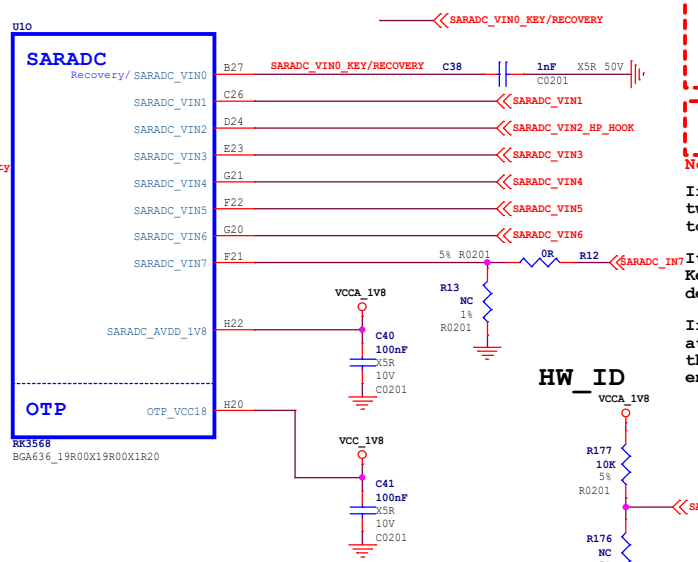


Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

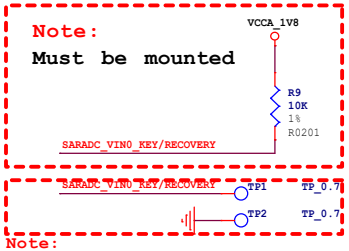


RK3568_O(SARADC/OTP)



Note:

Must be mounted



Note:

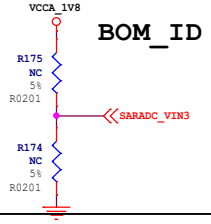
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

HW_ID

BOM_ID



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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A3	Page Name:	RK3568_ADC/RGMII0/HDMI	V1.1
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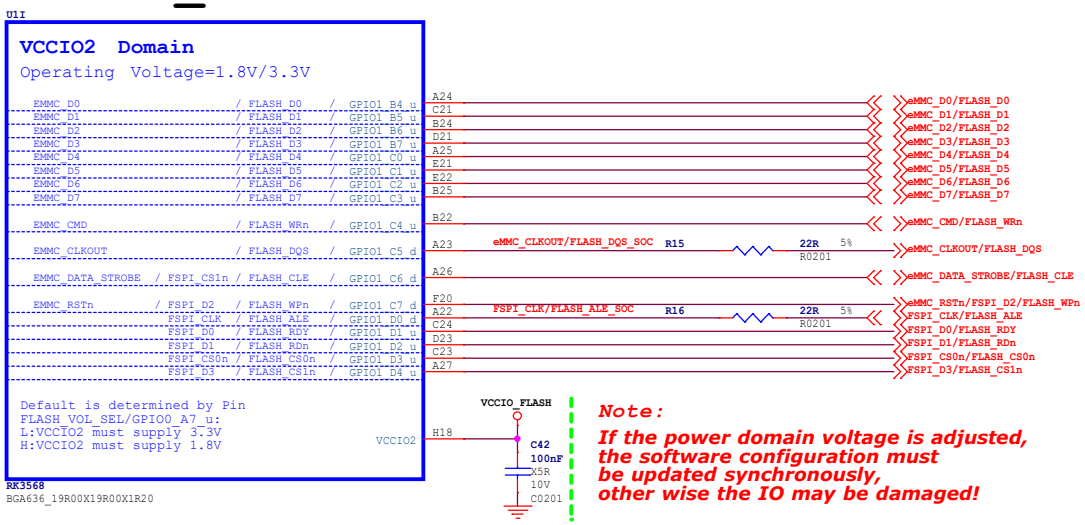
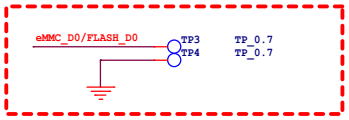
RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

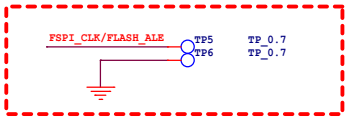


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

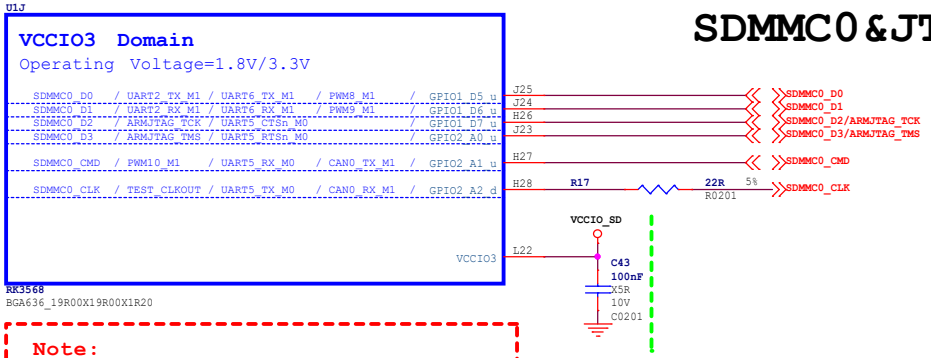
Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

Default

SDMMC0&JTAG



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Size A3	Title: Rock 3 Compute Module Plus	REV V1.1
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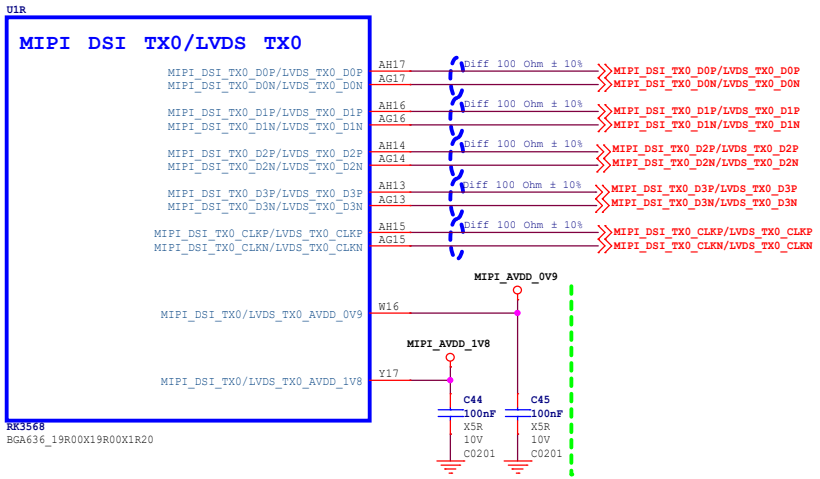
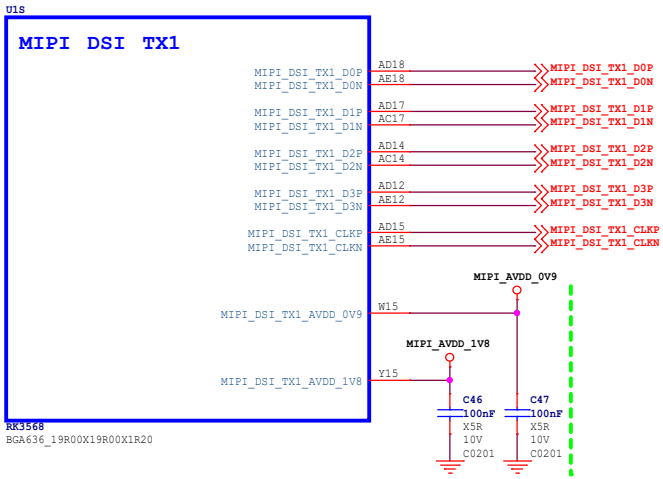
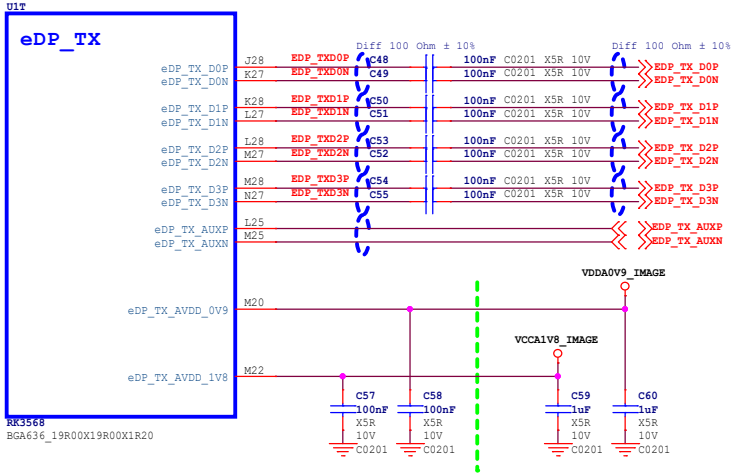
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
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Other caps should be placed close to the U1000 package

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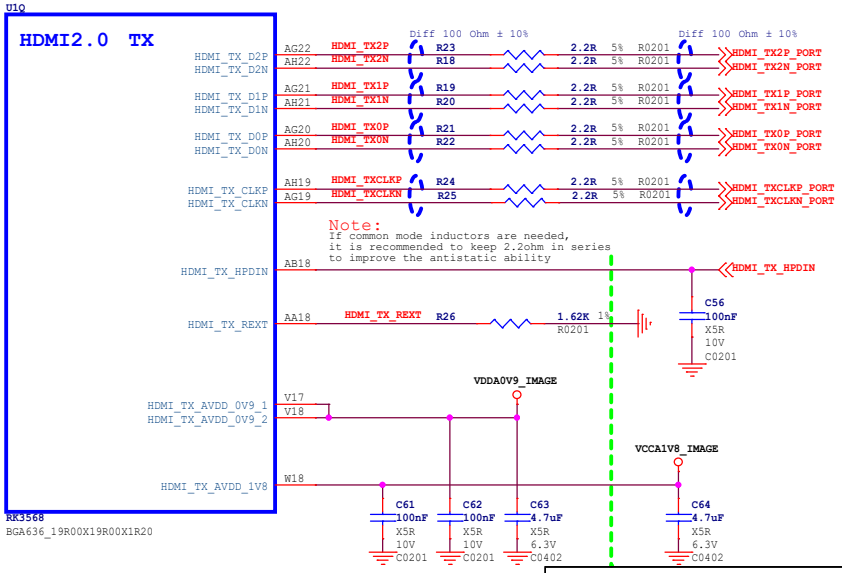
RK3568_Q(HDMI2.0 TX)



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	Page Name: RK3568_DSI_HDIM_EDP	
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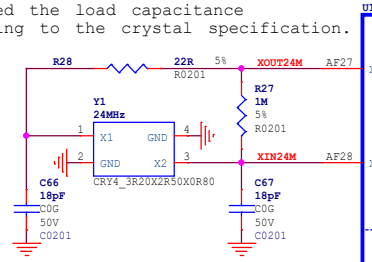
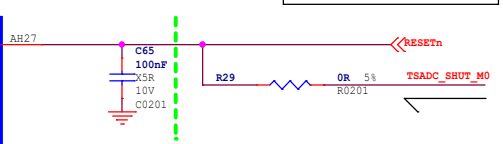
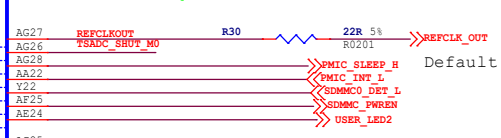
RK3568_G(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification.

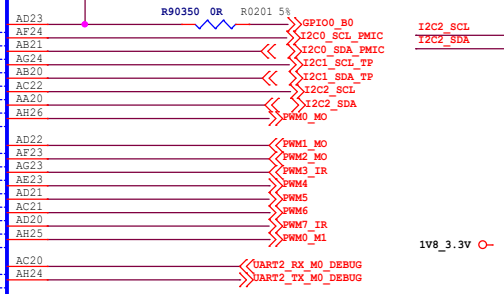


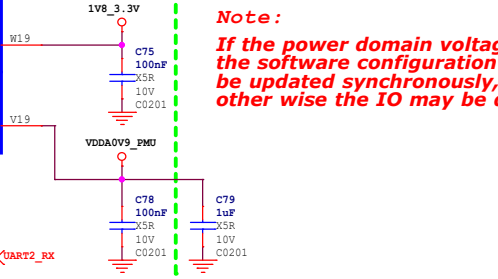
U1G

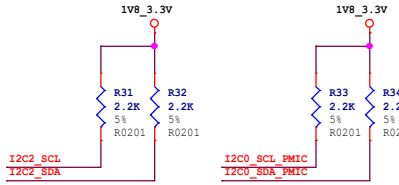


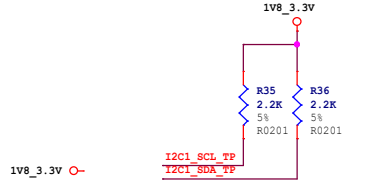


Default:24MHz

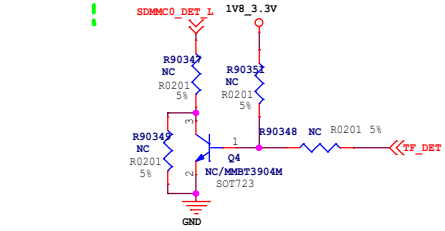




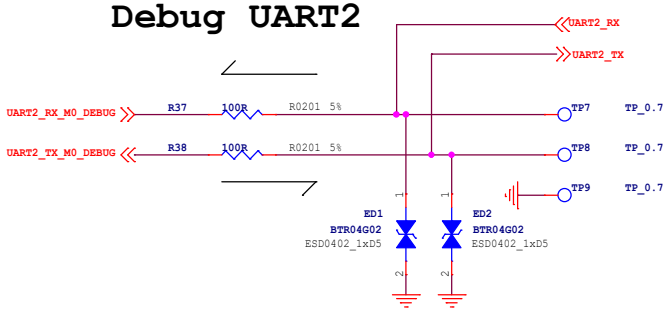


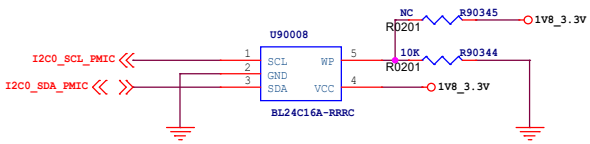


Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!



Debug UART2





Note:
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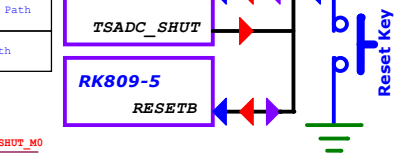
Other caps should be placed close to the U1000 package



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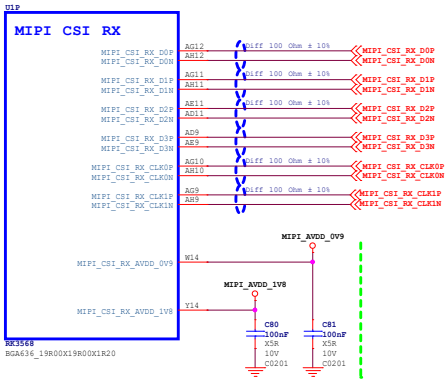
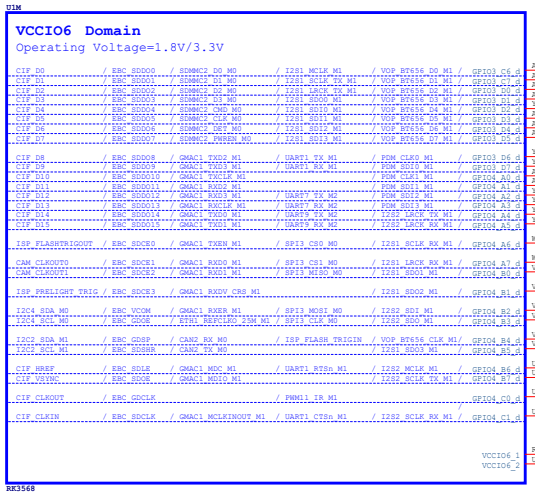
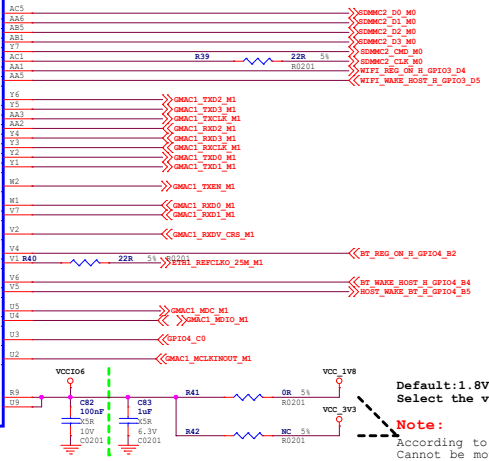
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)





Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN PHYx_CLKOUT125(Option)			
GMACx_MCLKINOUT	<-------		GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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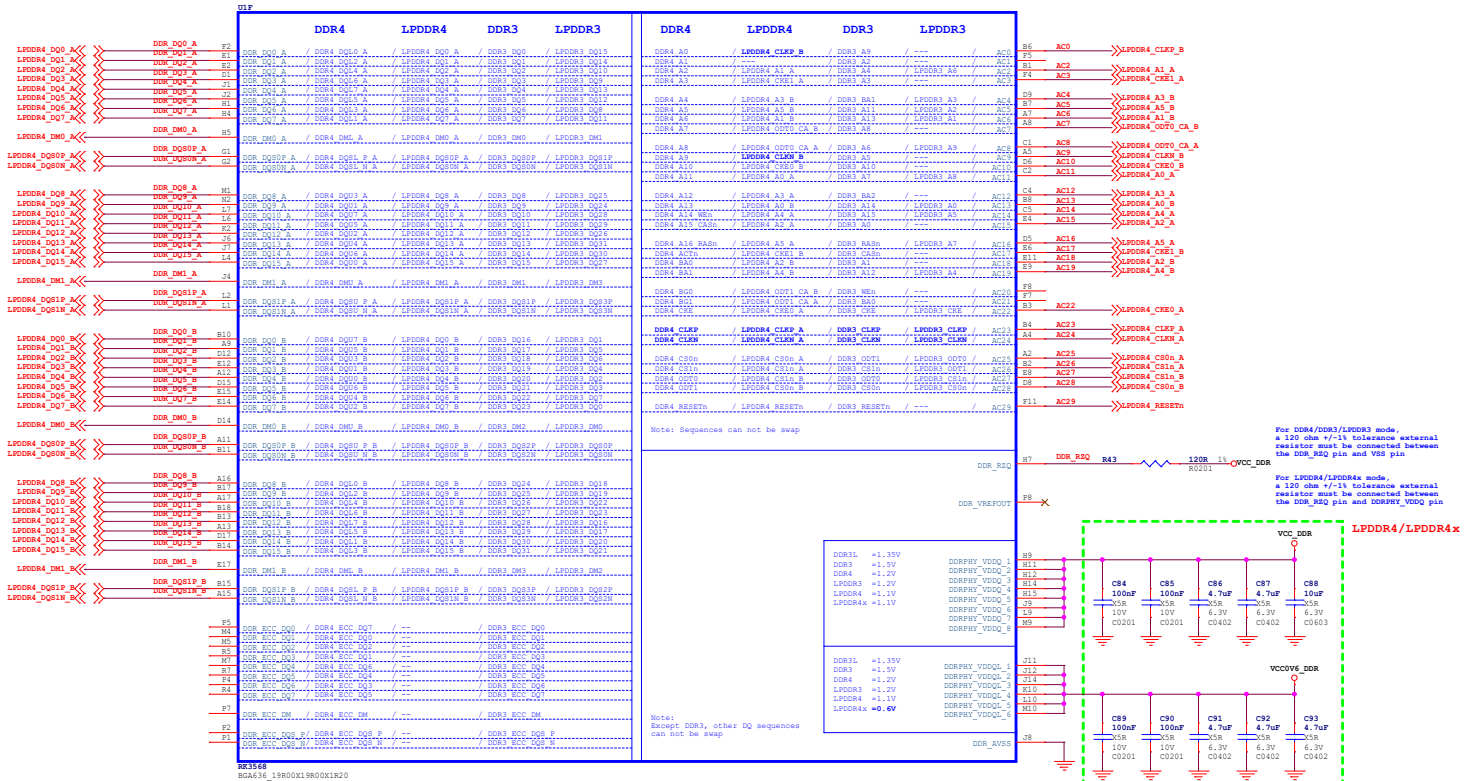
RK3568_F (DDR PHY)



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RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

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BGA636_19R00X19R00X1R20

AG6 SPI0_MISO_M1
AD7 SPI0_MOSI_M1
AC8 SPI0_CSO_M1
AC7 SPI0_CLK_M1
AF5 WL_nDis
AF6 SPI2_CS0
AD6 SPI2_MOSI_M1
AH5 SPI2_MISO_M1
AH4 SPI2_CLK_M1
AB8 SPI1_CSO_M1
AE5 I2S3_MCLK_M0
AG4 BT_nDis
AF4 I2S3_LRCK_RX_M0
AH3 I2S3_SDO0_M0
AG3 I2S3_SDI0_M0
AH2 GPIO3_A7
AG2 CAM_GPIO
AG1 PWM8_M0
AF2 PWM9_M0
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 I2C3_SCL_M1
AE3 I2C3_SDA_M1
AD4 PWM12_M0
AD2 PWM13_M0
AD1 SPI1_MOSI_M1
AA7 SPI1_MISO_M1
AC4 SPI1_CLK_M1
AC3 nPWR_LED
AC2 PWM15_IR_M0
V10 VCCIO5_1
V11 VCCIO5_2

1V8_3.3V
C94 100nF X5R 10V C0201

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

1V8_3.3V
R44 2.2K 5% R0201
R45 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

1V8_3.3V
R46 2.2K 5% R0201
R47 2.2K 5% R0201
I2C3_SCL_M1
I2C3_SDA_M1

+1V8 R48 0R R0603 5% VCC_1V8
+3V3 R49 0R R0603 5% VCC_3V3
C95 100nF X5R 10V C0201
C96 100nF X5R 10V C0201

1V8_3.3V
C97 4.7UF X5R 6.3V C0402
D1 TVS SOD_323
R52 NC 5% R0201
R50 0R R0603 5% GPIO_VREF
R51 NC R0201 5% VCC_1V8
R53 NC R0201 5% VCC_3V3

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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A4	Page Name:	RK3568_GPIO2_GPIO3	V1.1
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RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

D18 — GPIO1_A0
E18 — GPIO1_A1

A19 — I2S1_MCLK_M0_SOC — R54 22R 5% R0201 — I2S1_MCLK_M0_RK809

B19 — I2S1_SCLK_TX_M0_SOC — R55 22R 5% R0201 — I2S1_SCLK_TX_M0_RK809

F18 — GPIO1_A4

A20 — I2S1_LRCK_TX_M0_SOC — R56 22R 5% R0201 — I2S1_LRCK_TX_M0_RK809

C20 — PDM_CLK0_M0_SOC — R57 22R 5% R0201 — PDM_CLK0_M0_RK809

B20 — I2S1_SDO0_M0_RK809
D20 — PCIE20_CLKREQn_M2
E20 — GPIO1_B1
A21 — Pcie_nRST
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17 — C98 100nF X5R 10V C0201

Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Size	Title:	Rock 3 Compute Module Plus	REV
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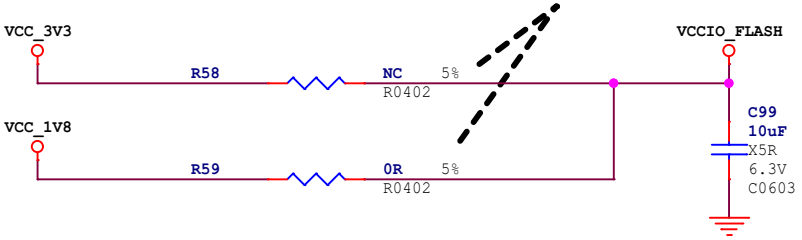
FLASH_VOL_SEL

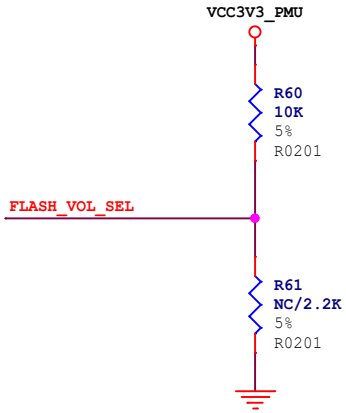
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven

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Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	Power_Flash Power Manage	V1.1
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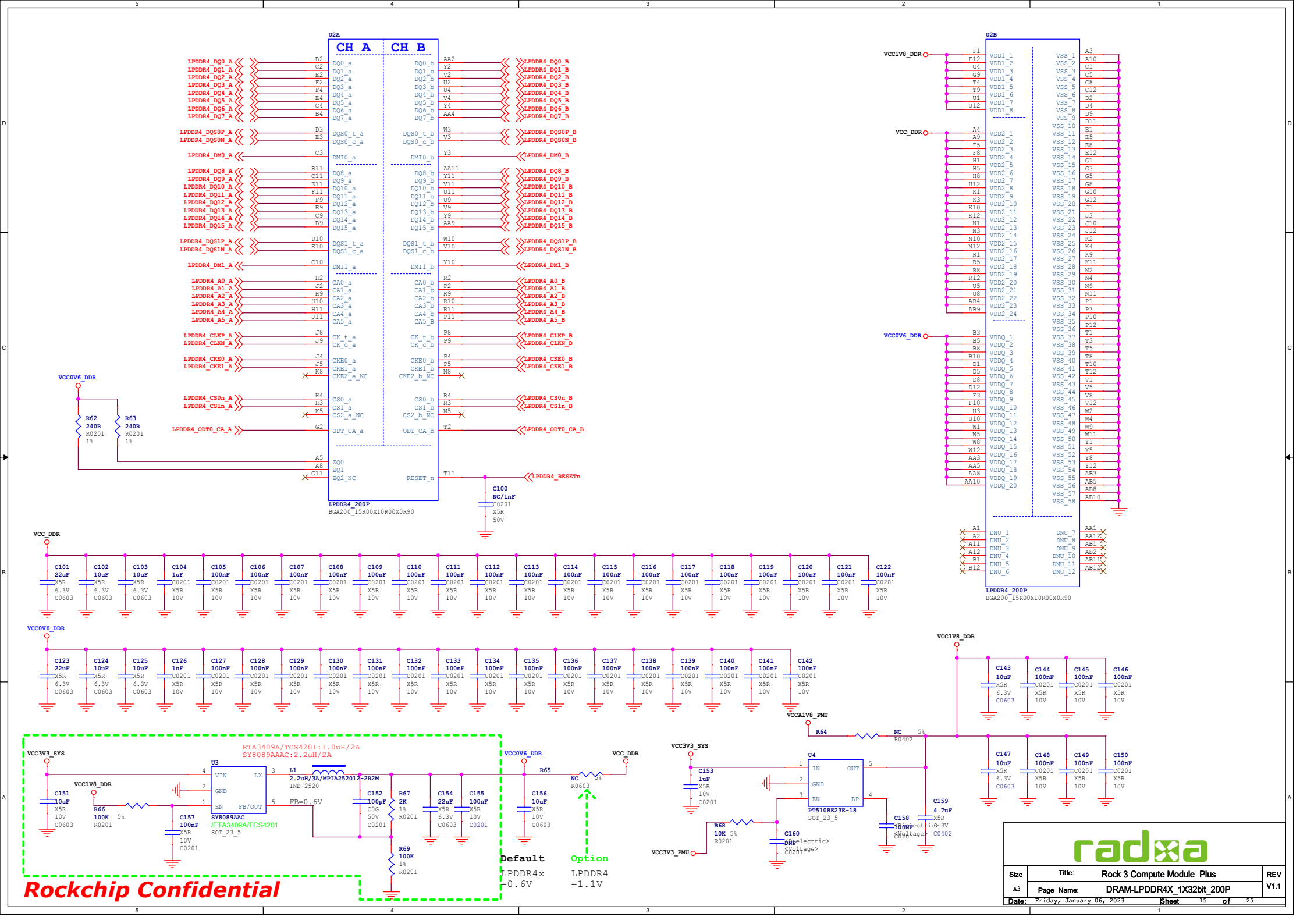
U2A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U2B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R62 240R R0201 1%
R63 240R R0201 1%
C100 NC/1nF C0201 X5R 50V
C101 22uF X5R 6.3V C0603
C102 10uF X5R 6.3V C0603
C103 10uF X5R 6.3V C0603
C104 1uF C0201 X5R 10V
C105 100nF C0201 X5R 10V
C106 100nF C0201 X5R 10V
C107 100nF C0201 X5R 10V
C108 100nF C0201 X5R 10V
C109 100nF C0201 X5R 10V
C110 100nF C0201 X5R 10V
C111 100nF C0201 X5R 10V
C112 100nF C0201 X5R 10V
C113 100nF C0201 X5R 10V
C114 100nF C0201 X5R 10V
C115 100nF C0201 X5R 10V
C116 100nF C0201 X5R 10V
C117 100nF C0201 X5R 10V
C118 100nF C0201 X5R 10V
C119 100nF C0201 X5R 10V
C120 100nF C0201 X5R 10V
C121 100nF C0201 X5R 10V
C122 100nF C0201 X5R 10V
C123 22uF X5R 6.3V C0603
C124 10uF X5R 6.3V C0603
C125 10uF X5R 6.3V C0603
C126 1uF C0201 X5R 10V
C127 100nF C0201 X5R 10V
C128 100nF C0201 X5R 10V
C129 100nF C0201 X5R 10V
C130 100nF C0201 X5R 10V
C131 100nF C0201 X5R 10V
C132 100nF C0201 X5R 10V
C133 100nF C0201 X5R 10V
C134 100nF C0201 X5R 10V
C135 100nF C0201 X5R 10V
C136 100nF C0201 X5R 10V
C137 100nF C0201 X5R 10V
C138 100nF C0201 X5R 10V
C139 100nF C0201 X5R 10V
C140 100nF C0201 X5R 10V
C141 100nF C0201 X5R 10V
C142 100nF C0201 X5R 10V
VCCA1V8_PMU
R64 NC 5% R0402
C143 10uF X5R 6.3V C0603
C144 100nF C0201 X5R 10V
C145 100nF C0201 X5R 10V
C146 100nF C0201 X5R 10V
C147 10uF X5R 6.3V C0603
C148 100nF C0201 X5R 10V
C149 100nF C0201 X5R 10V
C150 100nF C0201 X5R 10V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
VCC3V3_SYS
U3
VIN
LX
GND
EN
FB/OUT
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L1
2.2uH/3A/MPIA252012-2R2M
IND-2520
FB=0.6V
C151 10uF X5R 10V C0603
R66 100K 5% R0201
C157 100nF X5R 10V C0201
C152 100pF C0G 50V C0201
R67 2K 1% R0201
C154 22uF X5R 6.3V C0603
C155 100nF X5R 10V C0201
R69 100K 1% R0201
VCC0V6_DDR
R65 NC 5% R0603
VCC_DDR
C156 10uF X5R 10V C0603
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCC3V3_SYS
C153 1uF X5R 10V C0201
U4
IN
OUT
GND
EN
BP
PT5108E23E-18
SOT_23_5
R68 10K 5% R0201
VCC3V3_PMU
C160 <Electric> <Voltage> C0201
C158 100nF X5R 6.3V C0201
C159 4.7uF <Electric> <Voltage> C0402
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Size A3
Title: Rock 3 Compute Module Plus
REV V1.1
Page Name: DRAM-LPDDR4X_1X32bit_200P
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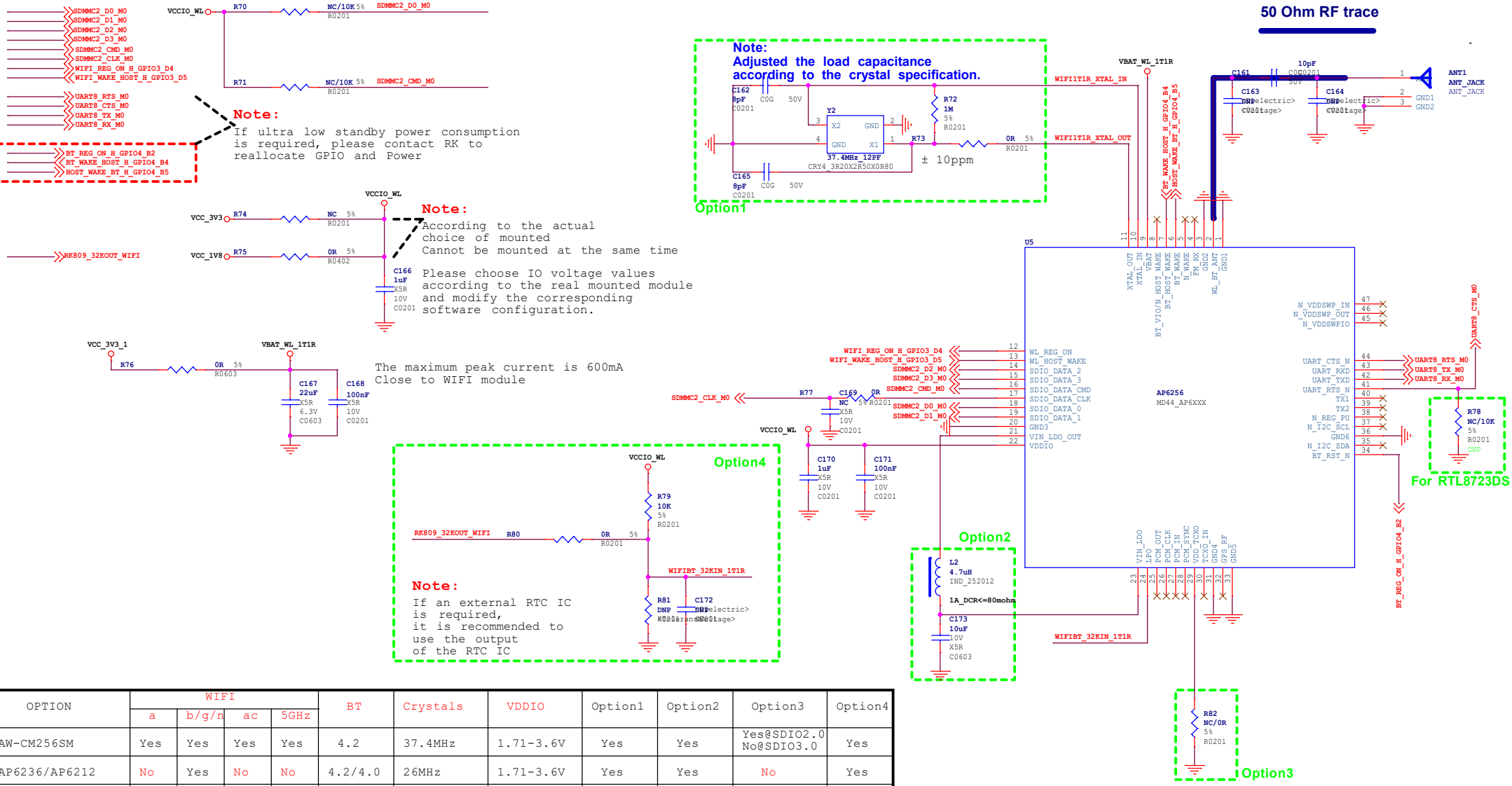
SDIO WIFI/BT MODULE

And Giga PHY0 Option



OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Using RTL8189ETV/FTV modules,please notice WIFI REG ON is on pin12 or pin34, choose according to the actual condition.

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

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A3	Page Name:	WIFI/BT	V1.1
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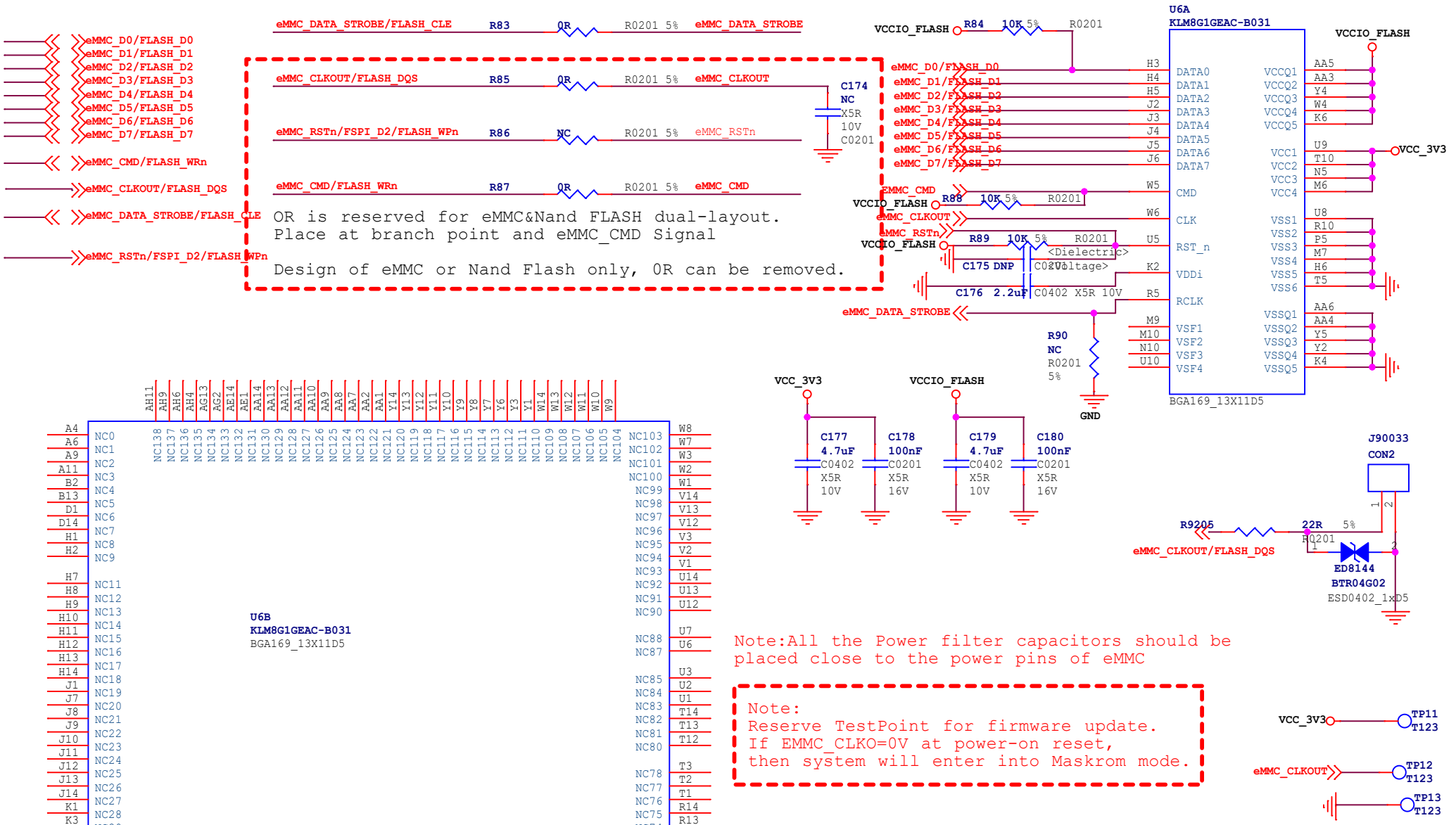
eMMC FLASH



Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	Memory-eMMC	V1.1
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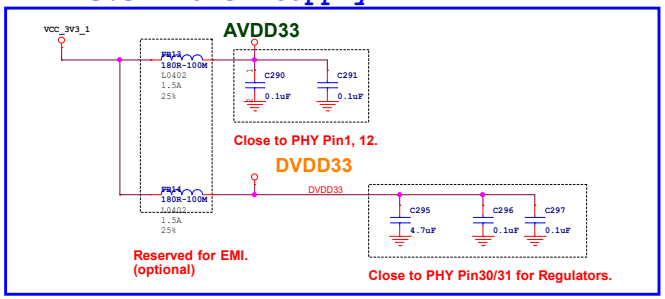
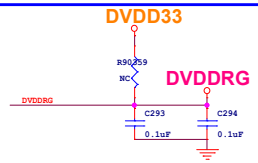
3.3V Power Supply



RGMII Power



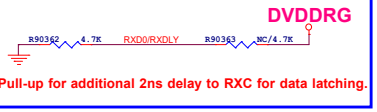
Note 1: R5 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

Note 2: DVDDRG must be short (or R5 be mounted) to DVDD33 if the external RGMII 3.3V is selected.

Note 3: R5 must be removed if the internal 2.5V/1.8V/1.5V RGMII is selected.

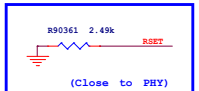
Note 4: CAPs must be closed to pin29 for EMI consideration.

RGMII RXC Delay Config.

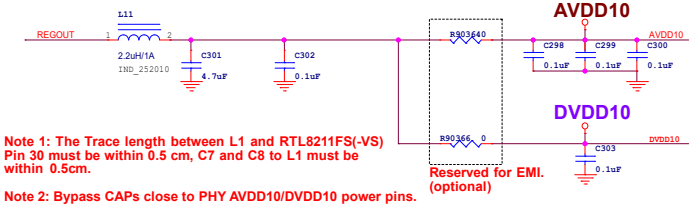


Pull-up for additional 2ns delay to RXC for data latching.

RSET



Switching Regulator

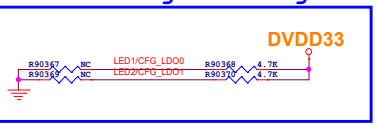


Note 1: The Trace length between L1 and RTL8211FS(-VS) Pin 30 must be within 0.5 cm, C7 and C8 to L1 must be within 0.5cm.

Note 2: Bypass CAPs close to PHY AVDD10/DVDD10 power pins.

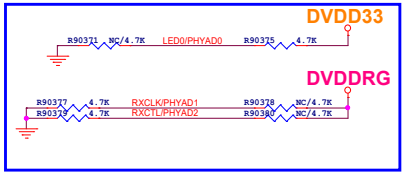
Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

RGMII Voltage Config.



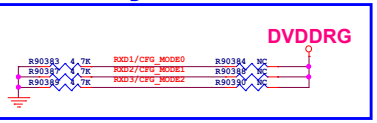
RGMII Power Source	CFG_LDO[1:0]
External 3.3V (default)	2'b00
Internal 2.5V	2'b01
Internal 1.8V	2'b10
Internal 1.5V	2'b11

PHY Address Config.



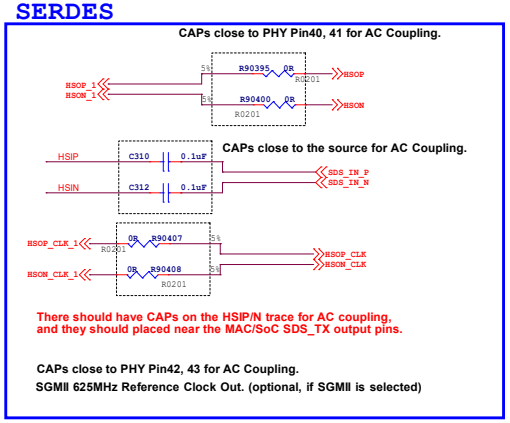
PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

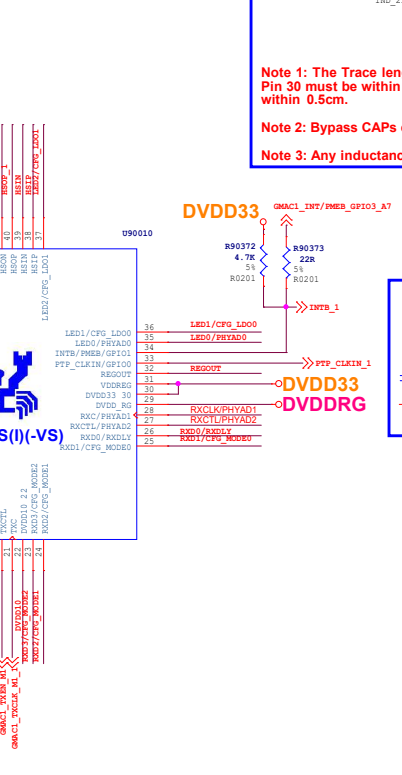
PHY Config.



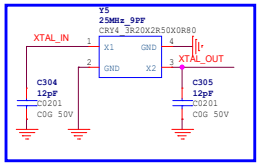
Operating Mode	CFG_MODE[2:0]
UTP <=> RGMII (default)	3'b000
FIBER <=> RGMII	3'b001
UTP/FIBER <=> RGMII	3'b010
UTP <=> SGMII	3'b011
SGMII (PHY) <=> RGMII	3'b100
SGMII (MAC) <=> RGMII	3'b101
UTP <=> FIBER (AUTO)	3'b110
UTP <=> FIBER (FORCE)	3'b111

SERDES

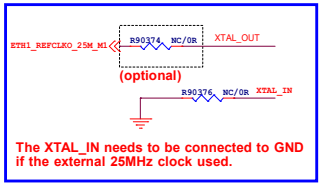




Crystal Case

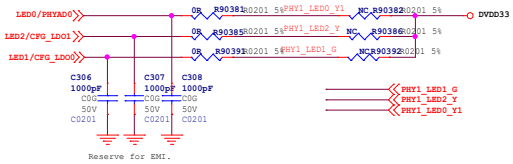


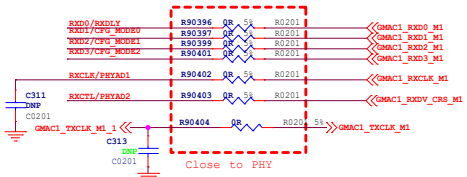
External clock Case

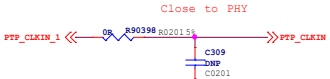


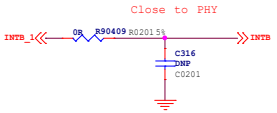
The XTAL_IN needs to be connected to GND if the external 25MHz clock used.

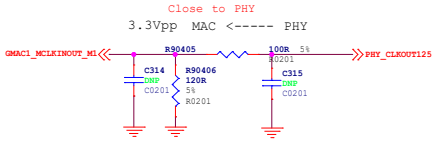
LEDs Configuration

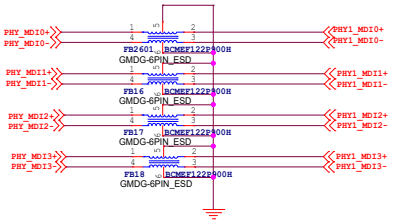












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Size	Title:	REV
C	Rock 3 Compute Module Plus	V1.1
	Page Name: Ethernet	
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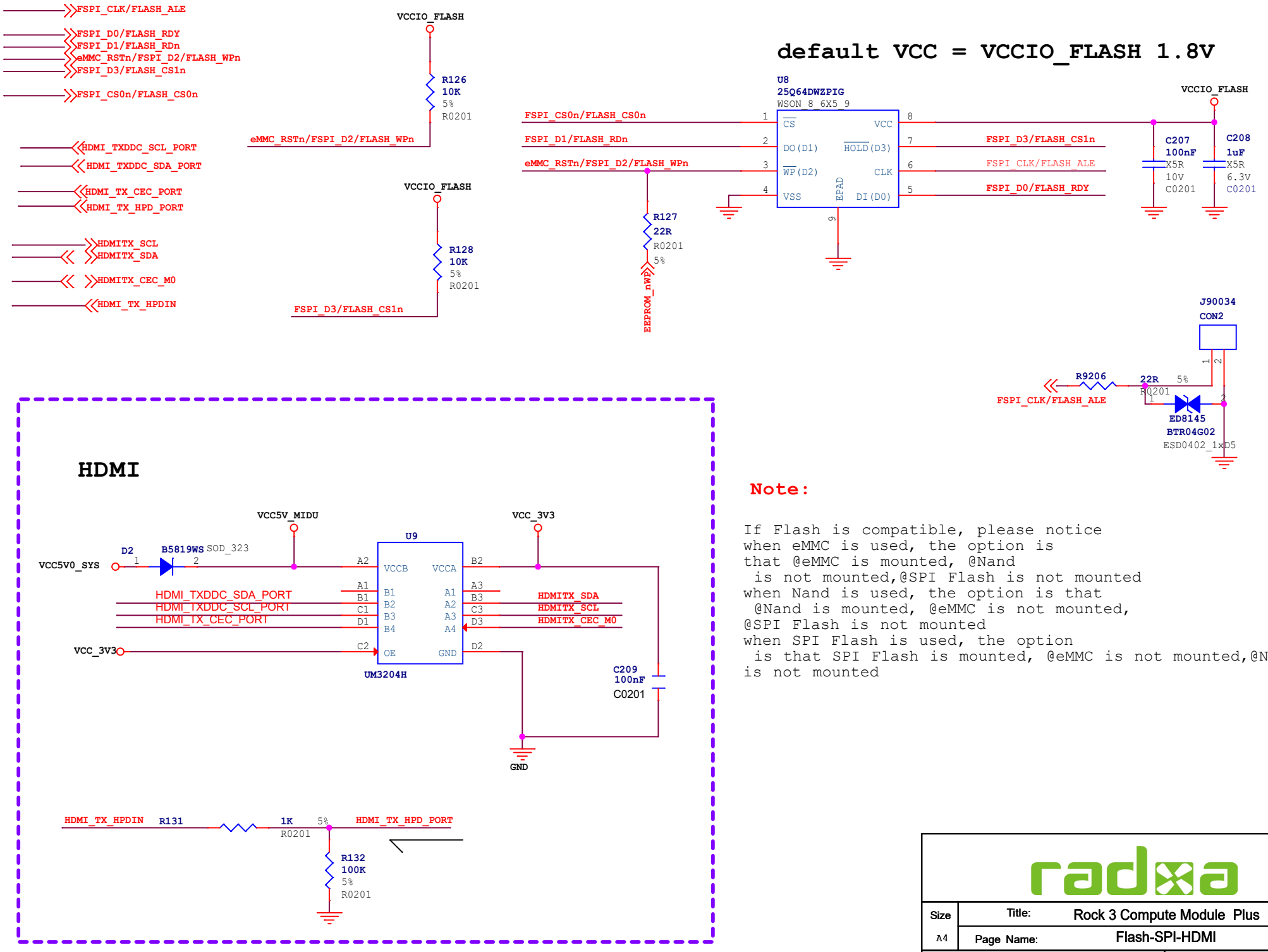
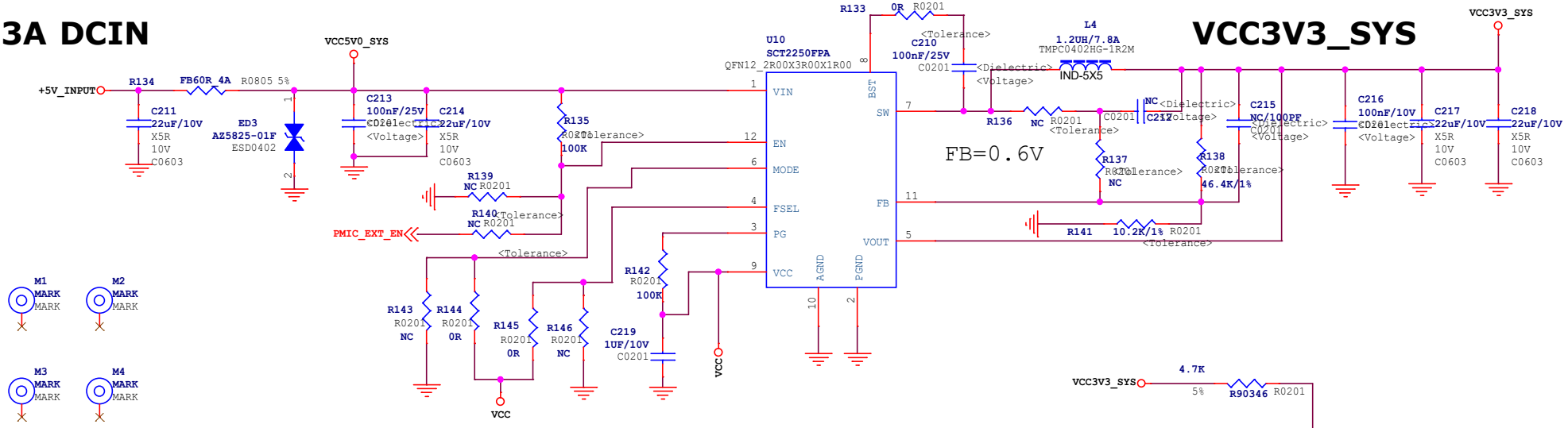


Note:

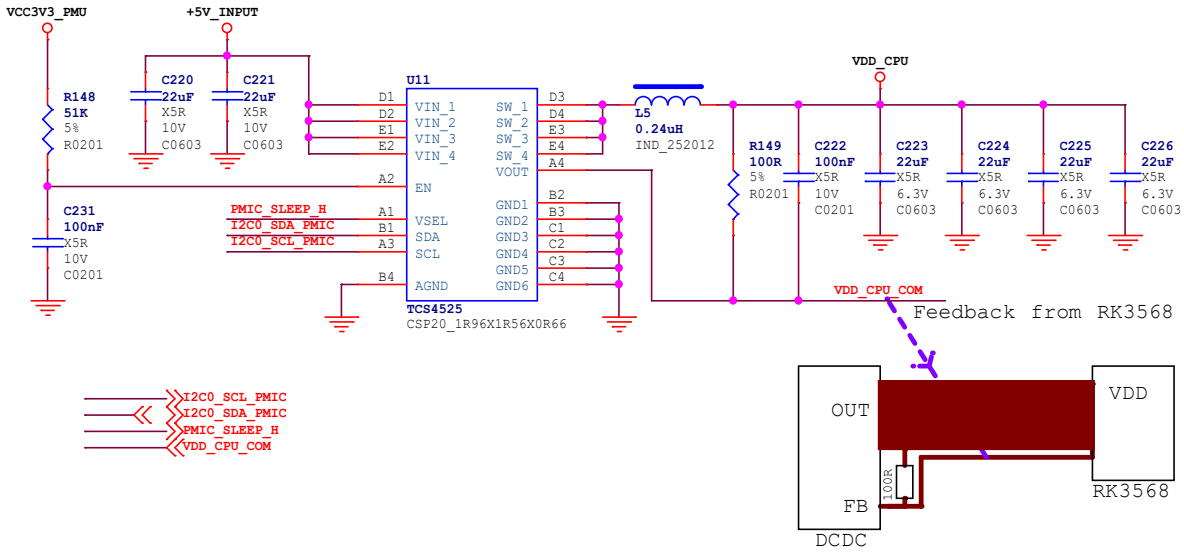
If Flash is compatible, please notice
when eMMC is used, the option is
that @eMMC is mounted, @Nand
is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that
@Nand is mounted, @eMMC is not mounted,
@SPI Flash is not mounted
when SPI Flash is used, the option
is that SPI Flash is mounted, @eMMC is not mounted,@Nand
is not mounted

Size: A4	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: Flash-SPI-HDMI	
Date: Friday, January 06, 2023	Sheet 19 of 25	

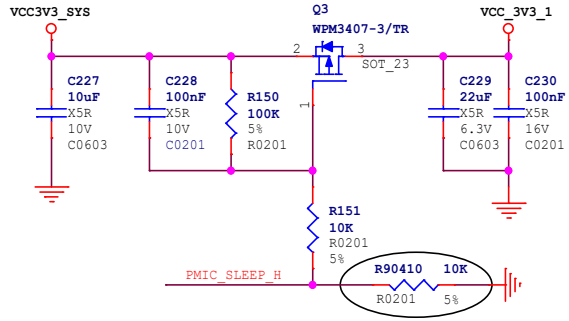
5V/3A DCIN



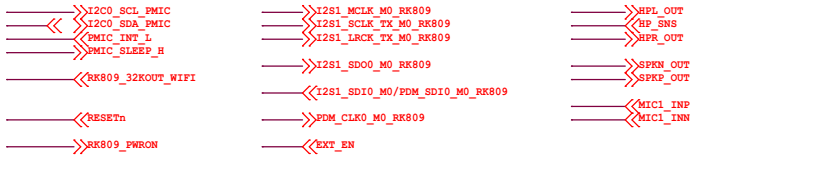
VDD_CPU

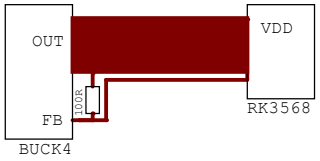


VCC_3V3 (Power OFF under SLEEP)

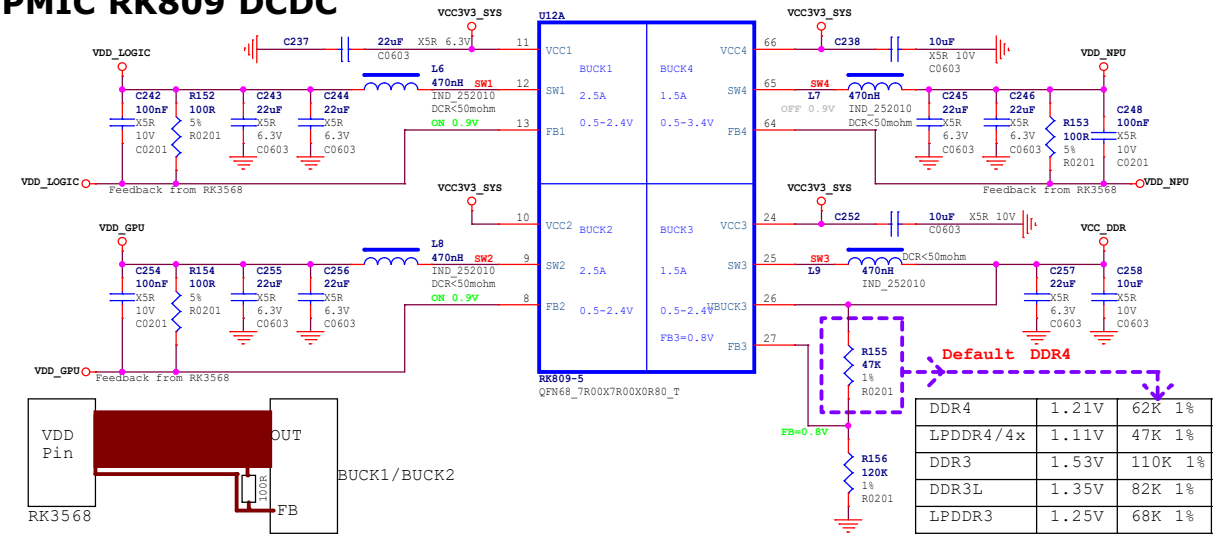


Size	Title: Rock 3 Compute Module Plus		REV
Custom	Page Name: Power_DC IN		V1.1
Date: Friday, January 06, 2023		Sheet 20 of 25	





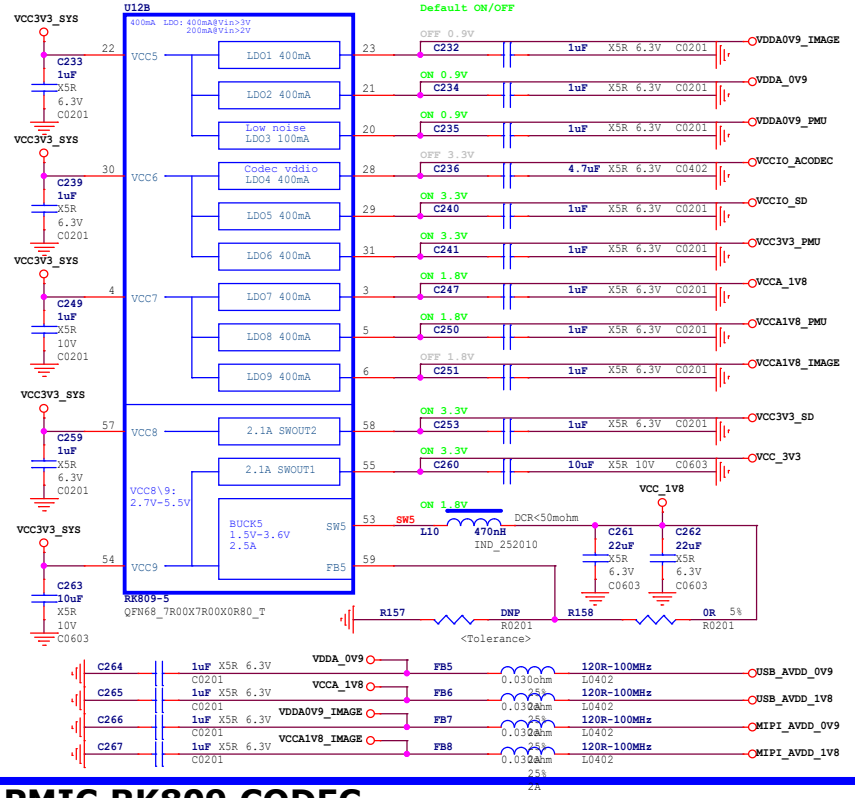
PMIC RK809 DCDC



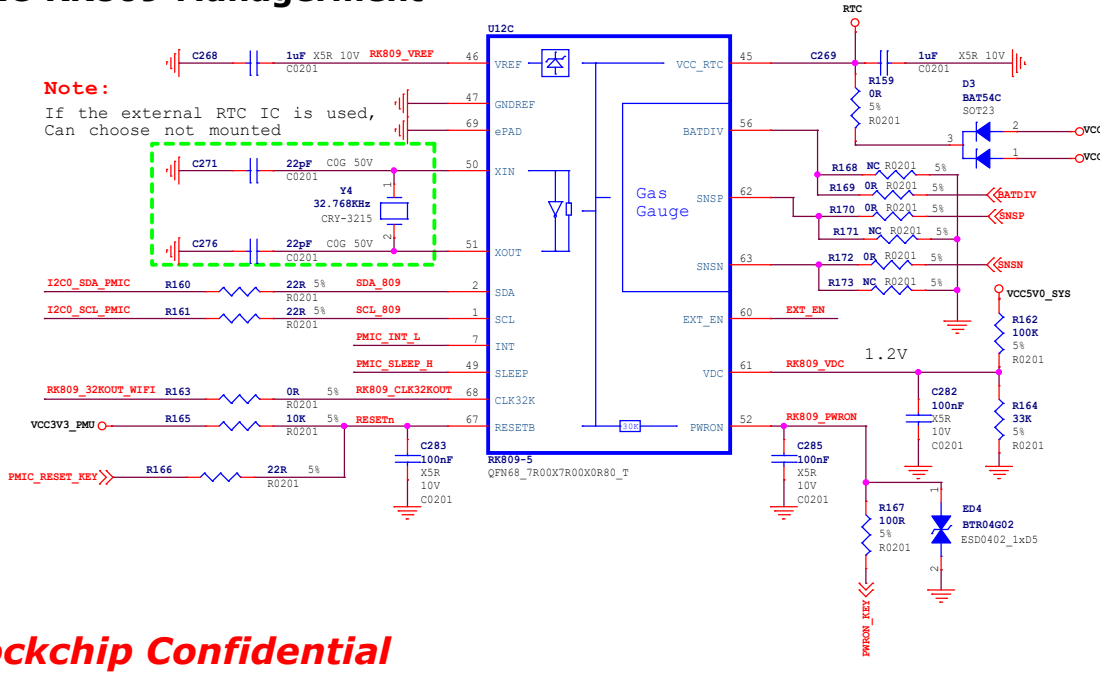
Default DDR4

DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

PMIC RK809 LDO

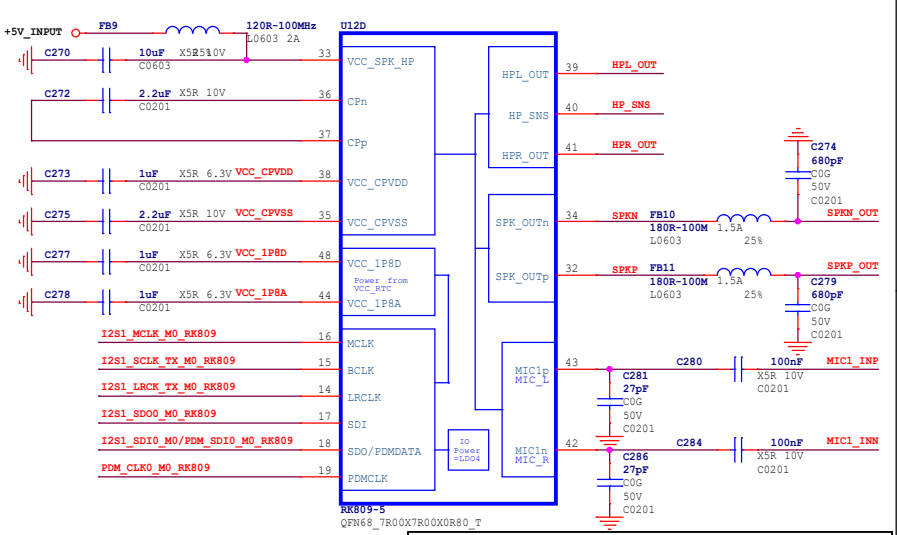


PMIC RK809 Management



Note:
If the external RTC IC is used,
Can choose not mounted

PMIC RK809 CODEC



Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

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Size: A3	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: Power_PMIC	
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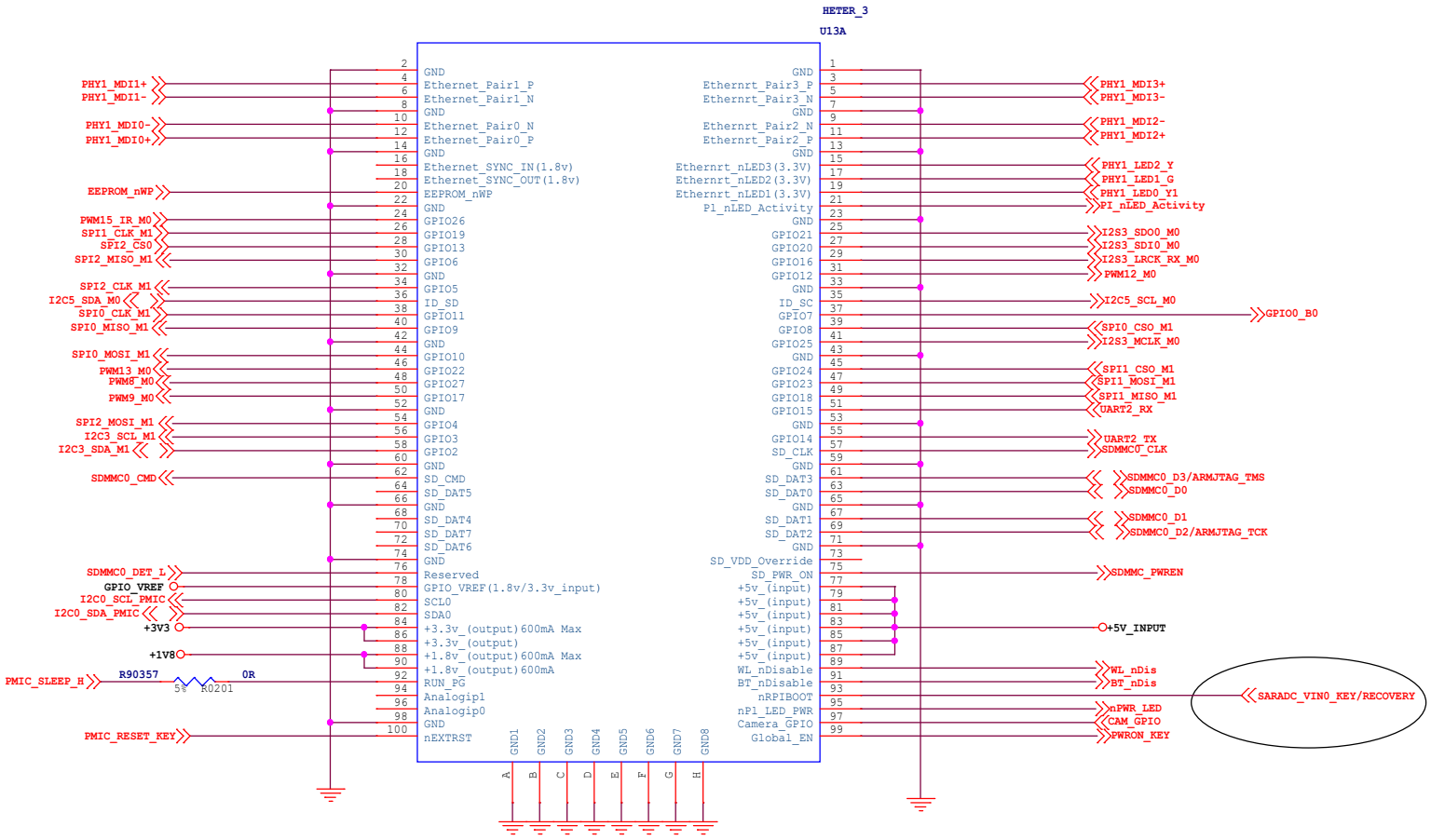
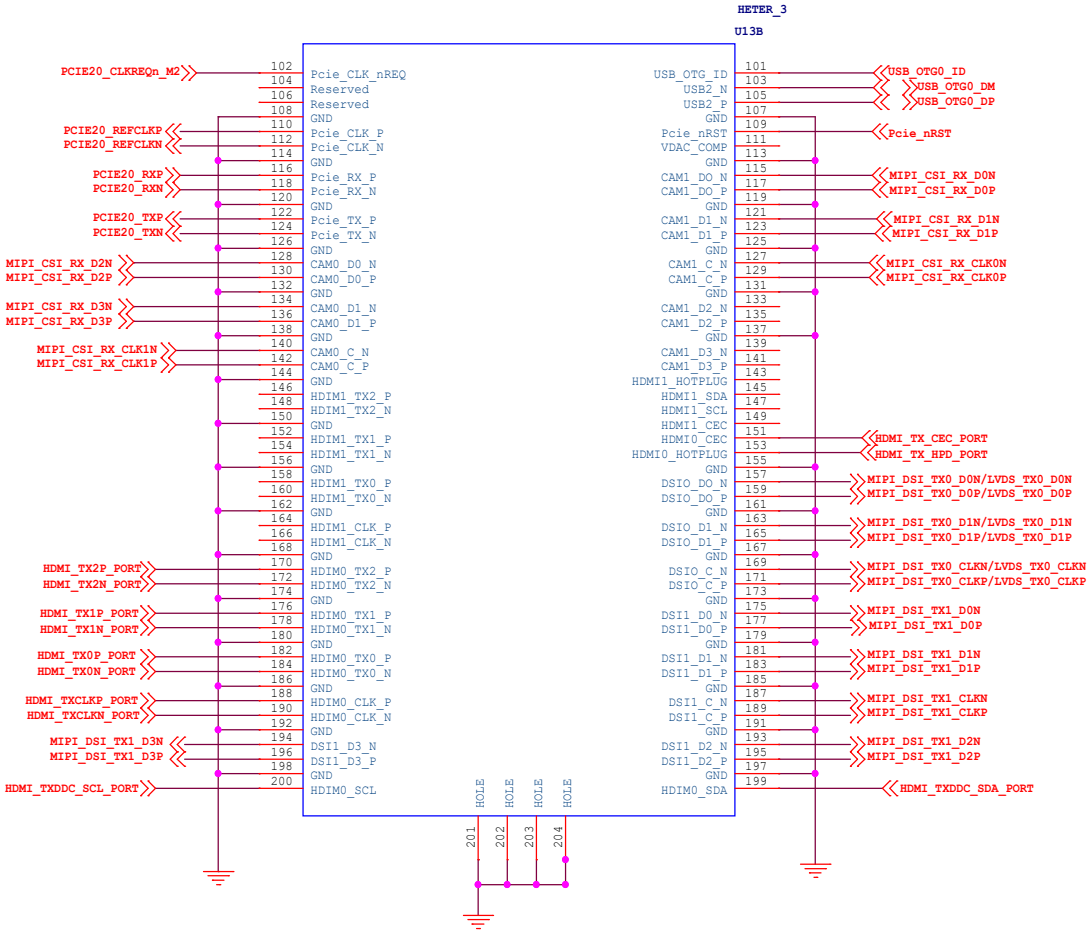
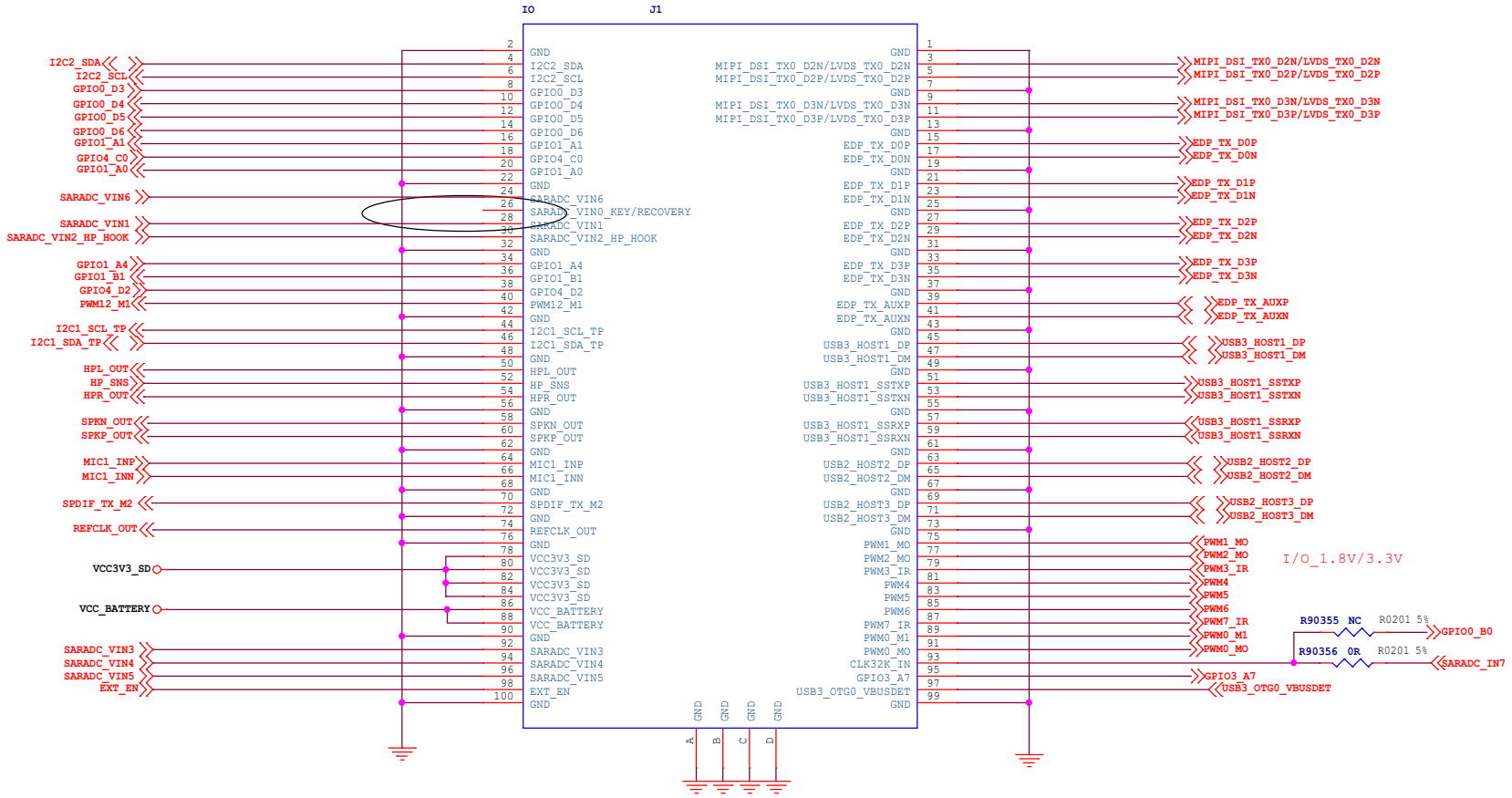


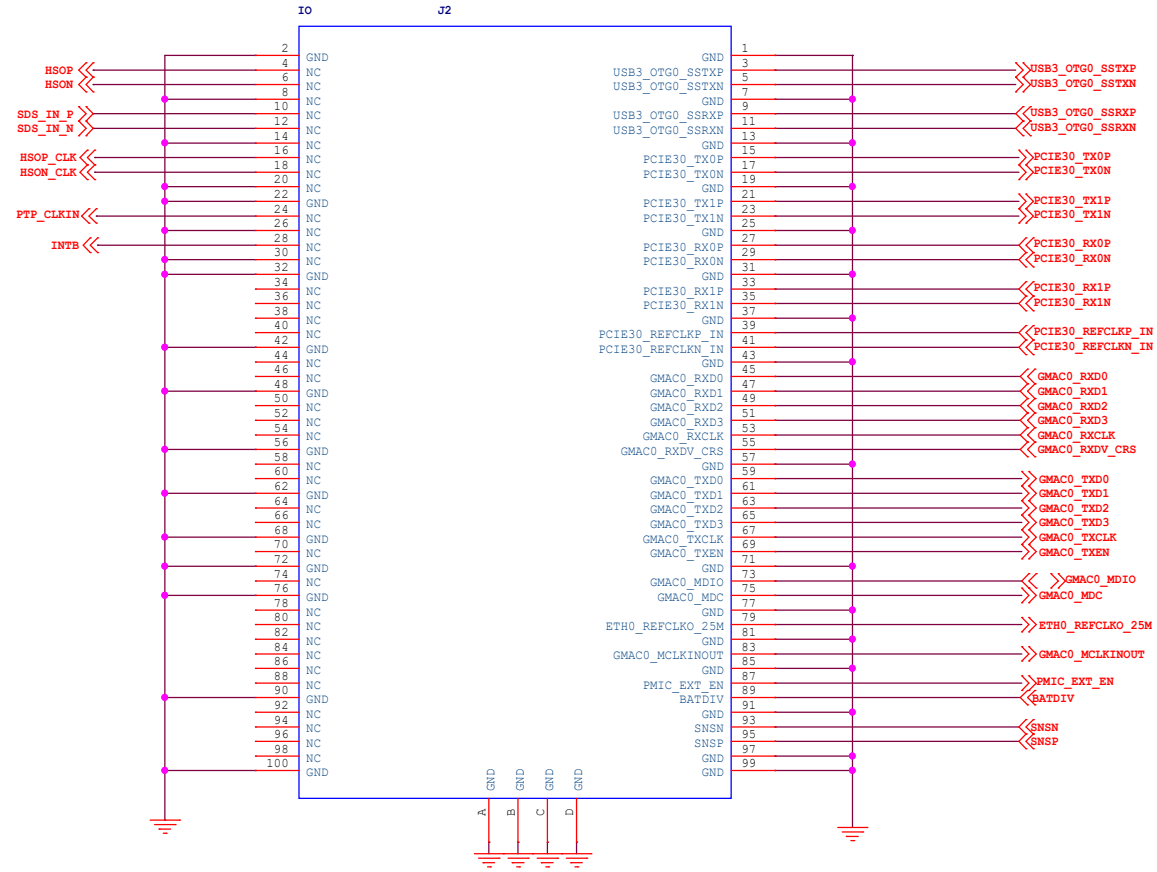
Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: GPIO+VCC_Connector	
Date: Friday, January 06, 2023	Sheet 22 of 25	



Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: High Speed Serial_Connector	
Date: Friday, January 06, 2023	Sheet 23 of 25	



Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: IO_Connector	
Date: Friday, January 06, 2023	Sheet 24 of 25	



Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: IO2_Connector	
Date: Friday, January 06, 2023	Sheet 25 of 25	