

# Radxa CM5 Carrier Board Design Note

Revision 1.0 2024-03-05



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# 1 Revision Control Table

| Version | Date       | Changes from previous version |
|---------|------------|-------------------------------|
| 1.0     | 2023/03/05 | First version                 |

# 2 Introduction

This guide is intended to provide engineers and developers with guidance on how to design and build an Carrier Board for the Radxa CM5.

Notice that the carrier board reference design files are provided at Radxa Github. In addition, Radxa offers the Radxa CM5 IO board to help customers to quickly show a basic use of the SoM.

### 3 Design Advice

#### 3.1 Power Supply

Rockchip officially recommends a 4V power supply for the RK806 to ensure optimal efficiency and peak performance of the PMU. Utilizing a 5V power supply may result in reduced efficiency and potentially lead to DC-DC whistling issues.

If VCC\_SYSIN(U13B-106 Pin) provides 5V input, this pin can be No Connect; if VCC\_SYSIN provides less than 5V, this pin needs to provide 5v from the IO board to the Radxa CM5.

|  |                  |                                    |  |   |   |    |              |     |           |     |           |             |          |    |        |    |   |   |         |    |     |    |             | 10         | 2 |     |     |     |    |            |    |  |  |  |  |
|--|------------------|------------------------------------|--|---|---|----|--------------|-----|-----------|-----|-----------|-------------|----------|----|--------|----|---|---|---------|----|-----|----|-------------|------------|---|-----|-----|-----|----|------------|----|--|--|--|--|
|  |                  | PCIE20x1_2_CLKREQn_M0>> 102<br>104 |  |   |   |    |              |     |           |     |           |             |          |    |        |    | 4 | F | ci      | e_ | CL  | K  | _nl         | RE         | Q |     |     |     |    |            |    |  |  |  |  |
|  |                  |                                    |  |   | Г |    | ~            | 202 | 10        | _   | ve        |             |          | Ē  | 295    | 61 | 6 |   |         | 0  | R   |    | $^{\wedge}$ | 10         | 6 | T   | (es | sei | ve | ea         |    |  |  |  |  |
|  |                  |                                    |  |   | L | V  | CC           | 5   | <u>vu</u> | _S  | Y-S       | 5 C         | <u>}</u> | Ē  | 20/    | 02 |   |   | <u></u> | ~~ |     |    |             | 10         | 8 | F   | Res | sei | ve | ed         |    |  |  |  |  |
|  |                  |                                    |  | - | - |    |              |     |           | -   |           |             |          | 1  | 7      |    |   |   |         |    | ſ   |    |             | 11         | 0 |     | ΒN  | D   |    |            |    |  |  |  |  |
|  |                  |                                    |  | P |   | 20 |              | 2   |           |     | E.        | (2)         |          |    |        |    |   |   |         |    |     |    |             | 11         | 2 | † F | Pci | e_  | CL | -K         | _P |  |  |  |  |
|  | PCIE20_0_REFCLKN |                                    |  |   |   |    |              |     |           |     |           | << <u>1</u> |          |    |        |    |   |   |         |    |     | 11 | 4           | Pcie_CLK_N |   |     |     |     |    |            |    |  |  |  |  |
|  |                  |                                    |  |   |   |    |              |     | ÷.,       | ÷., |           | _           |          | Č, |        |    |   |   |         |    | ौ   |    |             | 11         | 6 |     | ΒN  | D   |    |            |    |  |  |  |  |
|  |                  |                                    |  |   |   | PC |              | 20  | 20        | 느   | <b>XX</b> | Ρ.          |          | 2  | $\geq$ |    |   |   |         |    |     |    |             | 11         | 8 | † F | Pci | e_  | R> | <_F        | P  |  |  |  |  |
|  |                  |                                    |  |   |   |    | PCIEZU_U_RXN |     |           |     |           |             |          | >> |        |    |   |   |         |    |     |    |             | 12         | 0 | † F | ci  | e_  | R> | <u>(</u> ) | N  |  |  |  |  |
|  |                  |                                    |  |   |   |    |              |     |           |     |           |             |          |    |        |    |   |   |         |    | - 🛉 |    |             | 10         | 2 | - 0 | ΒN  | D   |    |            |    |  |  |  |  |

#### 3.2 HDMI

Regarding HDMI\_TX0\_HPD(U13B-153 Pin), this signal is connected directly to the HDMI connector without any processing due to the step-down processing on the Radxa CM5.



About the choice of HDMI signal line coupling capacitor: Since the Radxa CM5 has been connected in series with 220nF capacitor, if the IO board also needs to be connected in series, it is recommended to choose 220nF capacitor to ensure that the total capacitance is between 100 and 250nF.

#### 3.3 microSD Card

The SDMMC\_DET\_L(J1-74 Pin) needs to be pulled down by default if booting from microSD is required.

#### 3.4 GPIO

The GPIO has two types of 1.8V and 3.3V, which should be paid attention to when designing the circuit. You can see the schematic diagram of the Radxa CM5.

#### Note:

This RTC\_32K\_SOC(J1-90 Pin) GPIO port is already in use.



# 4 Support

For support please see the hardware documentation section of the Radxa Website and post questions to the Radxa forum.

For hardware related questions, please send email to hw@radxa.com. For software related questions, please send email to dev@radxa.com. For business and sales related questions, please send emails to sales@radxa.com.