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Radxa CM5

schematic

V2.21

Index

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Size	Title: CM5	REV
A4	Page Name: 02_INDEX	V2.2
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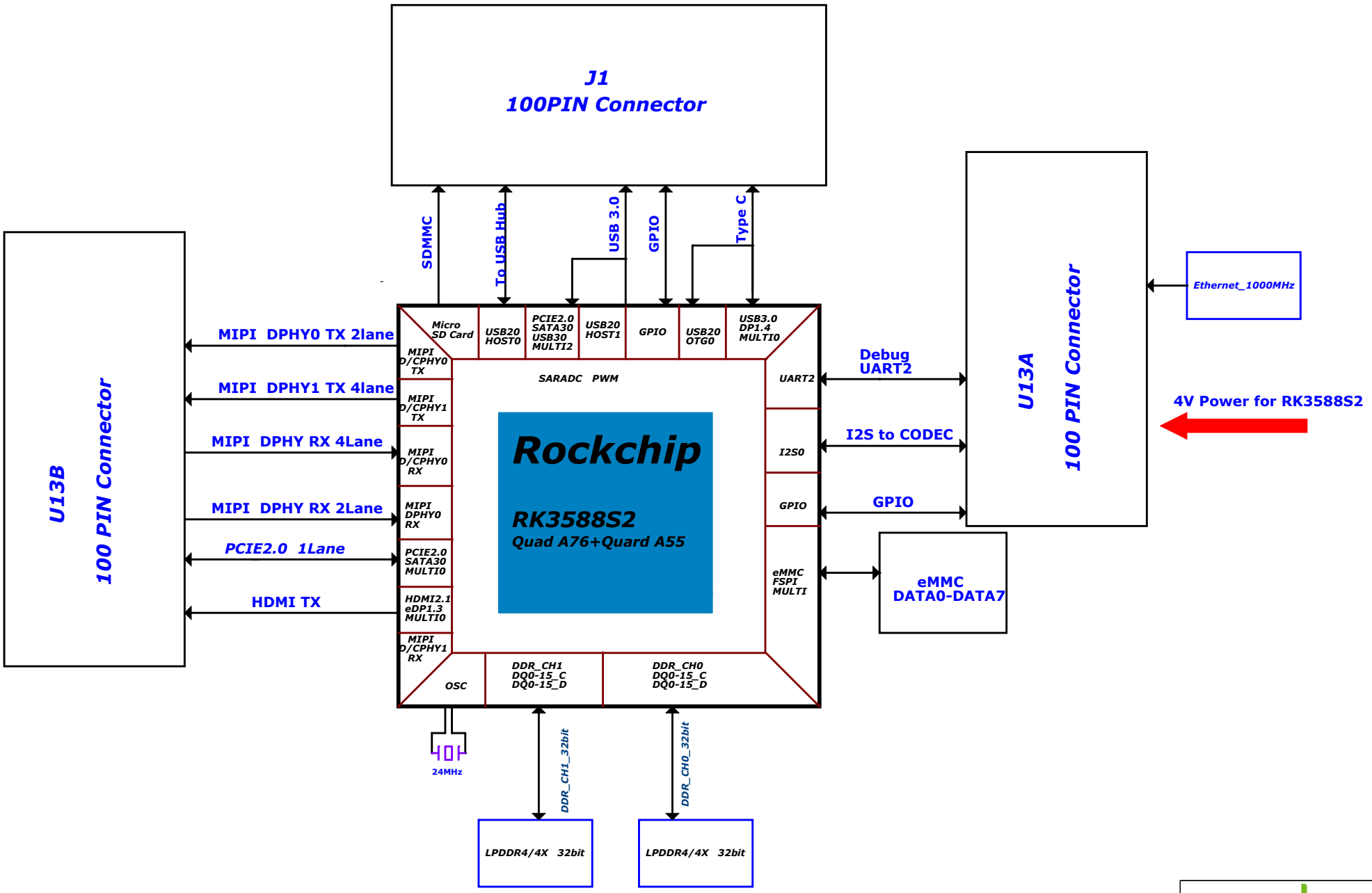
CM5 Block Diagram



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Size: A2	Title: CM5 Page Name: 03_Block	REV: V2.2
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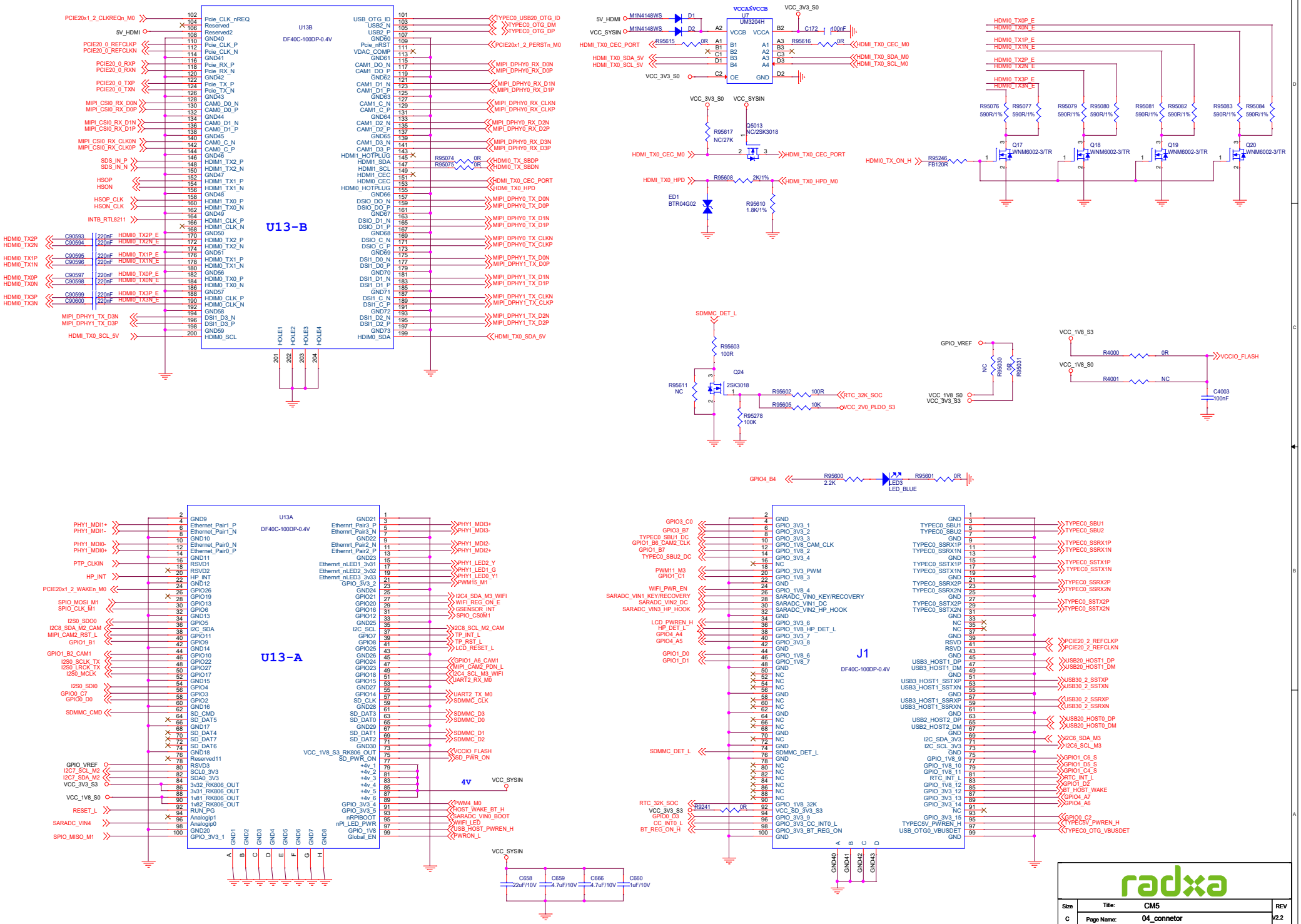
U13-B
U13B
DF40C-100DP-0.4V
U13-A
U13A
DF40C-100DP-0.4V
J1
DF40C-100DP-0.4V
U7
LM3204H
VCCA&VCCB
Q17
Q18
Q19
Q20
WNM6002-3/TR
Q24
2SK3018
Q5013
NC/2SK3018
ED1
BTR04G02
LED3
LED_BLUE
C658
22uF/10V
C659
4.7uF/10V
C666
4.7uF/10V
C660
1uF/10V
4V
VCC_SYSIN
VCC_3V3_S0
VCC_1V8_S0
VCC_1V8_S3
VCC_2V0_PLDO_S3
5V_HDMI
VCC_SYSIN
HDMI_TX0_CEC_PORT
HDMI_TX0_SDA_5V
HDMI_TX0_SCL_5V
HDMI_TX0_CEC_M0
HDMI_TX0_SDA_M0
HDMI_TX0_SCL_M0
HDMI_TX0_HPD
HDMI_TX0_HPD_M0
HDMI_TX_ON_H
HDMI_TX_SBDP
HDMI_TX_SBDN
HDMI_TX0_CEC_PORT
HDMI_TX0_HPD
MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_CLKP
MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D3N
MIPI_DPHY1_TX_D3P
SDMMC_DET_L
GPIO_VREF
RTC_32K_SOC
VCCIO_FLASH
GPIO4_B4
PCIE20x1_2_CLKREQn_M0
PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
PCIE20_0_RXP
PCIE20_0_RXN
PCIE20_0_TXP
PCIE20_0_TXN
MIPI_CSI0_RX_D0N
MIPI_CSI0_RX_D0P
MIPI_CSI0_RX_D1N
MIPI_CSI0_RX_D1P
MIPI_CSI0_RX_CLK0N
MIPI_CSI0_RX_CLK0P
SDS_IN_P
SDS_IN_N
HSOP
HSON
HSOP_CLK
HSON_CLK
INTB_RTL8211
HDMI0_TX2P
HDMI0_TX2N
HDMI0_TX1P
HDMI0_TX1N
HDMI0_TX0P
HDMI0_TX0N
HDMI0_TX3P
HDMI0_TX3N
HDMI0_SCL
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI0-
PHY1_MDI0+
PTP_CLKIN
HP_INT
PCIE20x1_2_WAKEn_M0
SPIO_MOSI_M1
SPIO_CLK_M1
I2S0_SDO0
I2C8_SDA_M2_CAM
MIPI_CAM2_RST_L
GPIO1_B1
GPIO1_B2_CAM1
I2S0_SCLK_TX
I2S0_LRCK_TX
I2S0_MCLK
I2S0_SDI0
GPIO0_C7
GPIO0_D0
SDMMC_CMD
GPIO_VREF
I2C7_SCL_M2
I2C7_SDA_M2
VCC_3V3_S3
VCC_1V8_S0
RESET_L
SARADC_VIN4
SPIO_MISO_M1
PHY1_MDI3+
PHY1_MDI3-
PHY1_MDI2-
PHY1_MDI2+
PHY1_LED2_Y
PHY1_LED1_G
PHY1_LED0_Y1
PWM15_M1
I2C4_SDA_M3_WIFI
WIFI_REG_ON_E
GSENSOR_INT
SPIO_CS0M1
I2C8_SCL_M2_CAM
TP_INT_L
TP_RST_L
LCD_RESET_L
GPIO1_A6_CAM1
MIPI_CAM2_PDN_L
I2C4_SCL_M3_WIFI
UART2_RX_M0
UART2_TX_M0
SDMMC_CLK
SDMMC_D3
SDMMC_D0
SDMMC_D1
SDMMC_D2
VCCIO_FLASH
SD_PWR_ON
PWM4_M0
HOST_WAKE_BT_H
SARADC_VIN0_BOOT
WIFI_LED
USB_HOST_PWREN_H
PWRON_L
GPIO3_C0
GPIO3_B7
TYPEC0_SBU1_DC
GPIO1_B6_CAM2_CLK
GPIO1_B7
TYPEC0_SBU2_DC
PWM11_M3
GPIO1_C1
WIFI_PWR_EN
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_DC
SARADC_VIN3_HP_HOOK
LCD_PWREN_H
HP_DET_L
GPIO4_A4
GPIO4_A5
GPIO1_D0
GPIO1_D1
SDMMC_DET_L
RTC_32K_SOC
VCC_3V3_S3
GPIO0_D3
CC_INT0_L
BT_REG_ON_H
TYPEC0_SBU1
TYPEC0_SBU2
TYPEC0_SSRX1P
TYPEC0_SSRX1N
TYPEC0_SSTX1P
TYPEC0_SSTX1N
TYPEC0_SSRX2P
TYPEC0_SSRX2N
TYPEC0_SSTX2P
TYPEC0_SSTX2N
PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
USB20_HOST1_DP
USB20_HOST1_DM
USB30_2_SSTXP
USB30_2_SSTXN
USB30_2_SSRXP
USB30_2_SSRXN
USB20_HOST0_DP
USB20_HOST0_DM
I2C6_SDA_M3
I2C6_SCL_M3
GPIO1_C6_S
GPIO1_D5_S
GPIO1_C4_S
RTC_INT_L
GPIO1_D2
BT_HOST_WAKE
GPIO4_A7
GPIO4_A6
GPIO0_C2
TYPEC5V_PWREN_H
TYPEC0_OTG_VBUSDET
USB_OTG0_VBUSDET
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C
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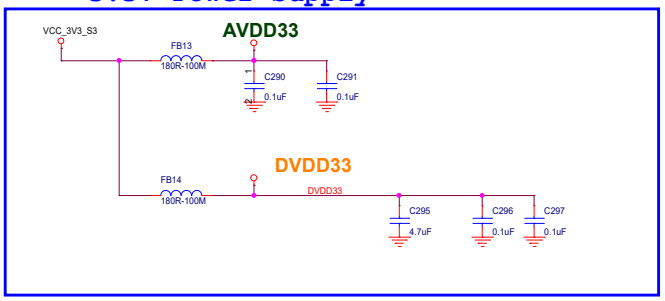
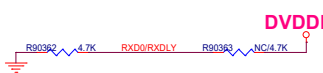
3.3V Power Supply



RGMII Power

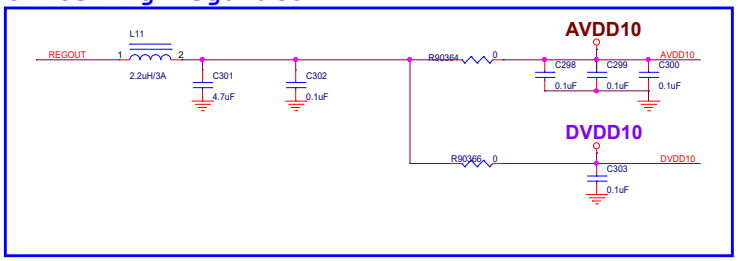
RGMII RXC Delay Config.



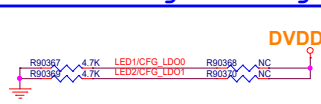
Pull-up for additional 2ns delay to RXC for data latching.

RSET

Switching Regulator

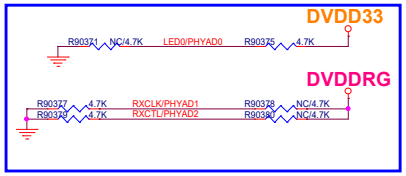


RGMII Voltage Config.



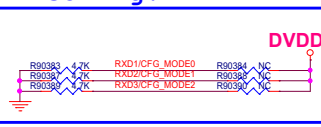
RGMII Power Source	CFG_LDO[1:0]
External 3.3V (default)	2'b00
Internal 2.5V	2'b01
Internal 1.8V	2'b10
Internal 1.5V	2'b11

PHY Address Config.



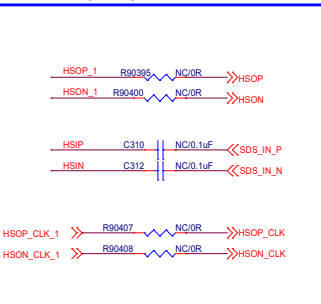
PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

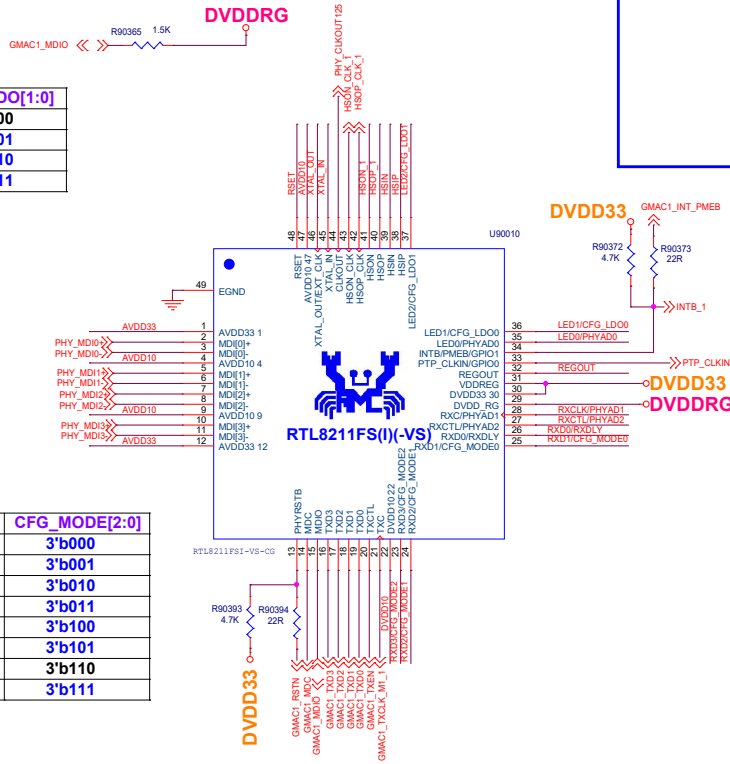
PHY Config.



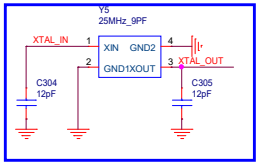
Operating Mode	CFG_MODE[2:0]
UTP <=> RGMII (default)	3'b000
FIBER <=> RGMII	3'b001
UTP/FIBER <=> RGMII	3'b010
UTP <=> SGMII	3'b011
SGMII (PHY) <=> RGMII	3'b100
SGMII (MAC) <=> RGMII	3'b101
UTP <=> FIBER (AUTO)	3'b110
UTP <=> FIBER (FORCE)	3'b111

SERDES (NC)

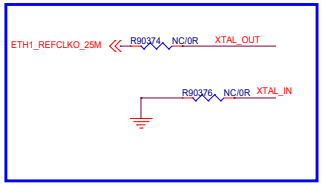




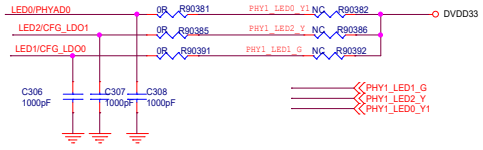
Crystal Case

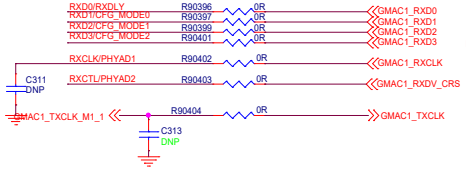


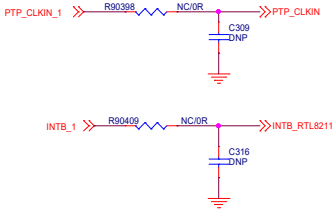
External clock Case

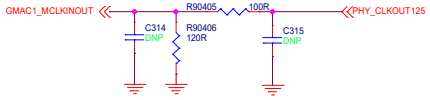


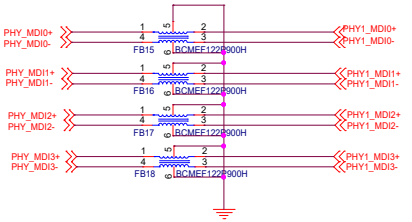
LEDs Configuration











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Size	Title:	CM5	REV
C	Page Name:	05_Ethernet_1000MHz	V2.2
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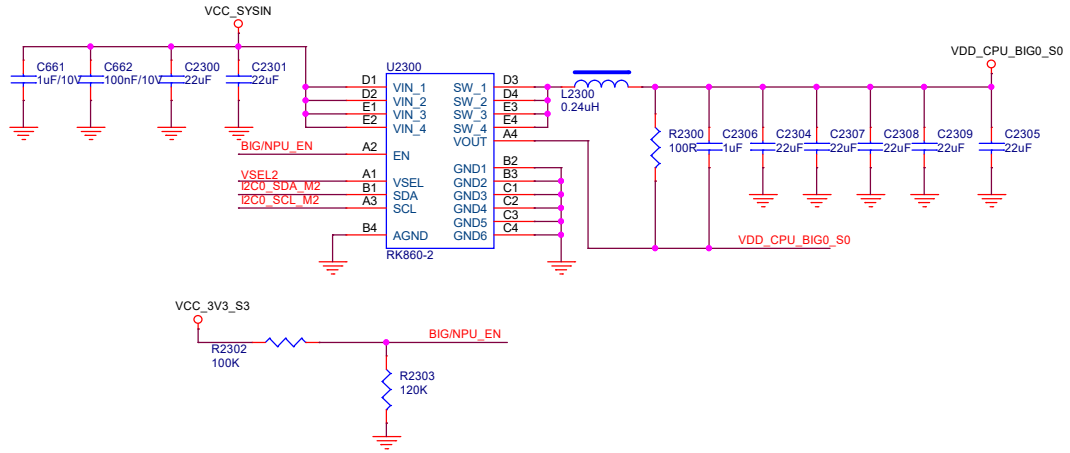
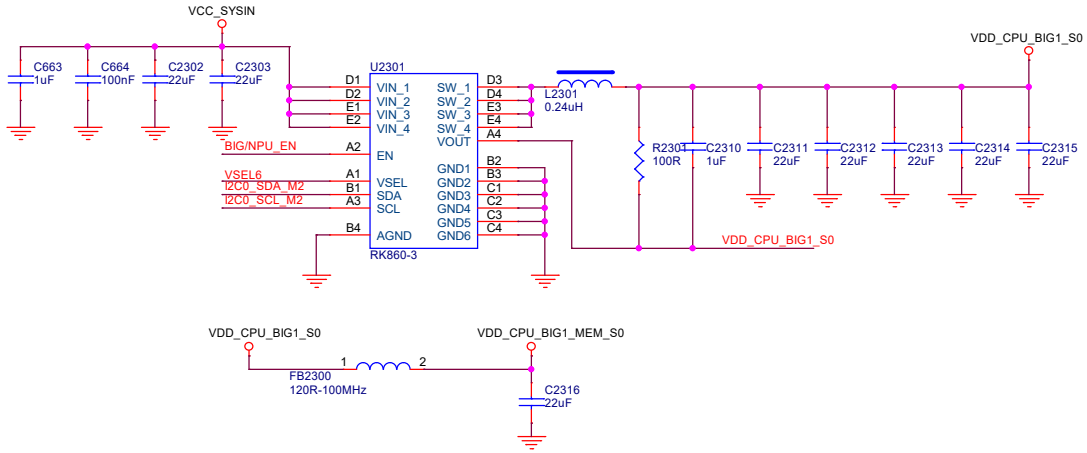
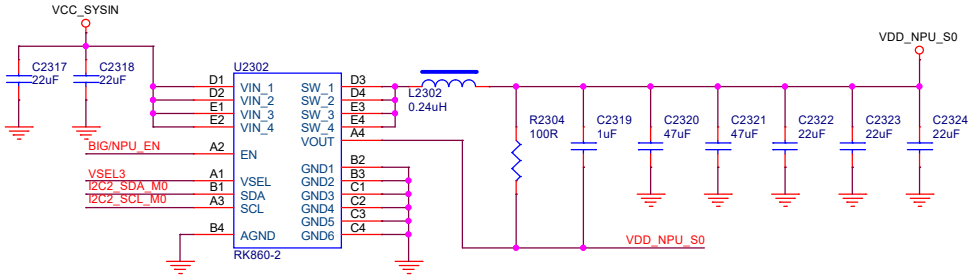
VDD_CPU_BIG0



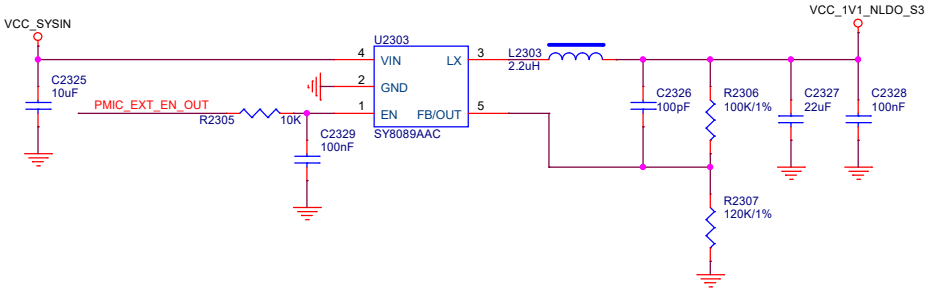
VDD_CPU_BIG1



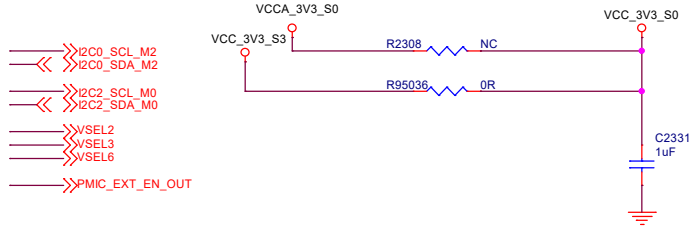
VDD_NPU



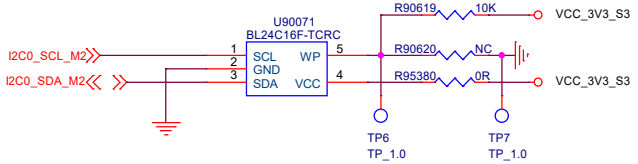
VCC_1V1_NLDO



VCC_3V3_S0



Mechine ID



Size: A3	Title: CM5	REV: V2.2
	Page Name: 06_Power_Ext Discrete	
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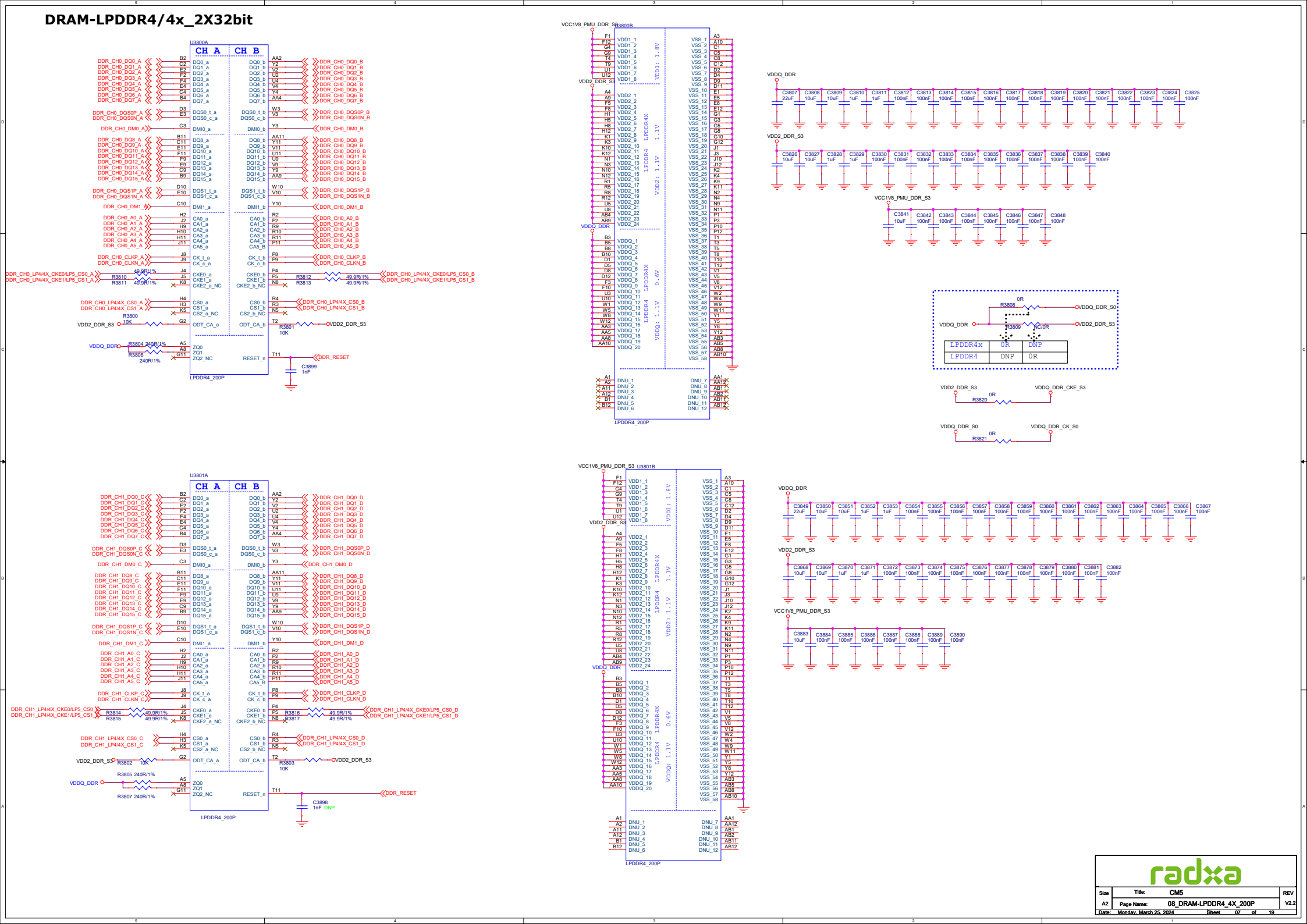
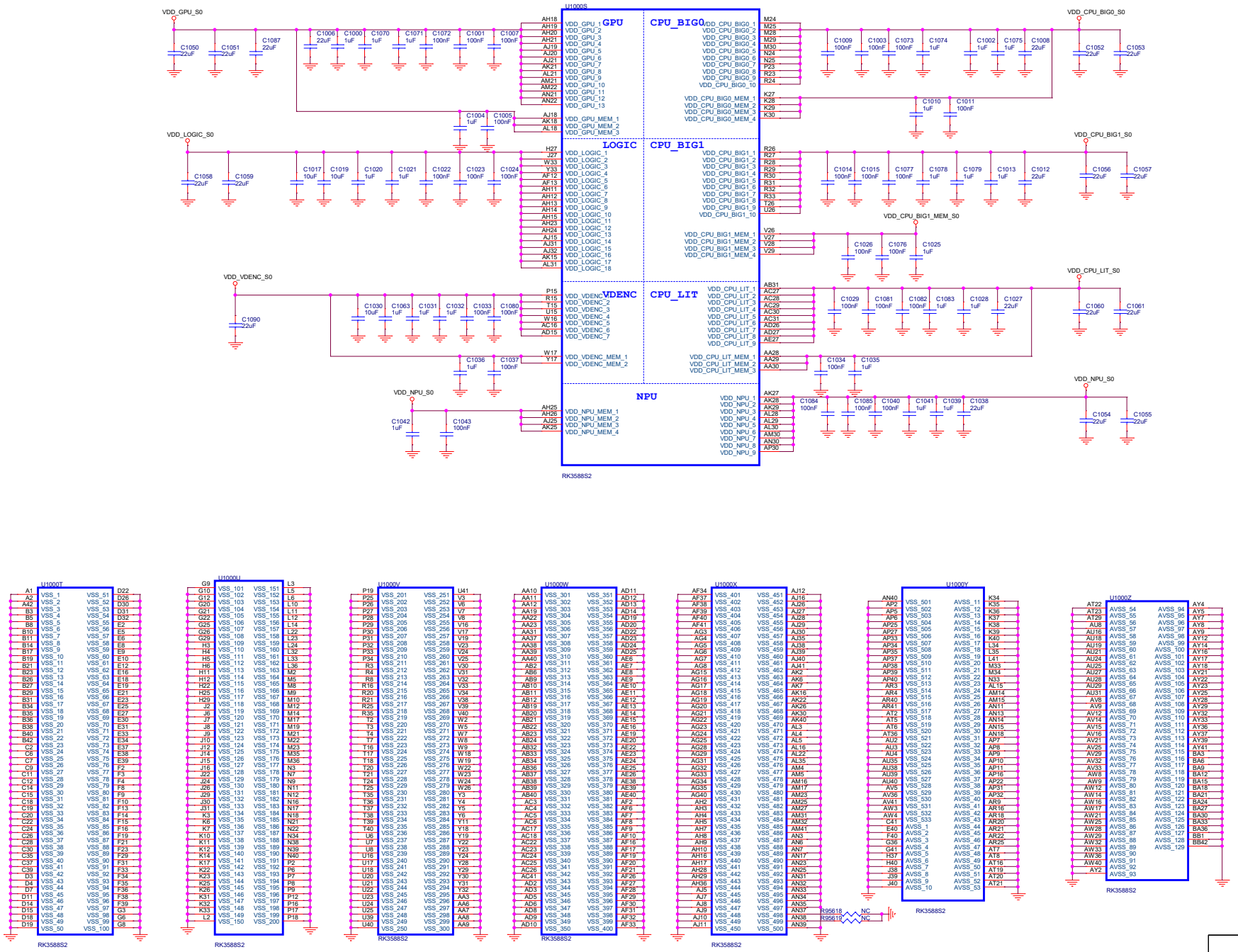
DRAM-LPDDR4/4x_2X32bit



RK3588S2 (Power&Gnd)



Size	Title: CM5		REV
A2	Page Name: 09_RK3588S_Power_GND		V2.2
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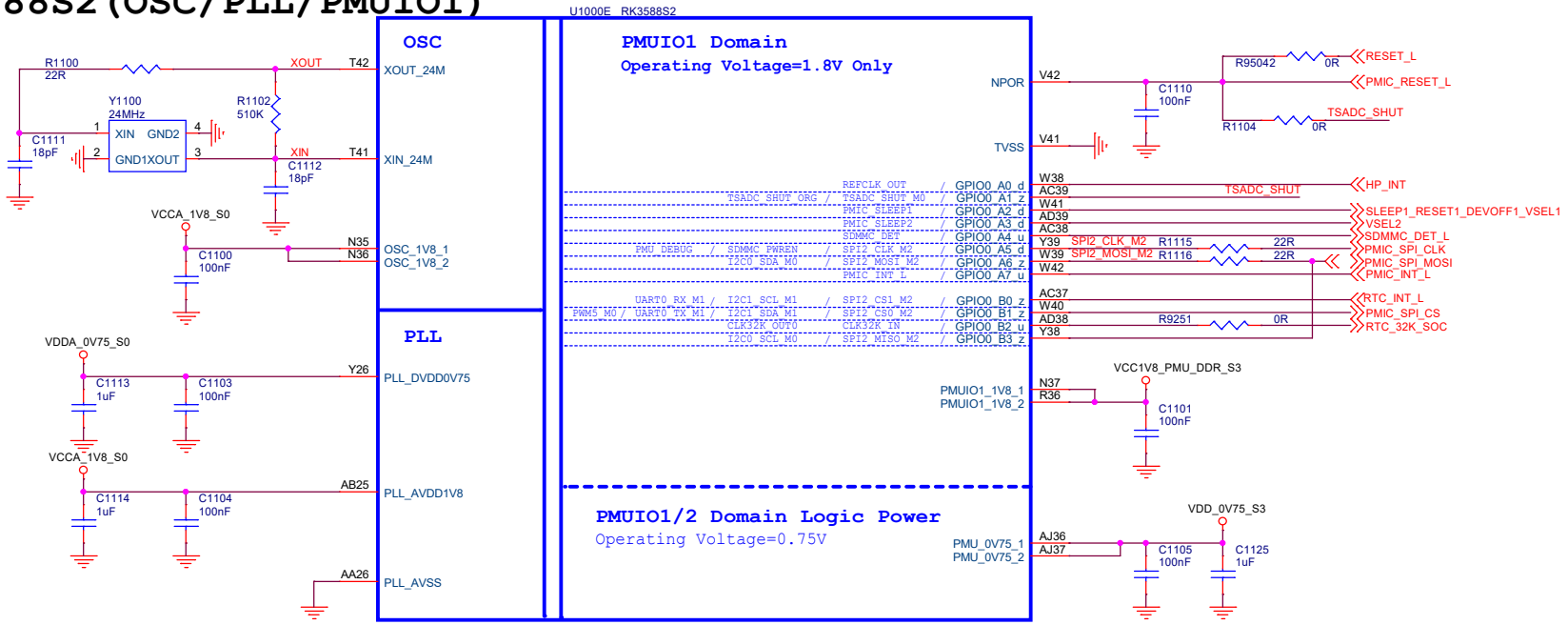
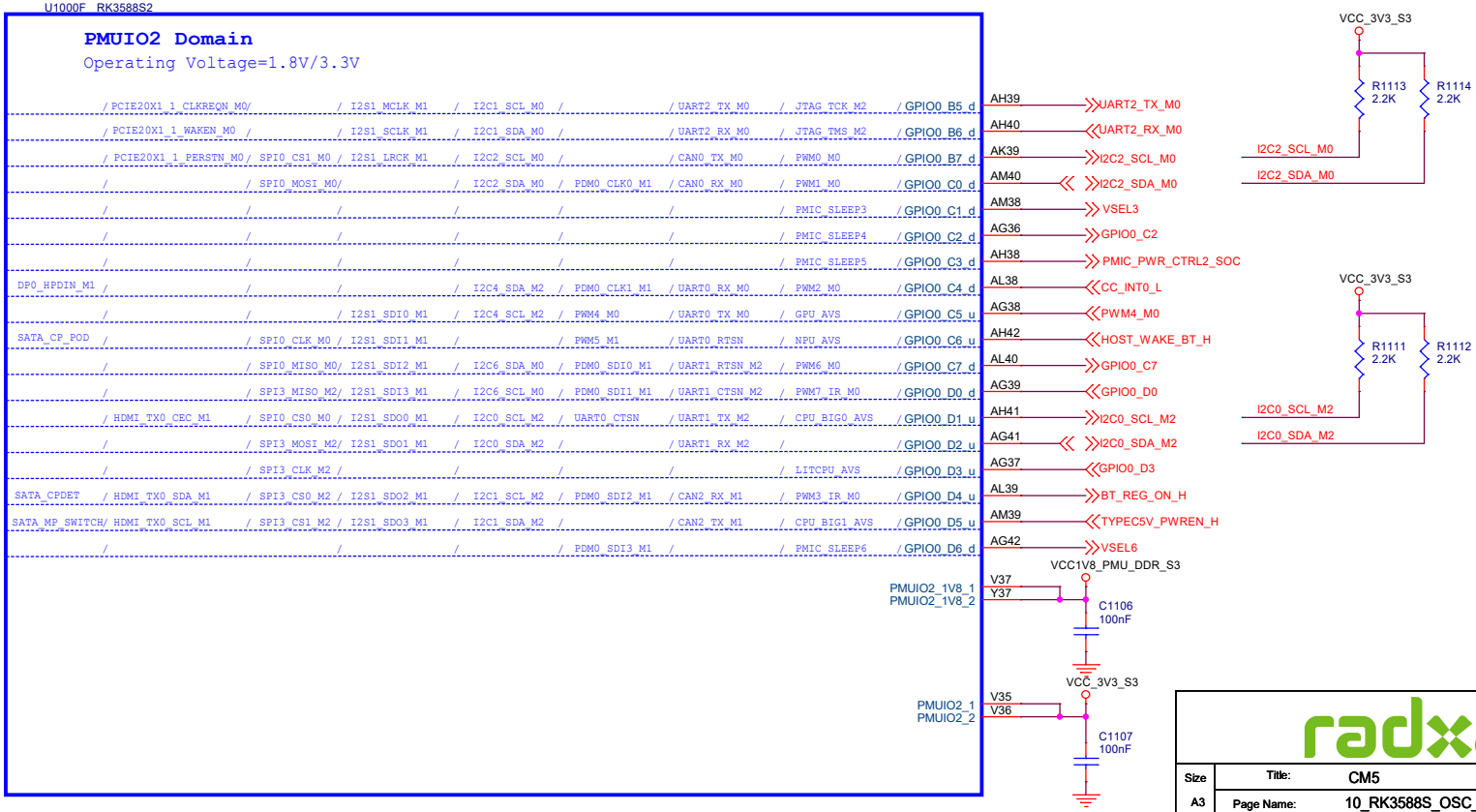
RK3588S2 (OSC/PLL/PMUIO1)



RK3588S2 (PMUIO2)



Size	Title: CM5		REV
A3	Page Name: 10_RK3588S_OSC_PLL_PMUIO		V2.2
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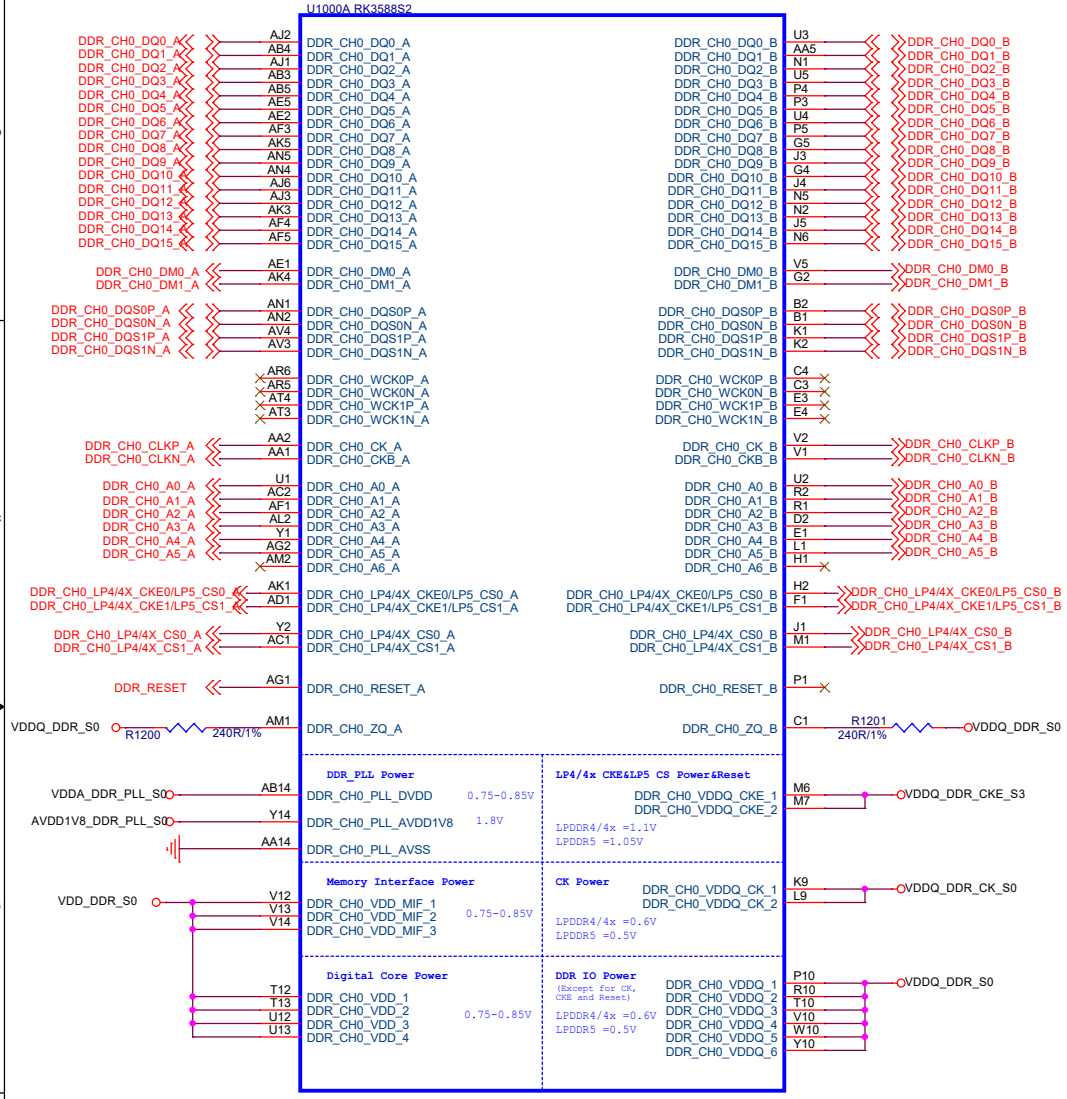
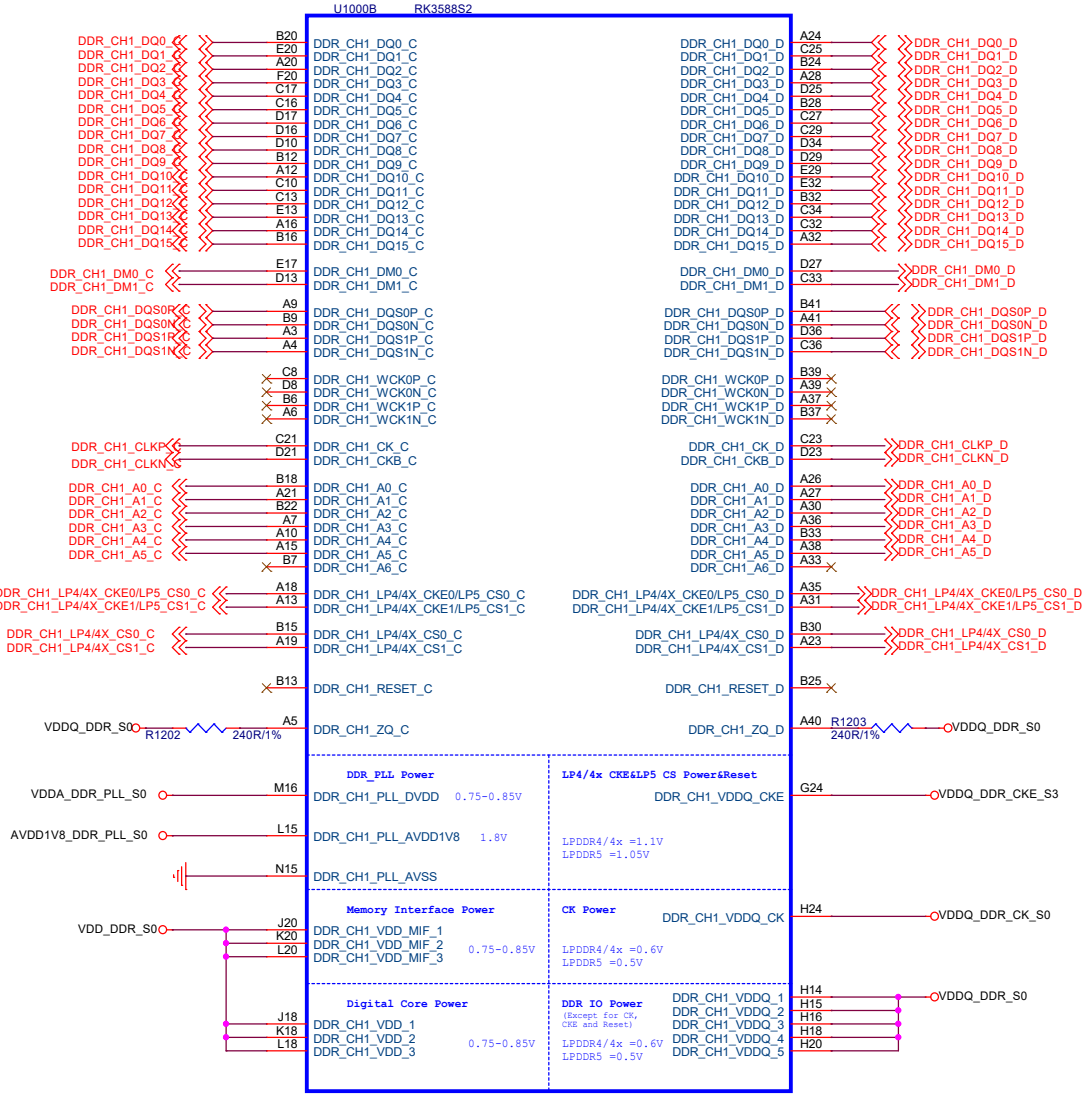
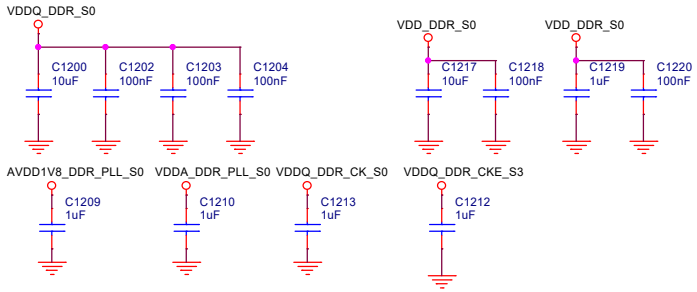
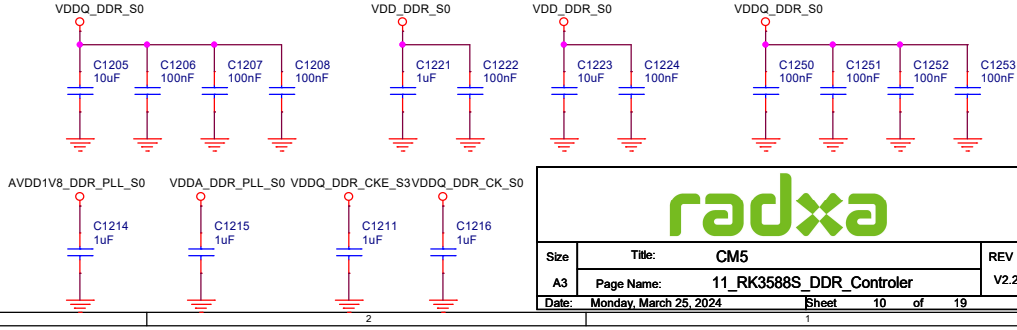
RK3588S2 (DDR PHY)





DDR FILTER





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Size	Title: CM5	REV
A3	Page Name: 11_RK3588S_DDR_Controler	V2.2
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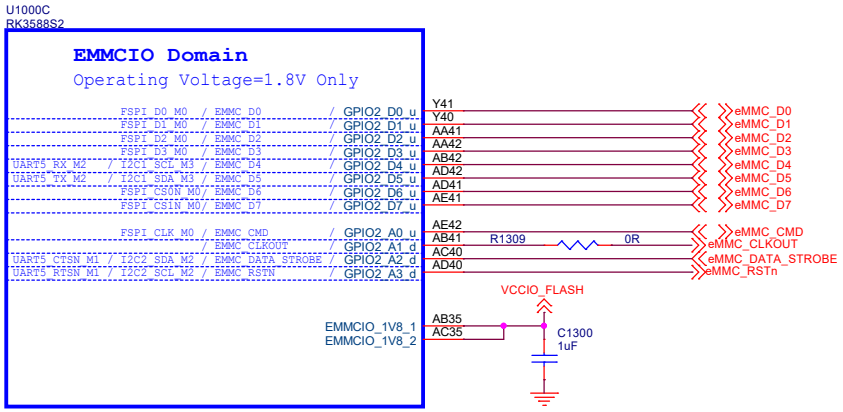
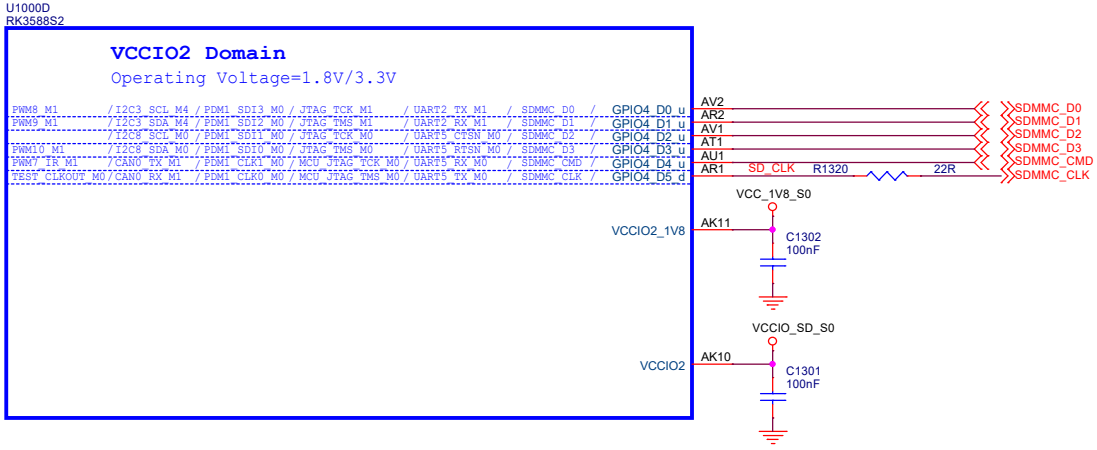
RK3588S2(EMMCIO Domain)



RK3588S2(VCCIO2 Domain)



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Size: A3	Title: CM5	REV: V2.2
	Page Name: 12_RK3588S_Flash_SD_Controller	
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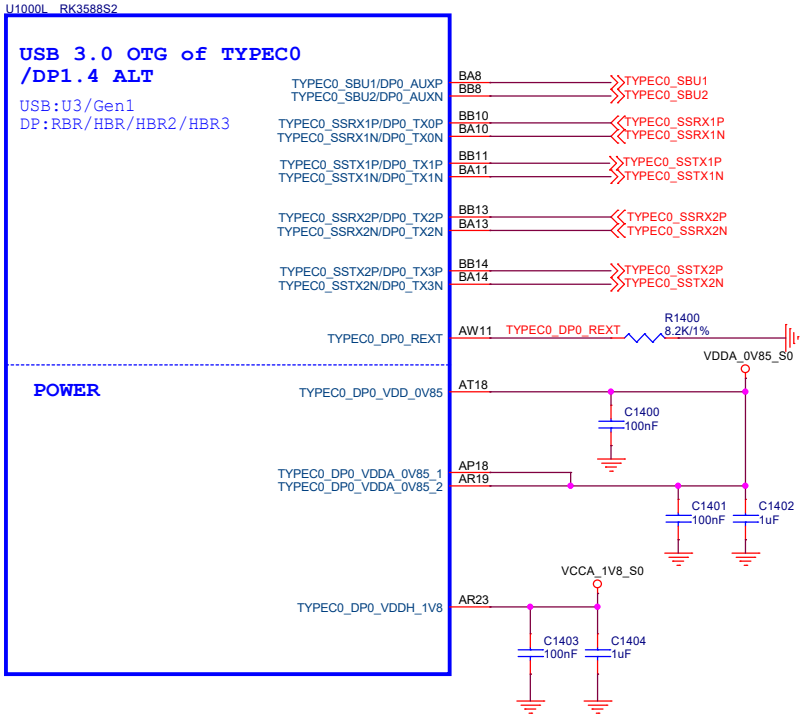
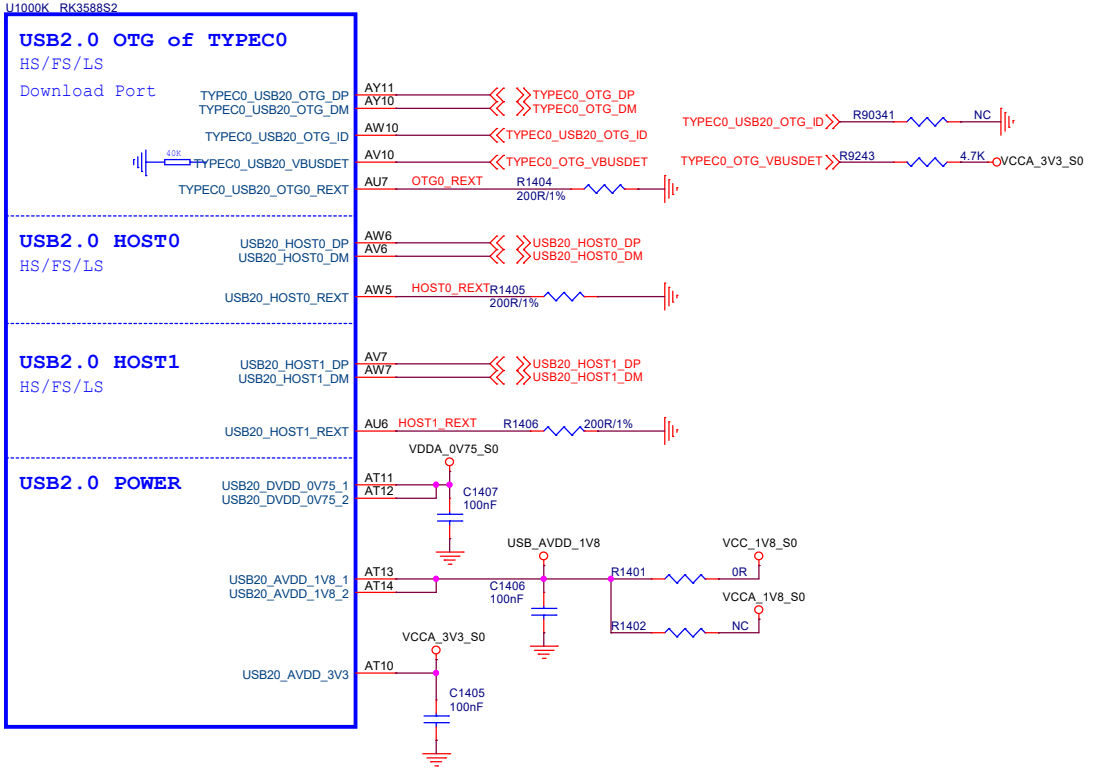
RK3588S2(USB3.0/DP1.4)



RK3588S2(USB2.0)



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A3	Page Name: 13_RK3588S_USB20_USB30_DP_PHY	V2.2
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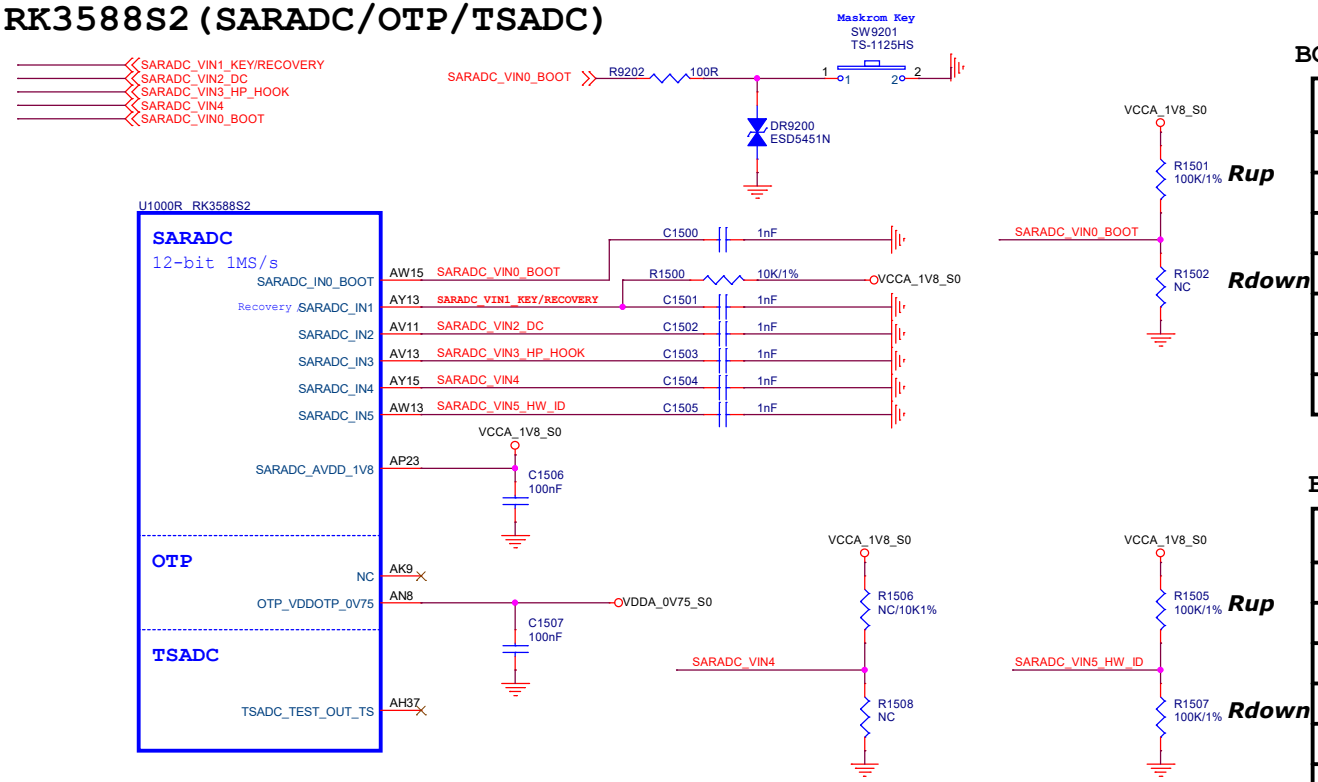
RK3588S2 (SARADC/OTP/TSADC)



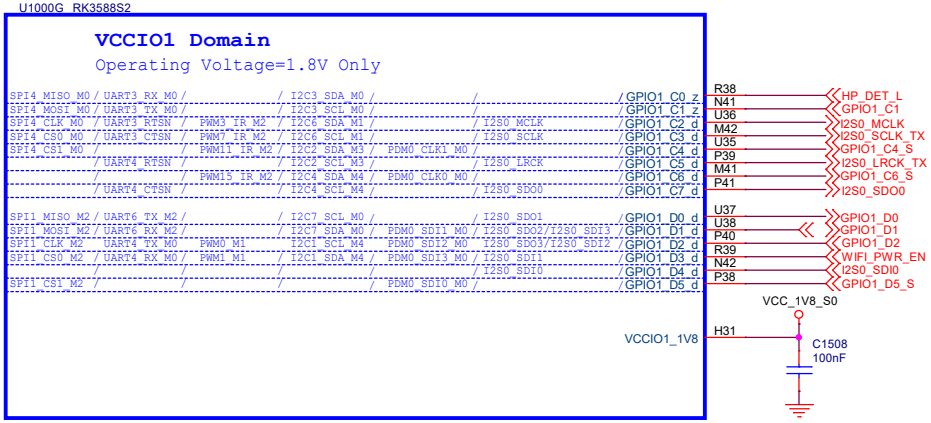
BOOT MODE CONFIG

Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	NC	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG

Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S2 (VCCIO1 Domain)



Size	Title: CM5		REV
A3	Page Name: 14_RK3588S_SARADC_1.8V_GPIO		V2.2
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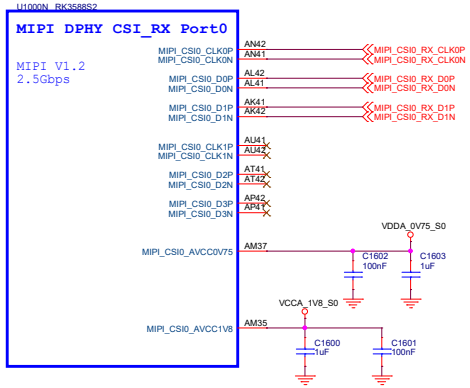
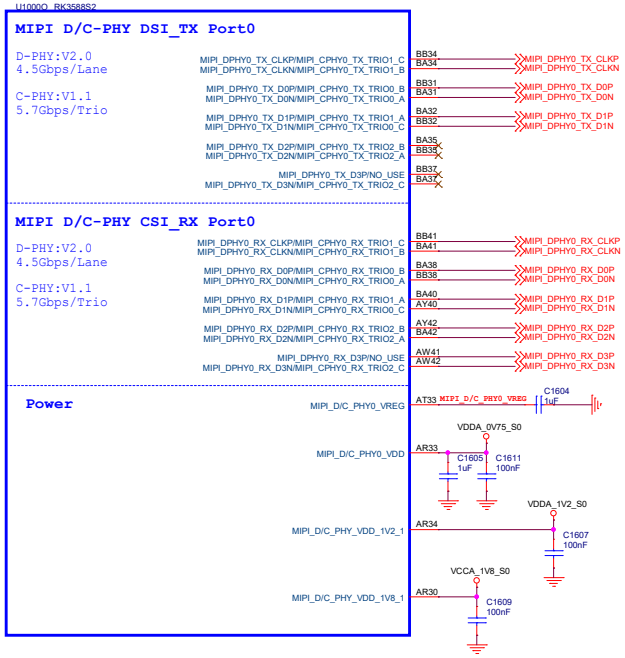
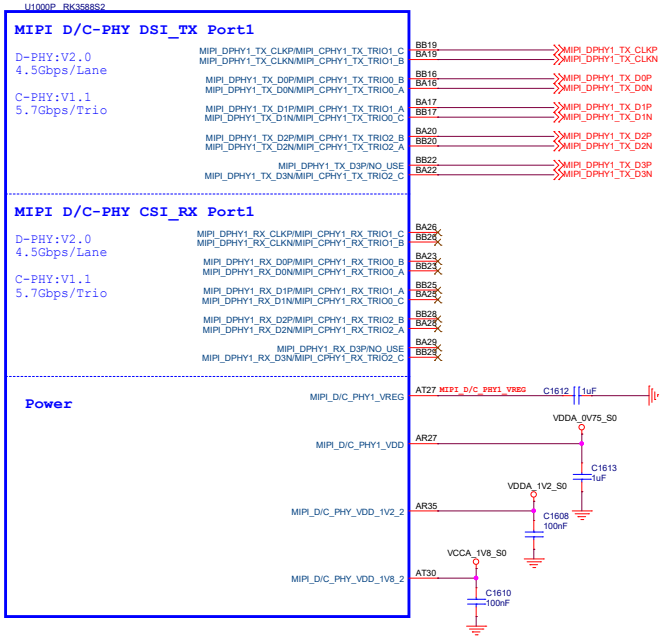
RK3588S2(MIPI_DPHY CSI0 RX)



RK3588S2(MIPI_D/C PHY0)

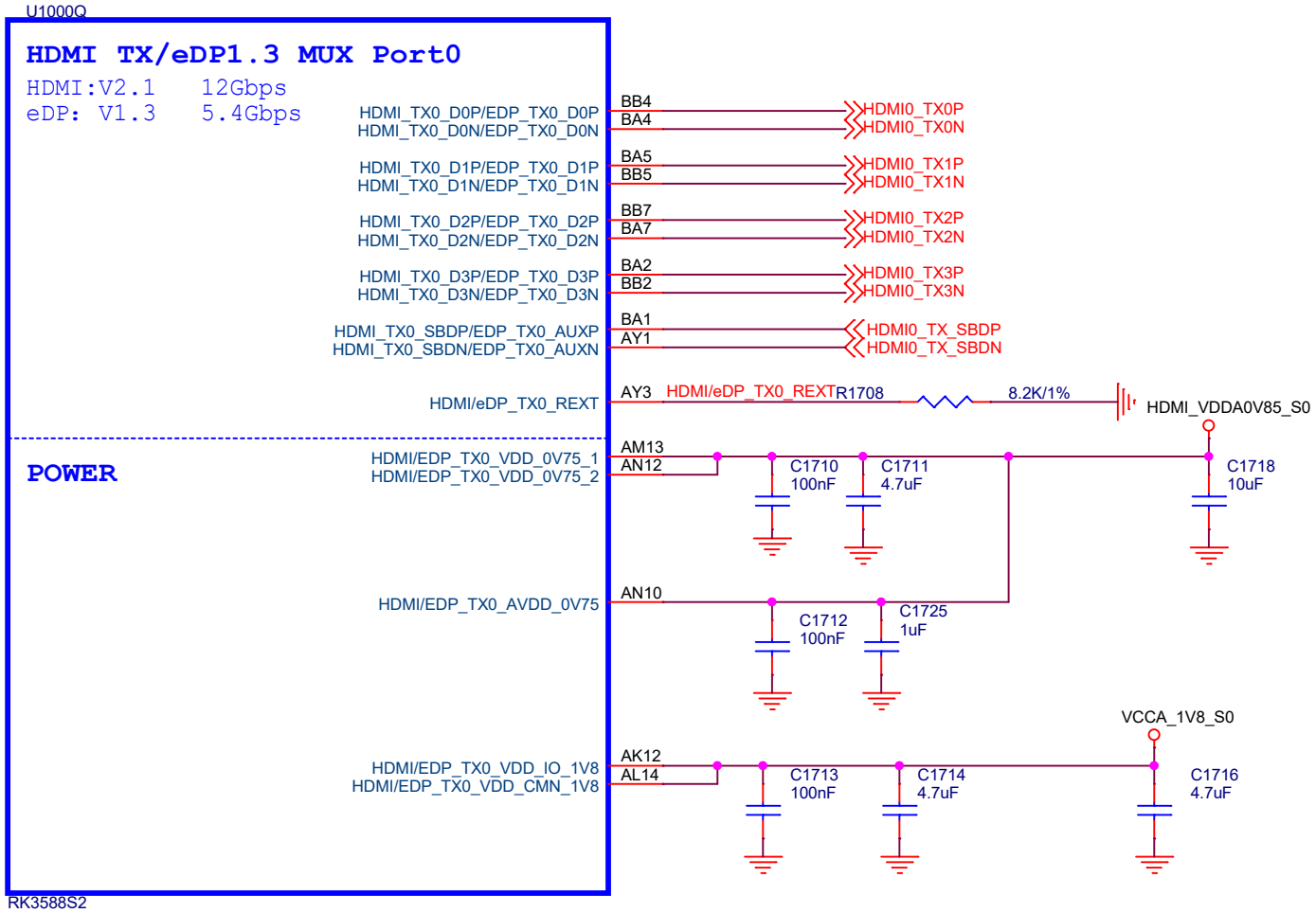


RK3588S2(MIPI_D/C PHY1)



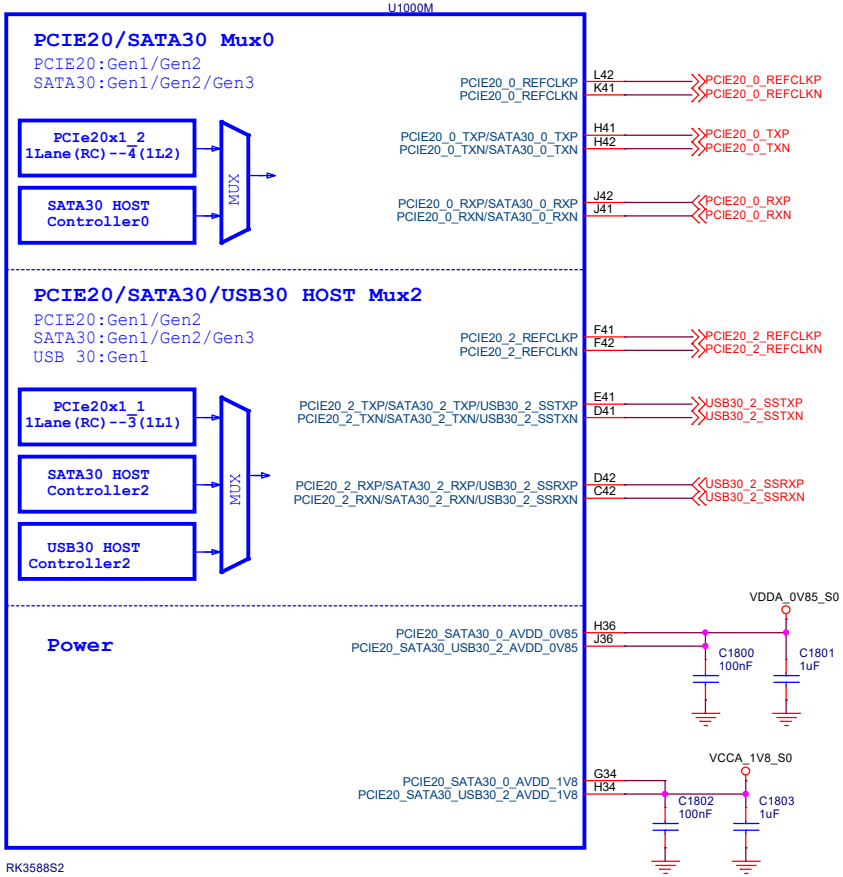
Size	Title: CM5	REV
A2	Page Name: 15_RK3588S_MIPI_Interface	V2.2
Date: Monday, March 25, 2024	Sheet 14 of 19	

RK3588S2(HDMI2.1 TX/eDP1.3 TX)



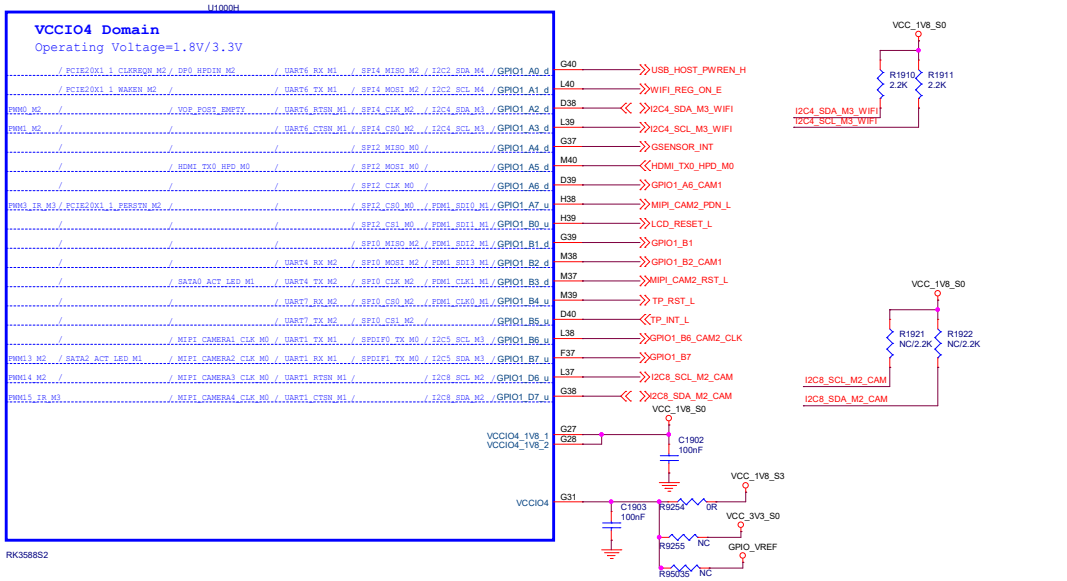
Size: A4	Title: CM5	REV: V2.2
	Page Name: 16_RK3588S_HDMI_eDP_Interface	
Date: Monday, March 25, 2024	Sheet 15 of 19	

RK3588S2(PCIE20/SATA30/USB30)

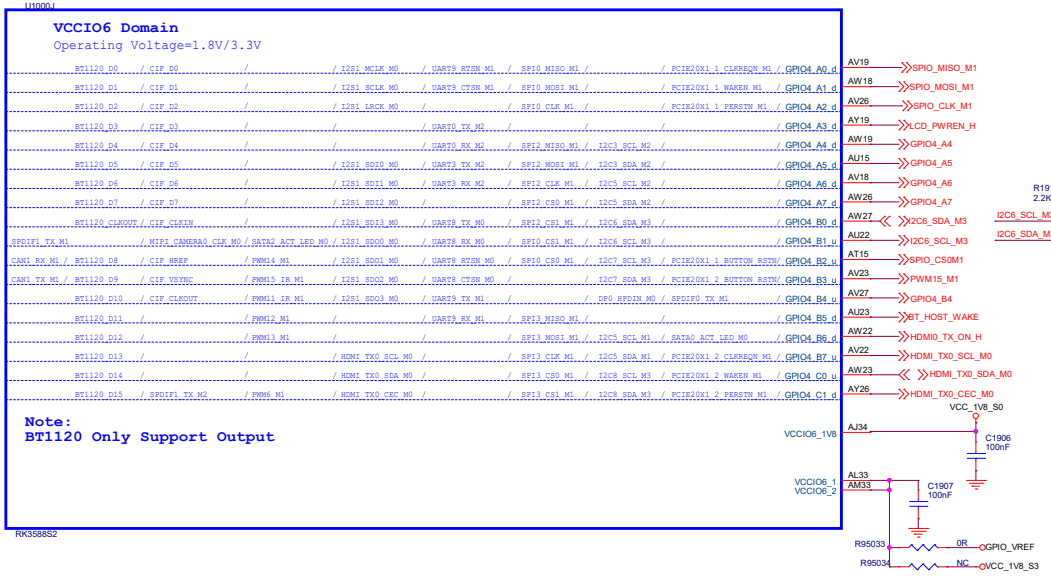


Size	Title: CM5	REV
A3	Page Name: 17_RK3588S PCIE2_SATA3_USB3_PHY	V2.2
Date: Monday, March 25, 2024	Sheet 16 of 19	

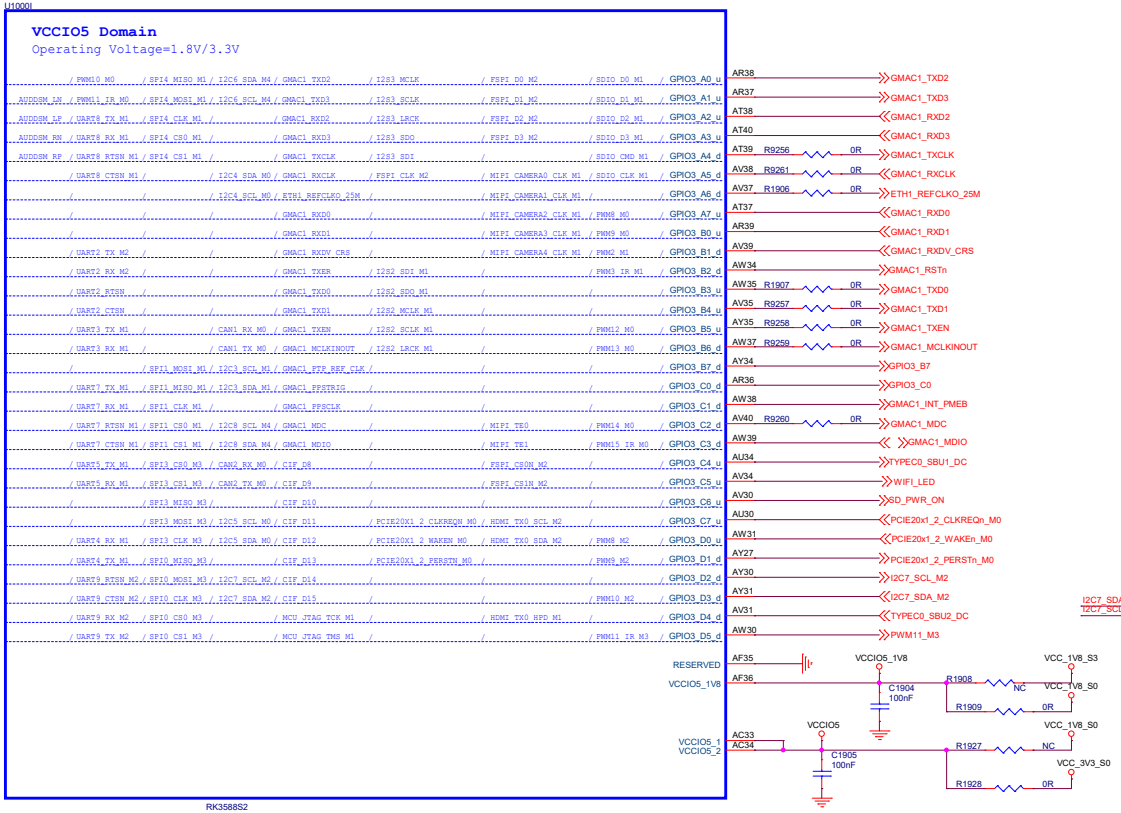
RK3588S2 (VCCIO4 Domain)



RK3588S2 (VCCIO6 Domain)



RK3588S2 (VCCIO5 Domain)



radxa			
Size	Title: CM5		REV
A2	Page Name: 18_RK3588S GPIO		V2.2
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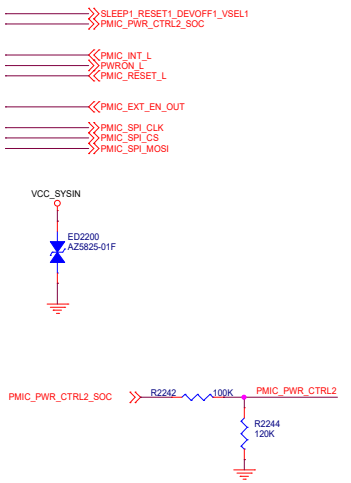
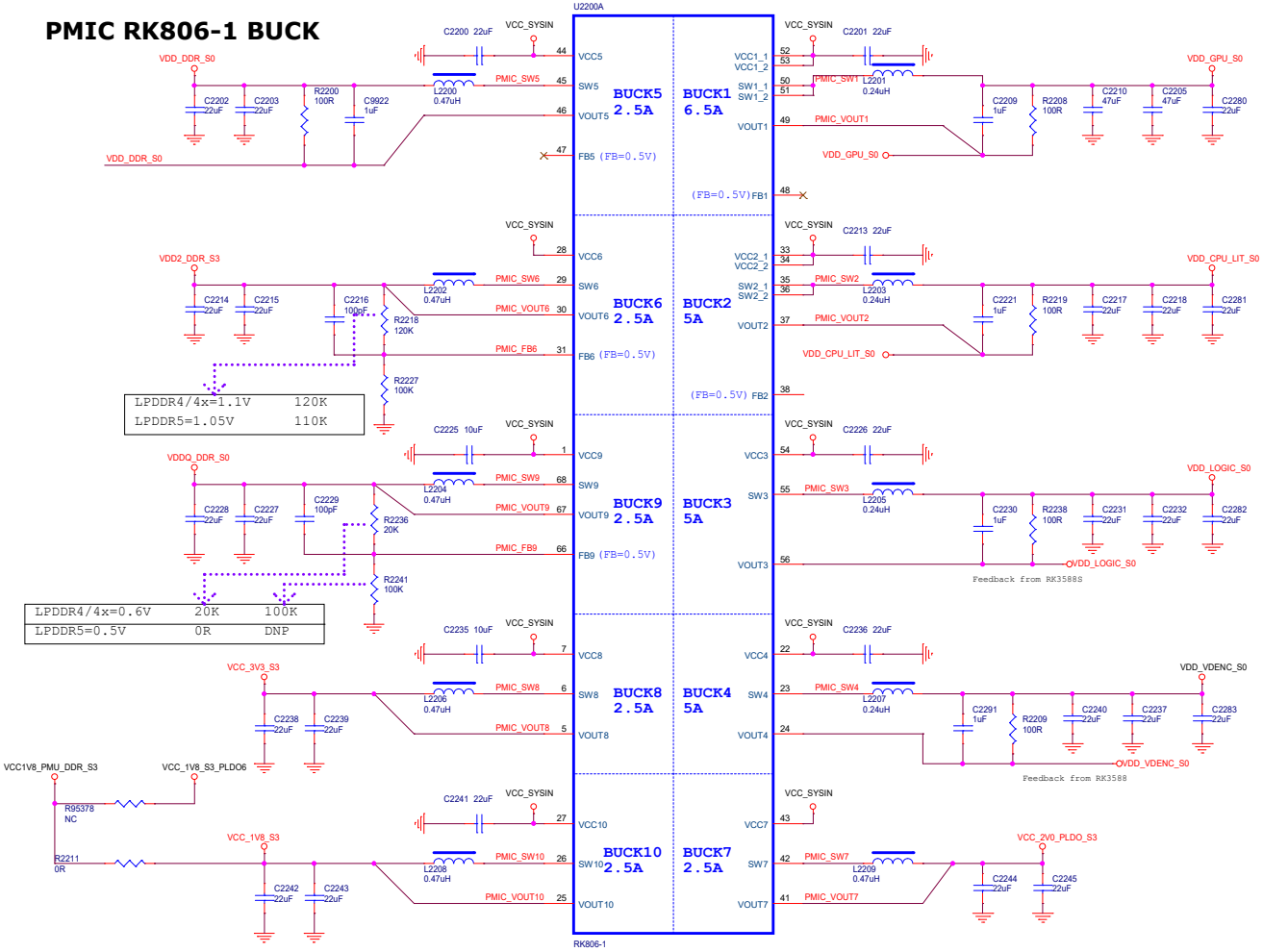
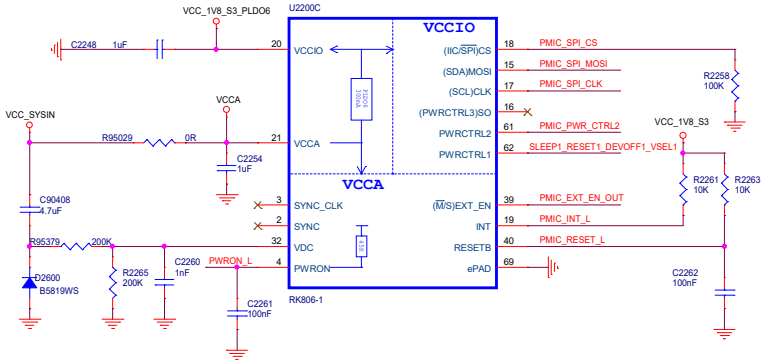
PMIC1 RK806-1



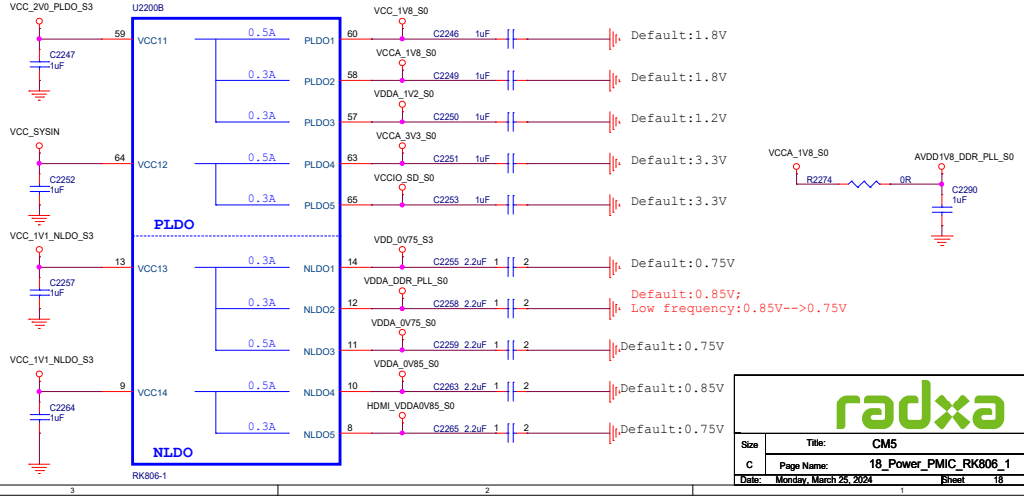
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO



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C	Page Name: 18_Power_PMIC_RK806_1		V2.2
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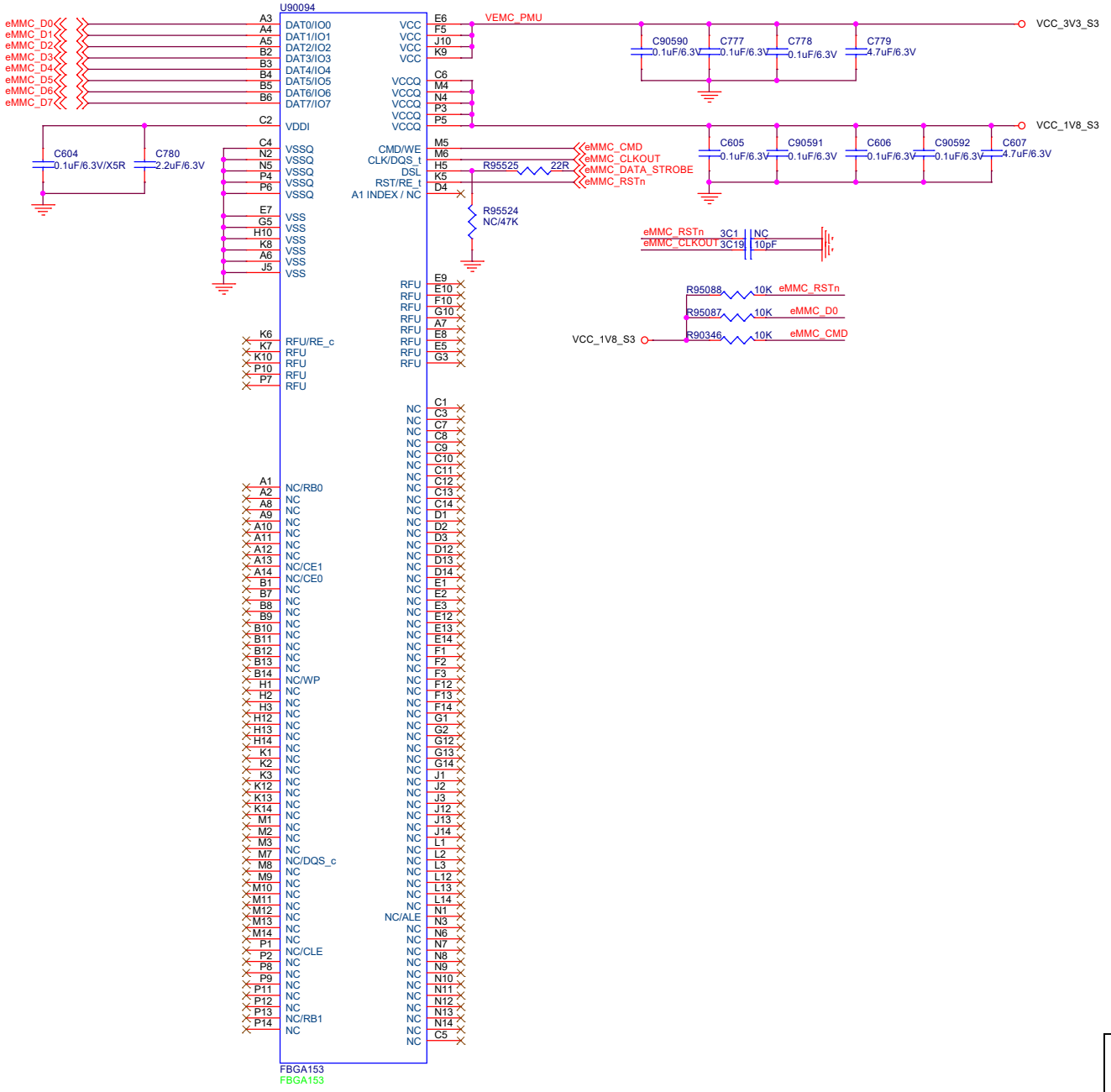
eMMC



Size A3	Title: CM5	REV V2.2
	Page Name: 19_eMMC	
Date: Monday, March 25, 2024	Sheet 19 of 19	