CM5 X2.1

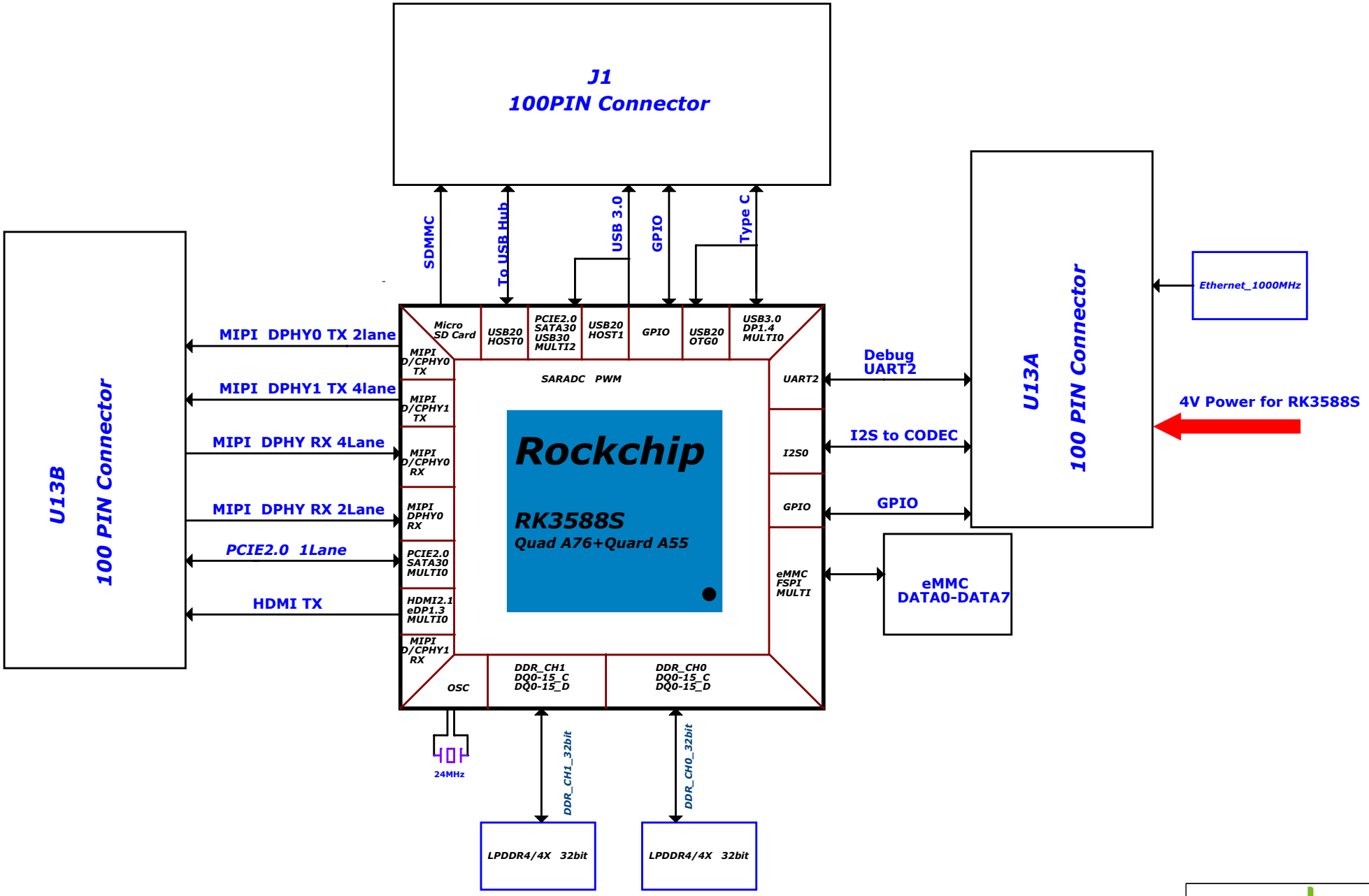
Size	Title: CM5	REV
A4	Page Name: 01.Cover	X2.1
Date: Wednesday, October 11, 2023	Sheet 01 of 19	

Index

radxa

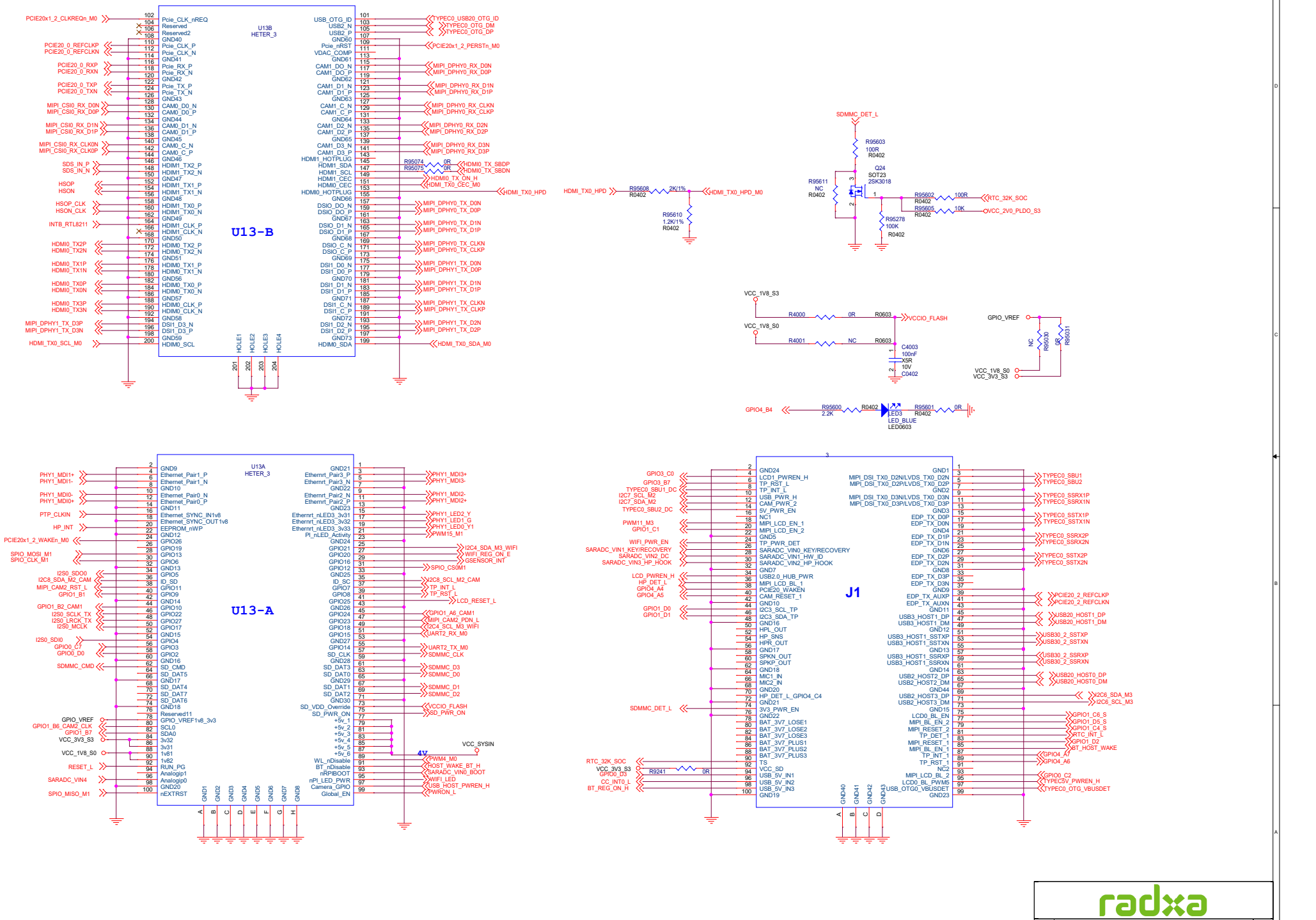
Size	Title: CM5	REV
A4	Page Name: 02_INDEX	X2.1
Date: Wednesday, October 11, 2023	Sheet 02 of 19	

RK3588S Block Diagram

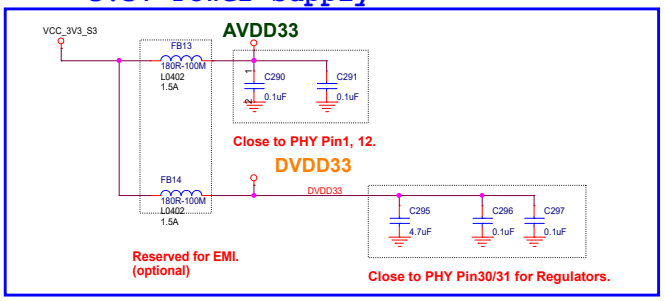


radxa

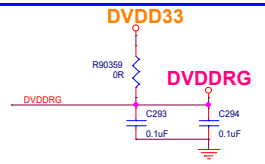
Size	Title:	REV
A2	CM5	X2.1
	Page Name: 03_Block	
Date: Wednesday, October 11, 2023	Sheet 03 of 19	


U13-B
U13B
HETER_3
U13-A
U13A
HETER_3
J1
PCIE20x1_2_CLKREQn_M0
PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
PCIE20_0_RXP
PCIE20_0_RXN
PCIE20_0_TXP
PCIE20_0_TXN
MIPI_CSI0_RX_D0N
MIPI_CSI0_RX_D0P
MIPI_CSI0_RX_D1N
MIPI_CSI0_RX_D1P
MIPI_CSI0_RX_CLK0N
MIPI_CSI0_RX_CLK0P
SDS_IN_P
SDS_IN_N
HSOP
HSON
HSOP_CLK
HSON_CLK
INTB_RTL8211
HDMI0_TX2P
HDMI0_TX2N
HDMI0_TX1P
HDMI0_TX1N
HDMI0_TX0P
HDMI0_TX0N
HDMI0_TX3P
HDMI0_TX3N
MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N
HDMI_TX0_SCL_M0
HOLE1
HOLE2
HOLE3
HOLE4
USB_OTG_ID
USB2_N
USB2_P
Pcie_nRST
VDAC_COMP
CAM1_D0_N
CAM1_D0_P
CAM1_D1_N
CAM1_D1_P
CAM1_C_N
CAM1_C_P
CAM1_D2_N
CAM1_D2_P
CAM1_D3_N
CAM1_D3_P
HDMI1_HOTPLUG
HDMI1_SDA
HDMI1_SCL
HDMI1_CEC
HDMI0_CEC
HDMI0_HOTPLUG
DSIO_D0_N
DSIO_D0_P
DSIO_D1_N
DSIO_D1_P
DSIO_C_N
DSIO_C_P
DSI1_D0_N
DSI1_D0_P
DSI1_D1_N
DSI1_D1_P
DSI1_C_N
DSI1_C_P
DSI1_D2_N
DSI1_D2_P
HDMI0_SDA
TYPEC0_USB20_OTG_ID
TYPEC0_OTG_DM
TYPEC0_OTG_DP
PCIE20x1_2_PERSTn_M0
MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D3N
MIPI_DPHY0_RX_D3P
R95074 0R
R95075 0R
HDMI0_TX_SBDP
HDMI0_TX_SBDN
HDMI0_TX_ON_H
HDMI_TX0_CEC_M0
HDMI_TX0_HPD
MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_CLKP
MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D2P
HDMI_TX0_SDA_M0
HDMI_TX0_HPD
R95608 2K/1%
R0402
HDMI_TX0_HPD_M0
R95610 1.2K/1%
R0402
SDMMC_DET_L
R95603 100R
R0402
Q24
SOT23
2SK3018
R95611 NC
R0402
R95602 100R
R0402
RTC_32K_SOC
R95605 10K
R0402
VCC_2V0_PLDO_S3
R95278 100K
R0402
VCC_1V8_S3
R4000 0R R0603
VCCIO_FLASH
VCC_1V8_S0
R4001 NC R0603
C4003 100nF X5R 10V
C0402
GPIO_VREF
R95030 NC
R95031 0R
VCC_1V8_S0
VCC_3V3_S3
GPIO4_B4
R95600 2.2K
R0402
LED3
LED_BLUE
LED0603
R95601 0R
R0402
GND9
Ethernet_Pair1_P
Ethernet_Pair1_N
GND10
Ethernet_Pair0_N
Ethernet_Pair0_P
GND11
Ethernet_SYNC_IN1v8
Ethernet_SYNC_OUT1v8
EEPROM_nWP
GND12
GPIO26
GPIO19
GPIO13
GPIO6
GND13
GPIO5
ID_SD
GPIO11
GPIO9
GND14
GPIO10
GPIO22
GPIO27
GPIO17
GND15
GPIO4
GPIO3
GPIO2
GND16
SD_CMD
SD_DAT5
GND17
SD_DAT4
SD_DAT7
SD_DAT6
GND18
Reserved11
GPIO_VREF1v8_3v3
SCL0
SDA0
3v32
3v31
1v81
1v82
RUN_PG
Analogip1
Analogip0
GND20
nEXTRST
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI0-
PHY1_MDI0+
PTP_CLKIN
HP_INT
PCIE20x1_2_WAKEn_M0
SPIO_MOSI_M1
SPIO_CLK_M1
I2S0_SDO0
I2C8_SDA_M2_CAM
MIPI_CAM2_RST_L
GPIO1_B1
GPIO1_B2_CAM1
I2S0_SCLK_TX
I2S0_LRCK_TX
I2S0_MCLK
I2S0_SDI0
GPIO0_C7
GPIO0_D0
SDMMC_CMD
GPIO_VREF
GPIO1_B6_CAM2_CLK
GPIO1_B7
VCC_3V3_S3
VCC_1V8_S0
RESET_L
SARADC_VIN4
SPIO_MISO_M1
GND21
Ethernrt_Pair3_P
Ethernrt_Pair3_N
GND22
Ethernrt_Pair2_N
Ethernrt_Pair2_P
GND23
Ethernrt_nLED3_3v31
Ethernrt_nLED3_3v32
Ethernrt_nLED3_3v33
PI_nLED_Activity
GND24
GPIO21
GPIO20
GPIO16
GPIO12
GND25
ID_SC
GPIO7
GPIO8
GPIO25
GND26
GPIO24
GPIO23
GPIO18
GPIO15
GND27
GPIO14
SD_CLK
GND28
SD_DAT3
SD_DAT0
GND29
SD_DAT1
SD_DAT2
GND30
SD_VDD_Override
SD_PWR_ON
+5v_1
+5v_2
+5v_3
+5v_4
+5v_5
+5v_6
WL_nDisable
BT_nDisable
nRPIBOOT
nPI_LED_PWR
Camera_GPIO
Global_EN
PHY1_MDI3+
PHY1_MDI3-
PHY1_MDI2-
PHY1_MDI2+
PHY1_LED2_Y
PHY1_LED1_G
PHY1_LED0_Y1
PWM15_M1
I2C4_SDA_M3_WIFI
WIFI_REG_ON_E
SSENSOR_INT
SPIO_CS0M1
I2C8_SCL_M2_CAM
TP_INT_L
TP_RST_L
LCD_RESET_L
GPIO1_A6_CAM1
MIPI_CAM2_PDN_L
I2C4_SCL_M3_WIFI
UART2_RX_M0
UART2_TX_M0
SDMMC_CLK
SDMMC_D3
SDMMC_D0
SDMMC_D1
SDMMC_D2
VCCIO_FLASH
SD_PWR_ON
VCC_SYSIN
4V
PWM4_M0
HOST_WAKE_BT_H
SARADC_VIN0_BOOT
WIFI_LED
USB_HOST_PWREN_H
PWRON_L
GPIO3_C0
GPIO3_B7
TYPEC0_SBU1_DC
I2C7_SCL_M2
I2C7_SDA_M2
TYPEC0_SBU2_DC
PWM11_M3
GPIO1_C1
WIFI_PWR_EN
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN2_DC
SARADC_VIN3_HP_HOOK
LCD_PWREN_H
HP_DET_L
GPIO4_A4
GPIO4_A5
GPIO1_D0
GPIO1_D1
SDMMC_DET_L
RTC_32K_SOC
VCC_3V3_S3
GPIO3_D3
CC_INT0_L
BT_REG_ON_H
R9241 0R
GND24
LCD1_PWREN_H
TP_RST_L
TP_INT_L
USB_PWR_H
CAM_PWR_2
5V_PWR_EN
NC1
MIPI_LCD_EN_1
MIPI_LCD_EN_2
GND5
TP_PWR_DET
SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_HP_HOOK
GND7
USB2.0_HUB_PWR
MIPI_LCD_BL_1
PCIE20_WAKEN
CAM_RESET_1
GND10
I2C3_SCL_TP
I2C3_SDA_TP
GND16
HPL_OUT
HP_SNS
HPR_OUT
GND17
SPKN_OUT
SPKP_OUT
GND18
MIC1_IN
MIC2_IN
GND20
HP_DET_L_GPIO4_C4
GND21
3V3_PWR_EN
GND22
BAT_3V7_LOSE1
BAT_3V7_LOSE2
BAT_3V7_LOSE3
BAT_3V7_PLUS1
BAT_3V7_PLUS2
BAT_3V7_PLUS3
TS
VCC_SD
USB_5V_IN1
USB_5V_IN2
USB_5V_IN3
GND19
GND1
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
GND2
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
GND3
EDP_TX_D0P
EDP_TX_D0N
GND4
EDP_TX_D1P
EDP_TX_D1N
GND6
EDP_TX_D2P
EDP_TX_D2N
GND8
EDP_TX_D3P
EDP_TX_D3N
GND9
EDP_TX_AUXP
EDP_TX_AUXN
GND11
USB3_HOST1_DP
USB3_HOST1_DM
GND12
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
GND13
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
GND14
USB2_HOST2_DP
USB2_HOST2_DM
GND44
USB2_HOST3_DP
USB2_HOST3_DM
GND15
LCD0_BL_EN
MIPI_BL_EN_2
MIPI_RESET_2
TP_DET_1
MIPI_RESET_1
MIPI_BL_EN_1
TP_INT_1
TP_RST_1
NC2
MIPI_LCD_BL_2
LCD0_BL_PWM5
USB_OTG0_VBUSDET
GND23
TYPEC0_SBU1
TYPEC0_SBU2
TYPEC0_SSRX1P
TYPEC0_SSRX1N
TYPEC0_SSTX1P
TYPEC0_SSTX1N
TYPEC0_SSRX2P
TYPEC0_SSRX2N
TYPEC0_SSTX2P
TYPEC0_SSTX2N
PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
USB20_HOST1_DP
USB20_HOST1_DM
USB30_2_SSTXP
USB30_2_SSTXN
USB30_2_SSRXP
USB30_2_SSRXN
USB20_HOST0_DP
USB20_HOST0_DM
I2C6_SDA_M3
I2C6_SCL_M3
GPIO1_C6_S
GPIO1_D5_S
GPIO1_C4_S
RTC_INT_L
GPIO1_D2
RT_HOST_WAKE
GPIO4_A7
GPIO4_A6
GPIO0_C2
TYPEC5V_PWREN_H
TYPEC0_OTG_VBUSDET
radxa
Size C
Title: CM5
REV V2.1
Page Name: 04_connetor
Date: Wednesday, October 11, 2023
Sheet 04 of 19

3.3V Power Supply



RGMII Power



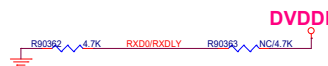
Note 1: R5 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

Note 2: DVDDRG must be short (or R5 be mounted) to DVDD33 if the external RGMII 3.3V is selected.

Note 3: R5 must be removed if the internal 2.5V/1.8V/1.5V RGMII is selected.

Note 4: CAPs must be closed to pin29 for EMI consideration.

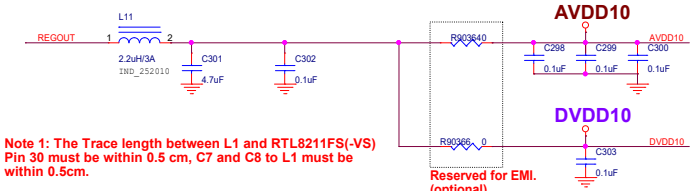
RGMII RXC Delay Config.



Pull-up for additional 2ns delay to RXC for data latching.

RSET

Switching Regulator

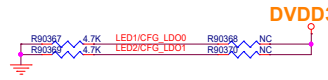


Note 1: The Trace length between L1 and RTL8211FS(-VS) Pin 30 must be within 0.5 cm, C7 and C8 to L1 must be within 0.5cm.

Note 2: Bypass CAPs close to PHY AVDD10/DVDD10 power pins.

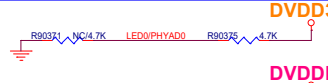
Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

RGMII Voltage Config.



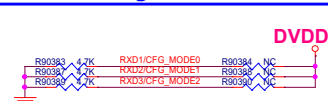
RGMII Power Source	CFG_LDO[1:0]
External 3.3V (default)	2'b00
Internal 2.5V	2'b01
Internal 1.8V	2'b10
Internal 1.5V	2'b11

PHY Address Config.

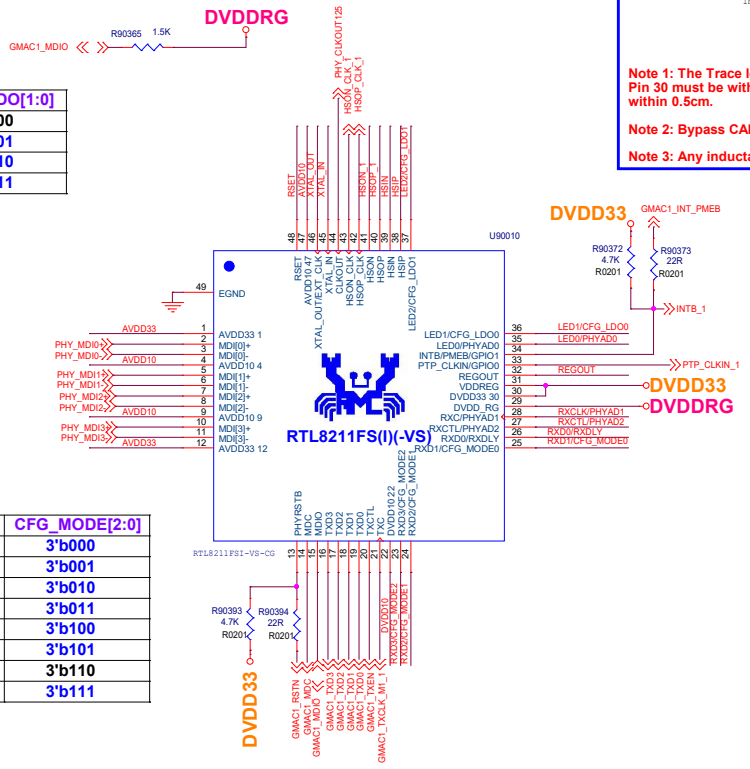


PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

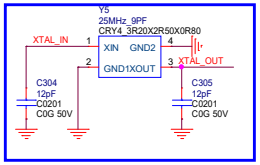
PHY Config.



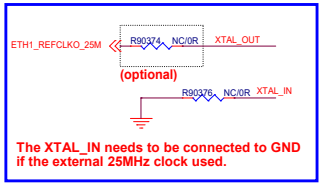
Operating Mode	CFG_MODE[2:0]
UTP <=> RGMII (default)	3'b000
FIBER <=> RGMII	3'b001
UTP/FIBER <=> RGMII	3'b010
UTP <=> SGMII	3'b011
SGMII (PHY) <=> RGMII	3'b100
SGMII (MAC) <=> RGMII	3'b101
UTP <=> FIBER (AUTO)	3'b110
UTP <=> FIBER (FORCE)	3'b111



Crystal Case

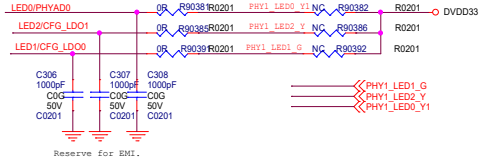


External clock Case



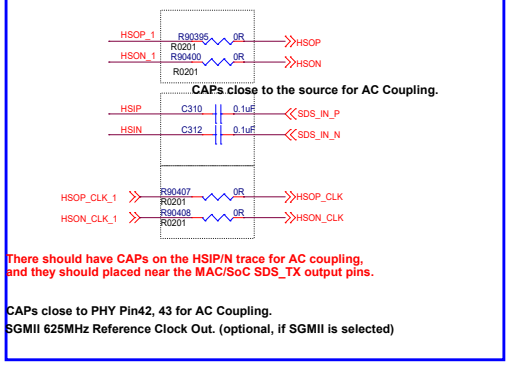
The XTAL_IN needs to be connected to GND if the external 25MHz clock used.

LEDs Configuration



SERDES

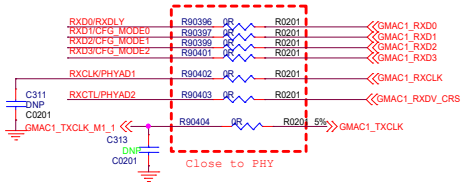
CAPs close to PHY Pin40, 41 for AC Coupling.

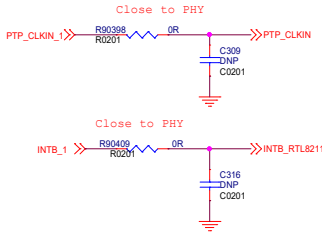


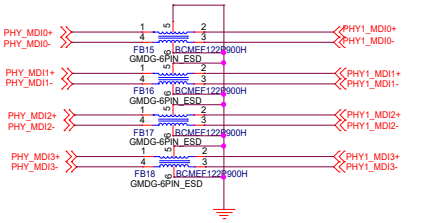
There should have CAPs on the HSIP/N trace for AC coupling, and they should placed near the MAC/SoC SDS_TX output pins.

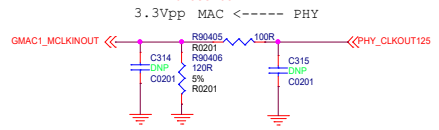
CAPs close to PHY Pin42, 43 for AC Coupling.

SGMII 625MHz Reference Clock Out. (optional, if SGMII is selected)





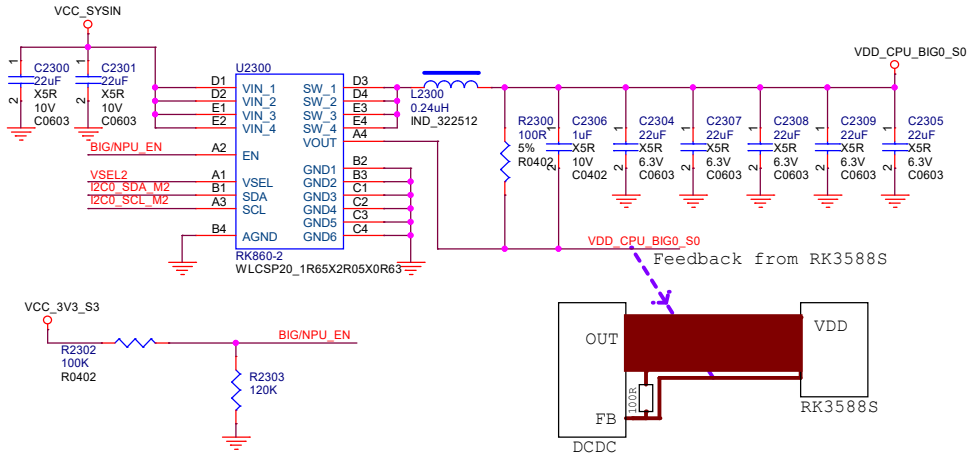




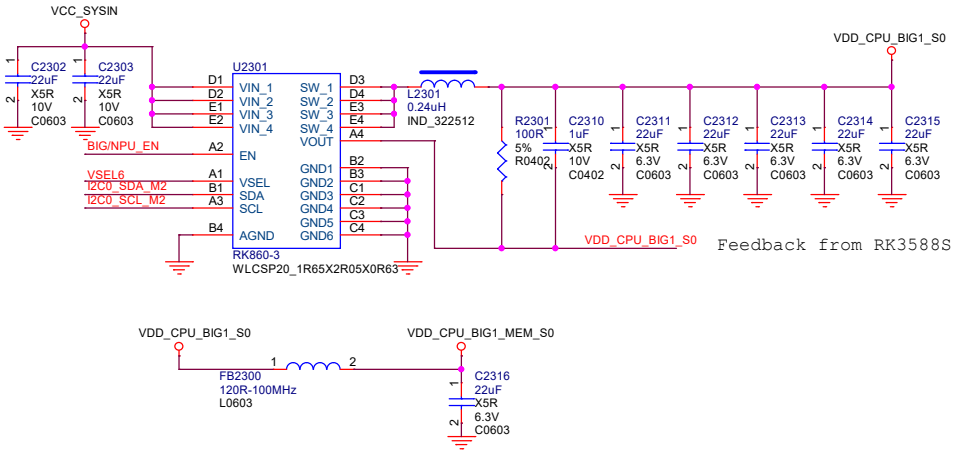
radxa

Size	Title:	REV
C	CM5	X2.1
	Page Name: 05_Ethernet_1000MHz	
Date: Wednesday, October 11, 2023	Sheet 05 of 19	

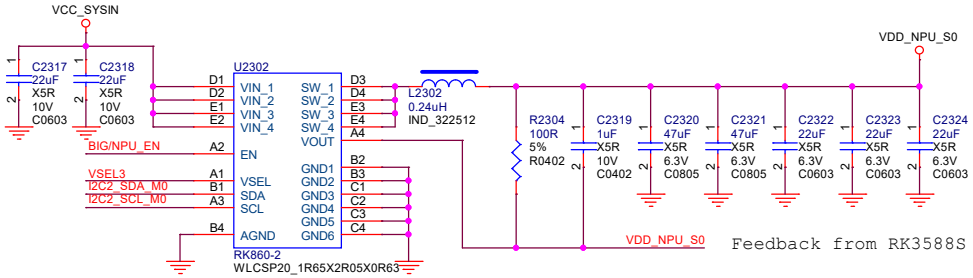
VDD_CPU_BIG0



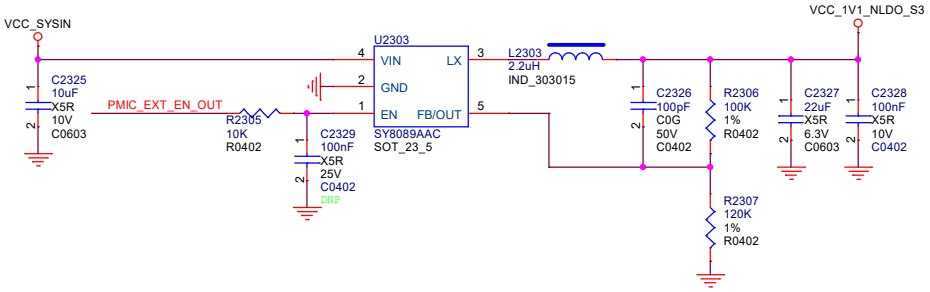
VDD_CPU_BIG1



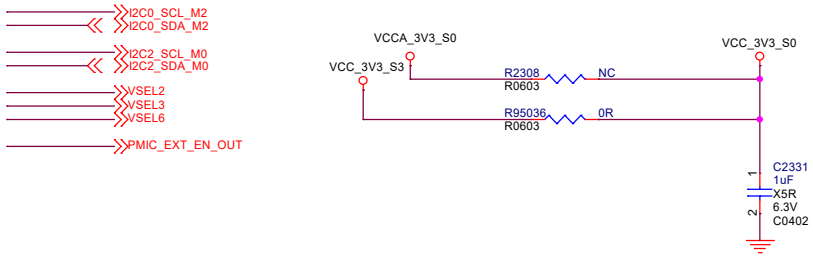
VDD_NPU



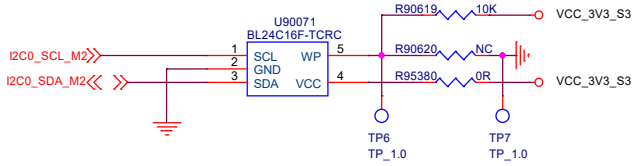
VCC_1V1_NLDO



VCC_3V3_S0



Mechine ID

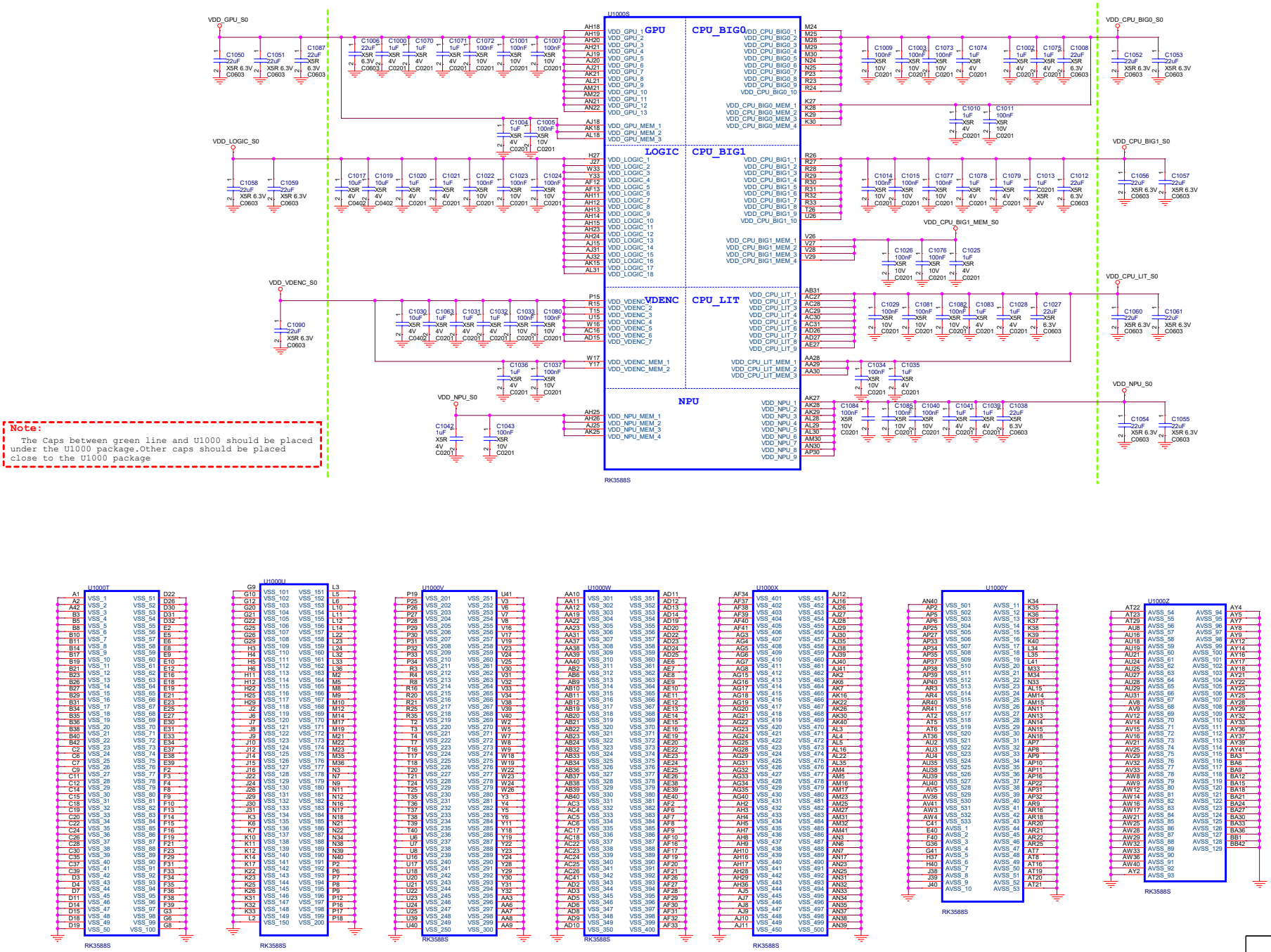


Size	Title: CM5	REV
A3	Page Name: 06_Power_Ext Discrete	X2.1
Date: Wednesday, October 11, 2023	Sheet 06 of 19	

DRAM-LPDDR4/4x_2X32bit

Size	Title: CM5		REV
A2	Page Name: 08_DRAM-LPDDR4_4X_200P		X2.1
Date: Wednesday, October 11, 2023	Sheet 07 of 19		

RK3588S(Power&Gnd)



Size	Title: CM5		REV
A2	Page Name: 09_RK3588S_Power_GND		X2.1
Date: Wednesday, October 11, 2023	Sheet 08 of 19		

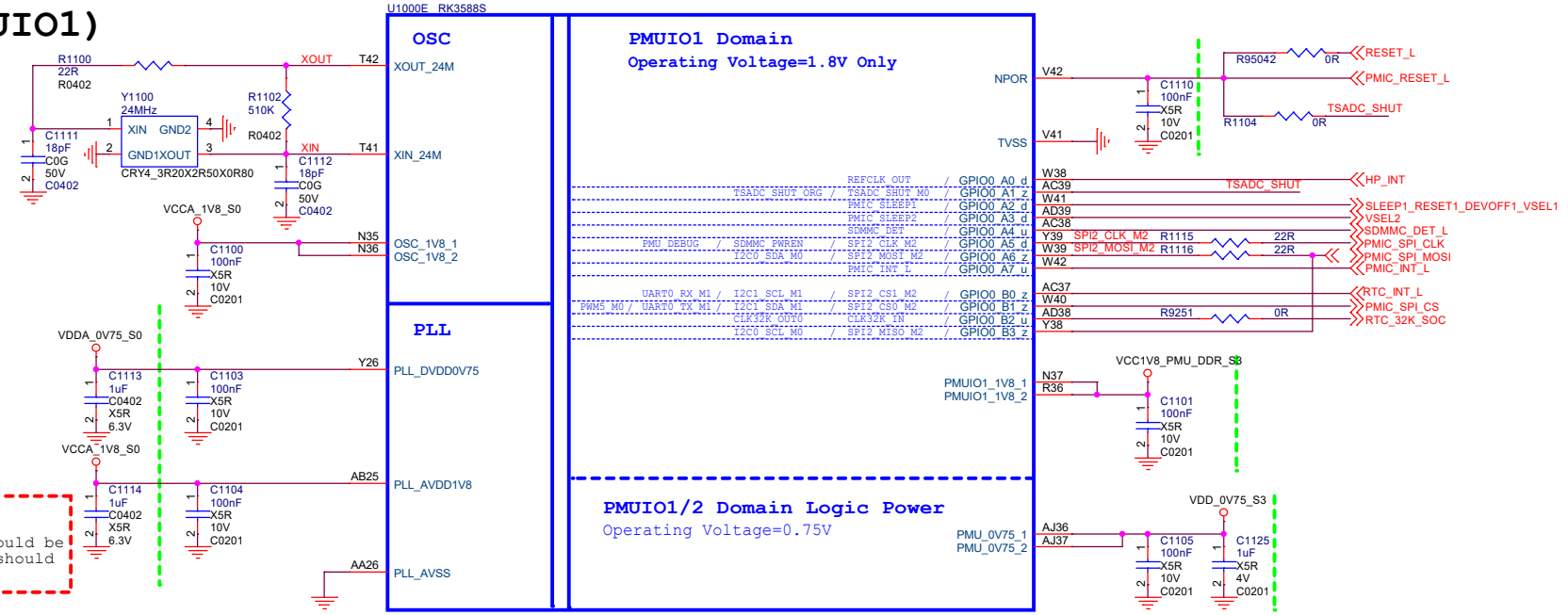
RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

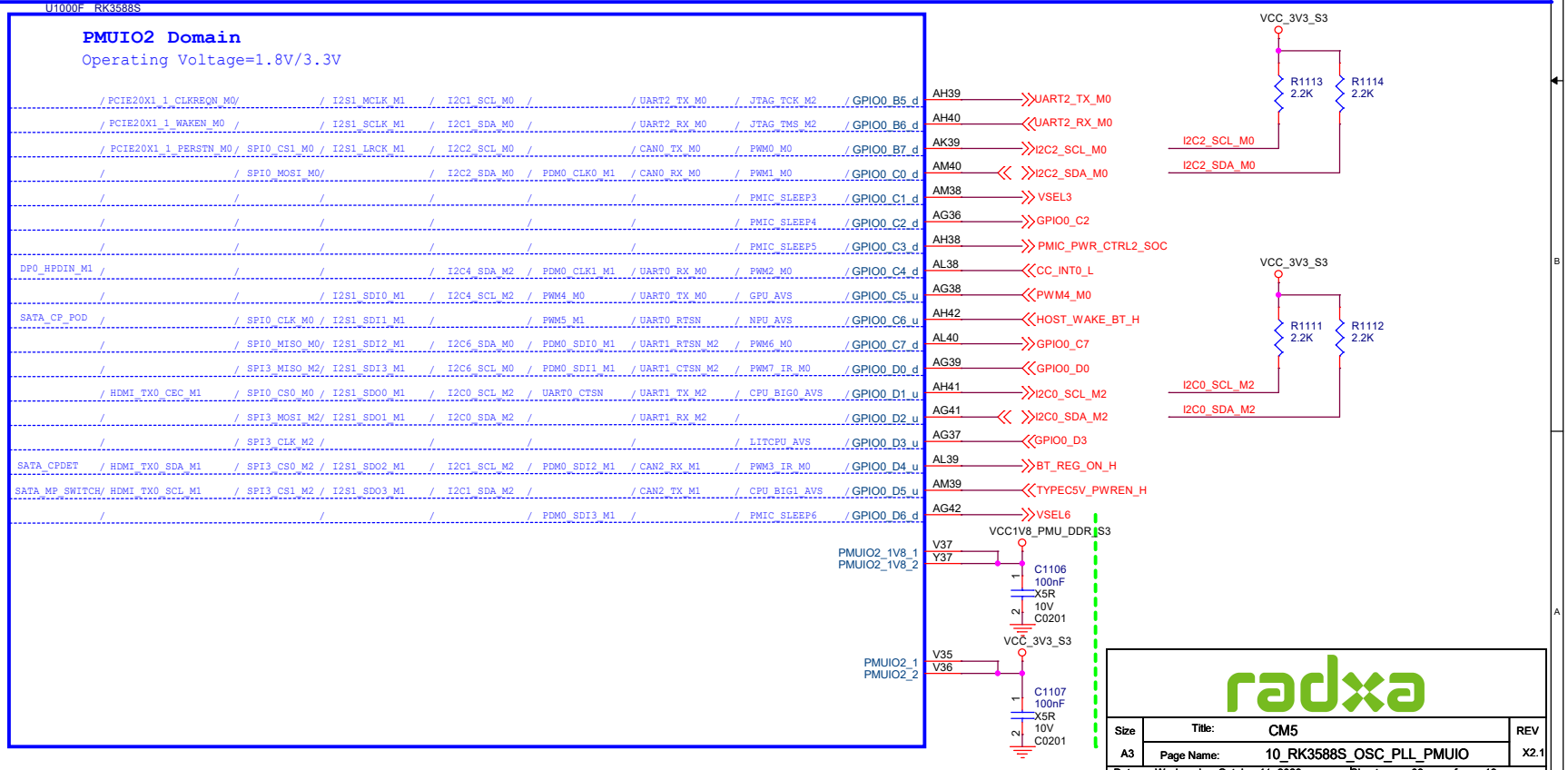
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

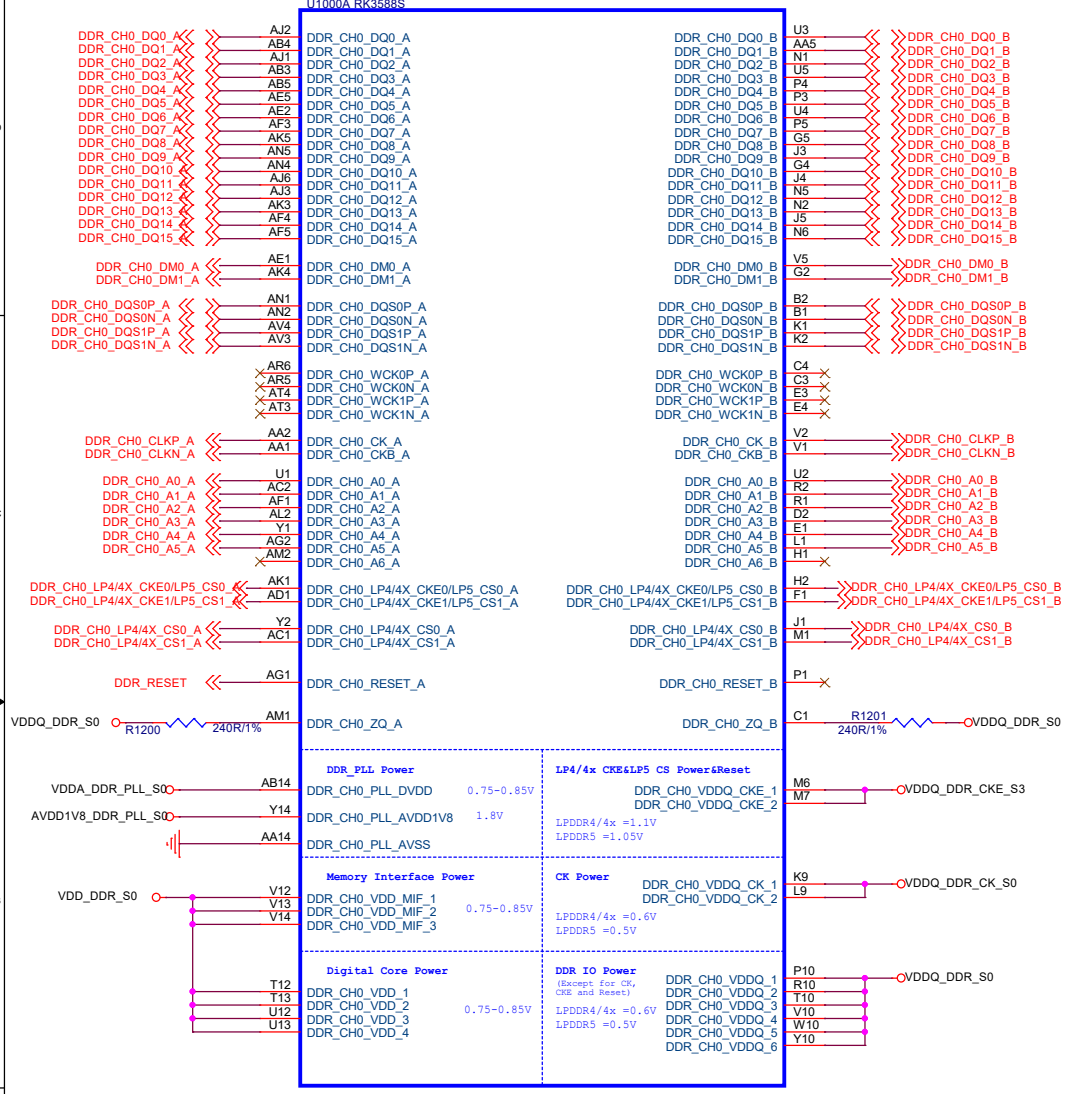


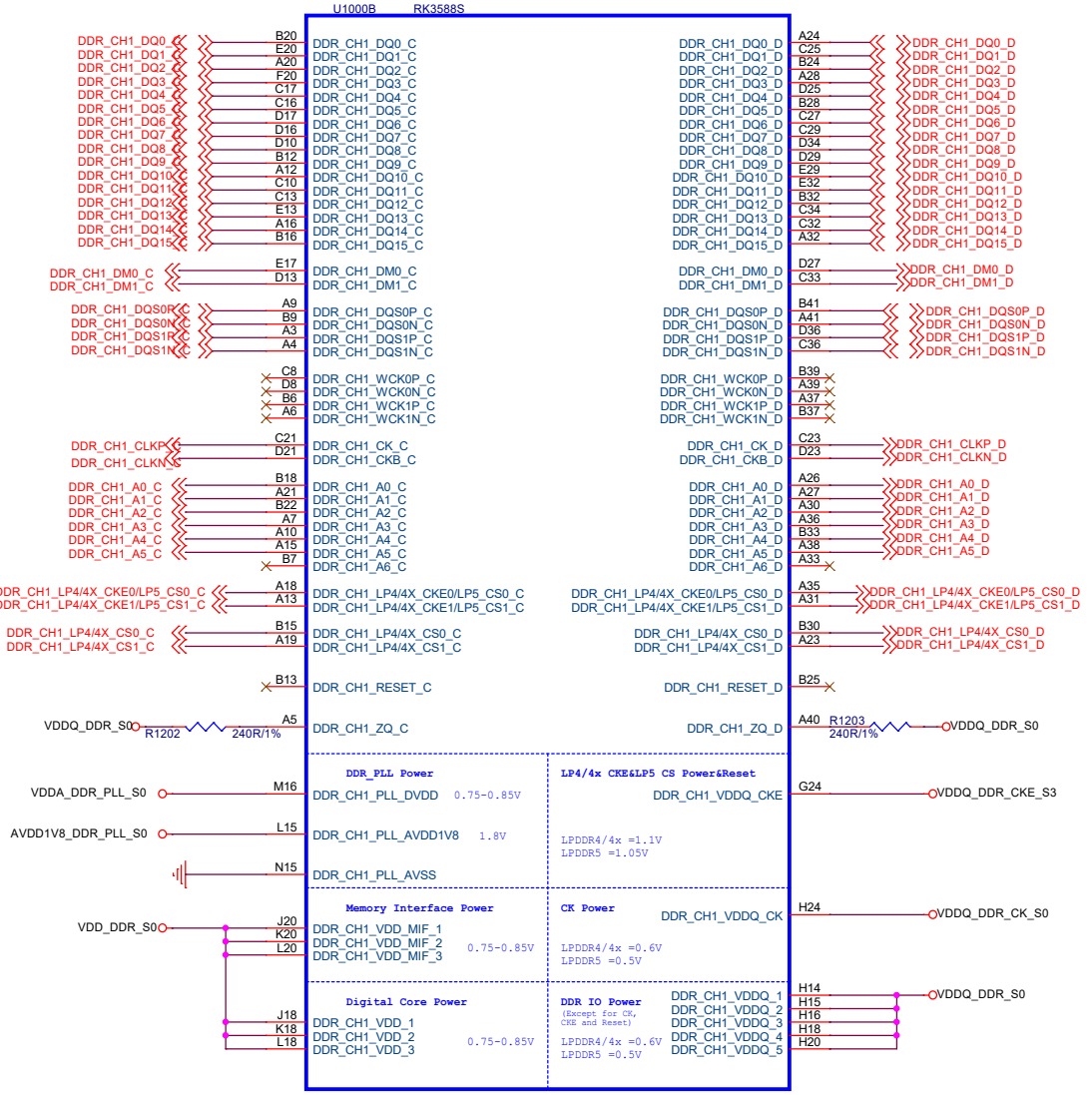
RK3588S(PMUIO2)



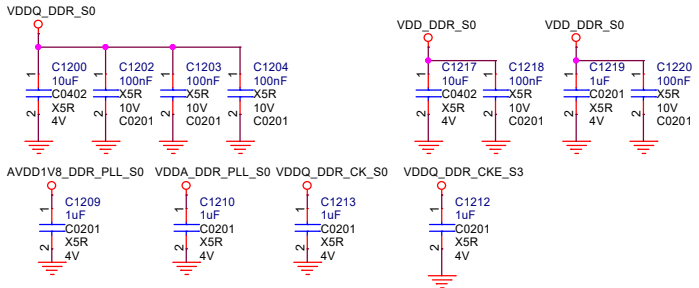
Size	Title: CM5	REV
A3	Page Name: 10_RK3588S_OSC_PLL_PMUIO	X2.1
Date: Wednesday, October 11, 2023	Sheet 09 of 19	

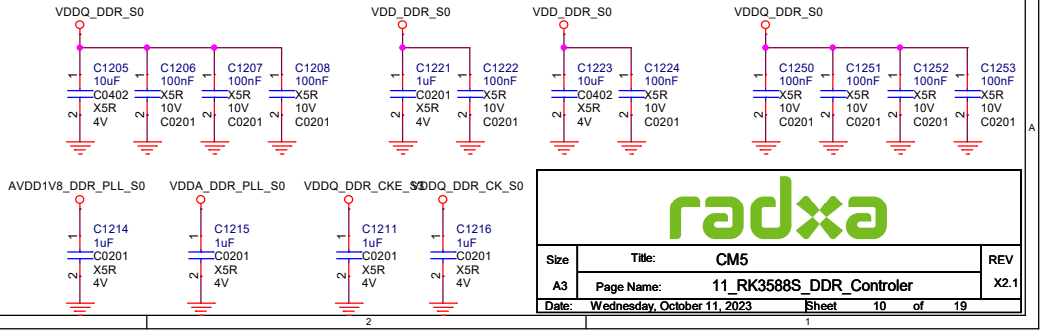
RK3588S(DDR PHY)





DDR FILTER

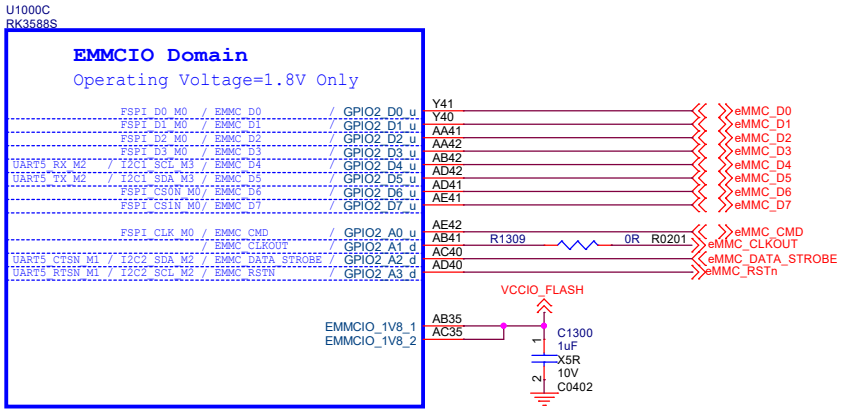




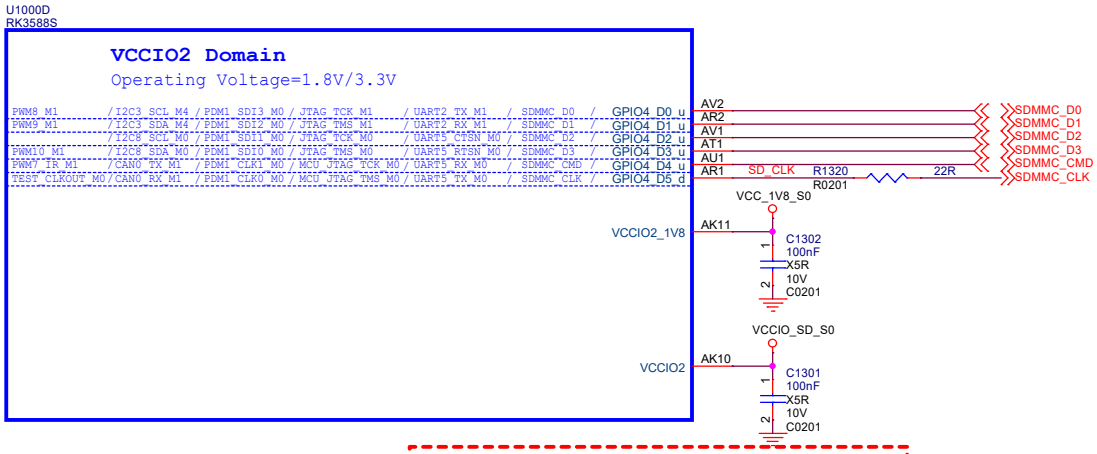
radxa

Size	Title: CM5	REV
A3	Page Name: 11_RK3588S_DDR_Controler	X2.1
Date: Wednesday, October 11, 2023	Sheet 10 of 19	

RK3588S(EMMCIO Domain)



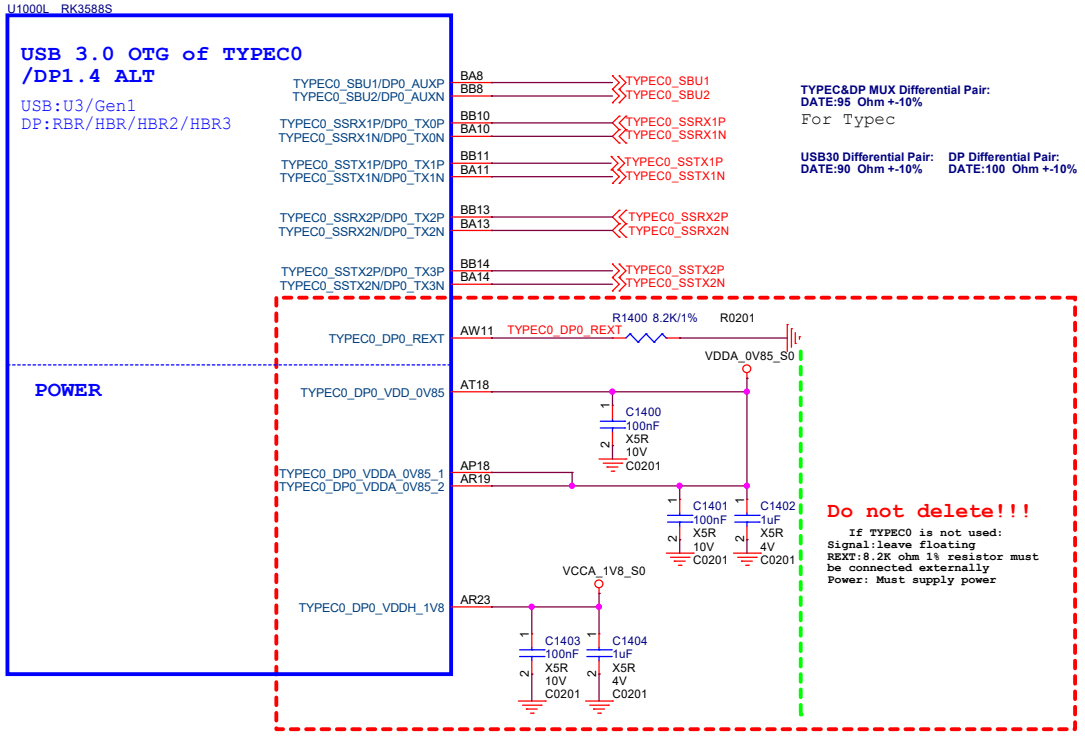
RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Size	Title:	REV
A3	CM5	X2.1
	Page Name: 12_RK3588S_Flash_SD_Controller	
Date: Wednesday, October 11, 2023	Sheet 11 of 19	

RK3588S(USB3.0/DP1.4)

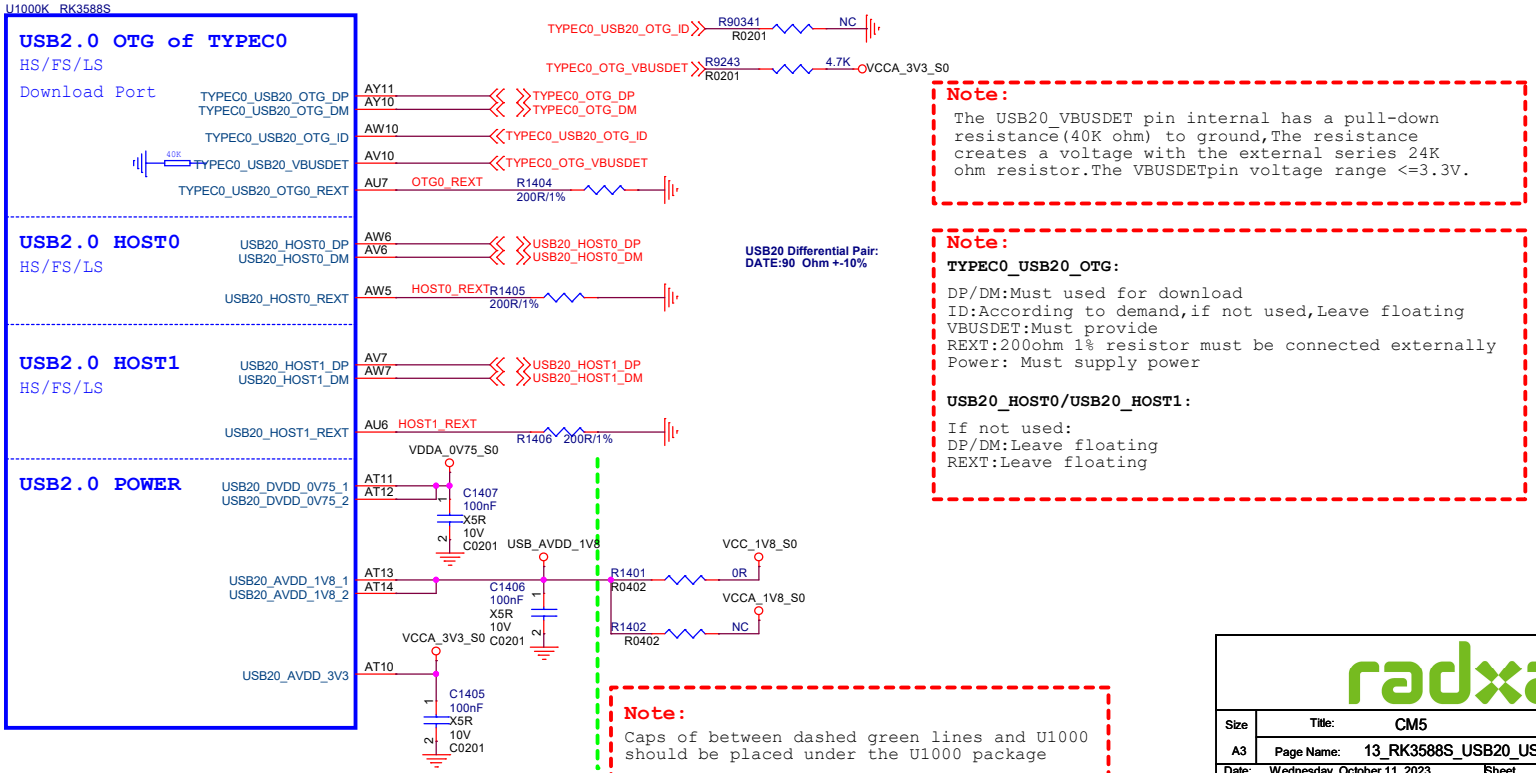


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

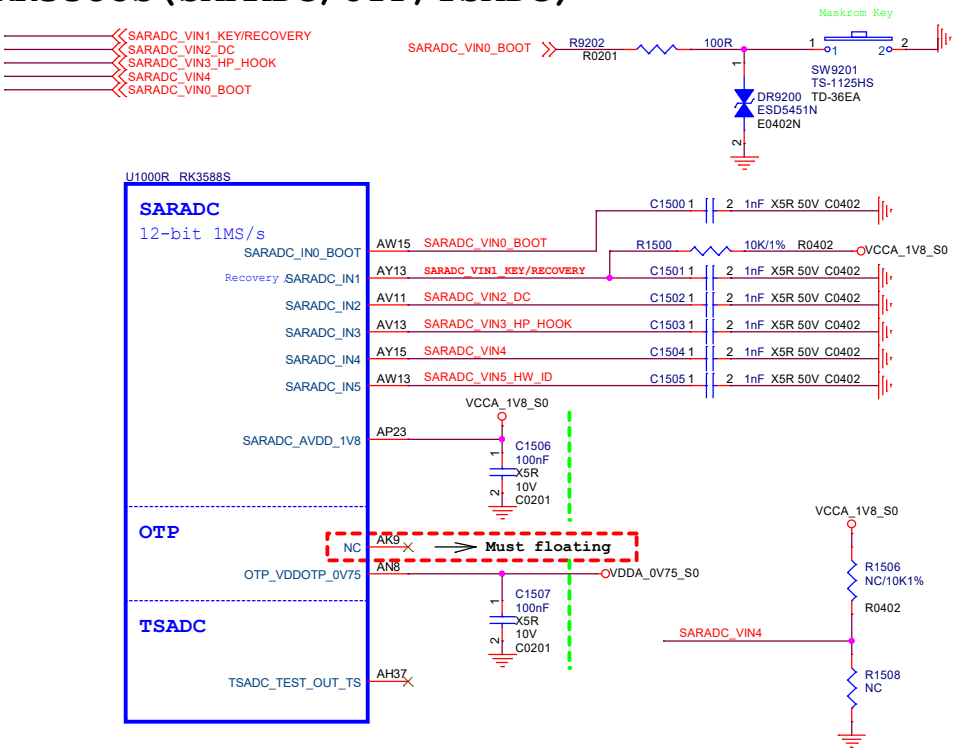
RK3588S(USB2.0)



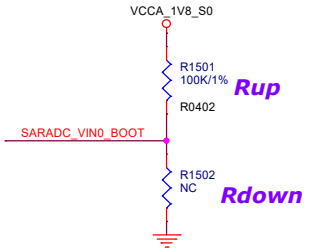
radxa

Size	Title:	REV
A3	CM5	X2.1
	Page Name: 13_RK3588S_USB20_USB30_DP_PHY	
Date: Wednesday, October 11, 2023	Sheet 12 of 19	

RK3588S(SARADC/OTP/TSADC)

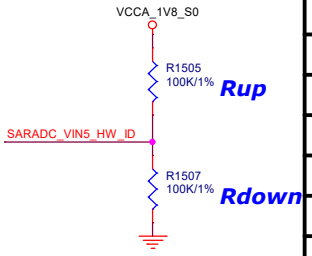


BOOT MODE CONFIG



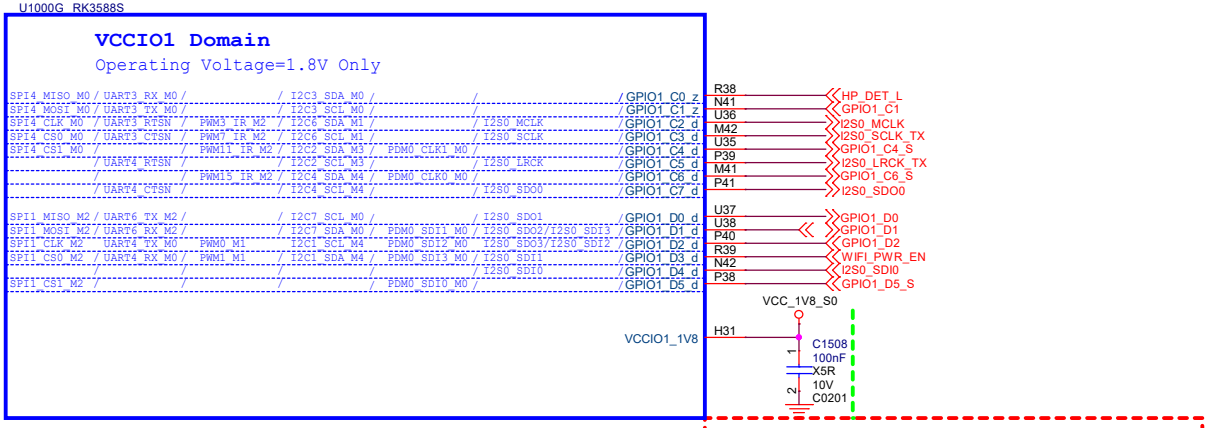
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	NC	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

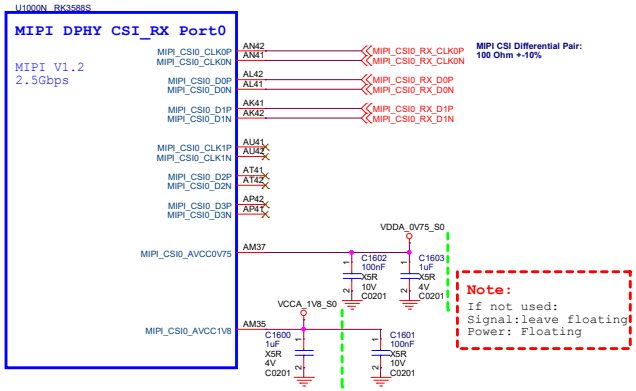
RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Size	Title:	REV
A3	CM5	X2.1
	Page Name: 14_RK3588S_SARADC_1.8V_GPIO	
Date: Wednesday, October 11, 2023	Sheet 13 of 19	

RK3588S(MIPI_DPHY CSI0 RX)

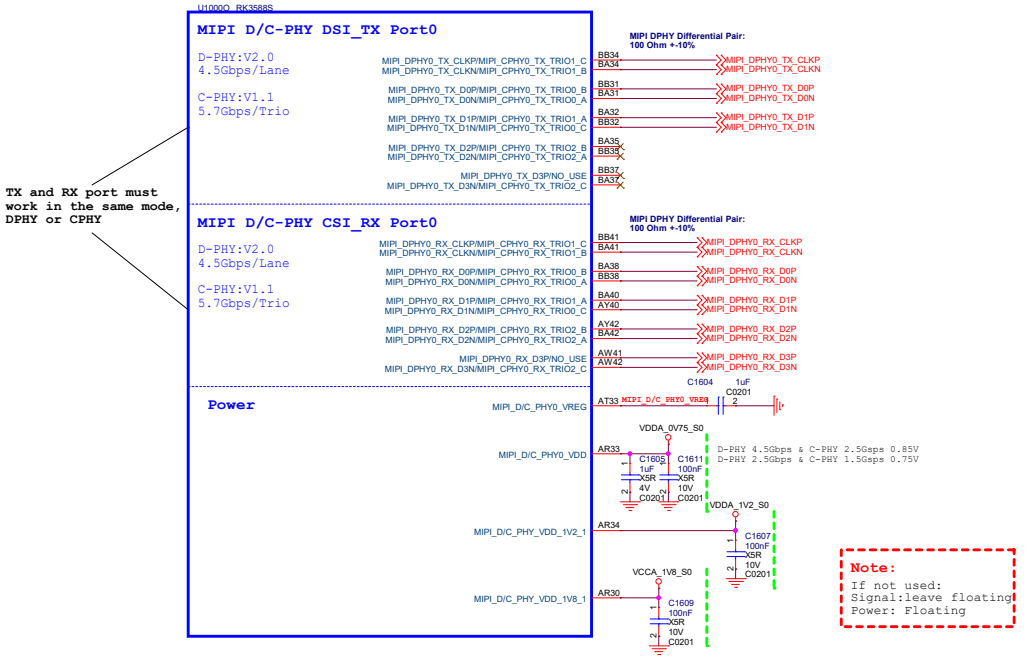


Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

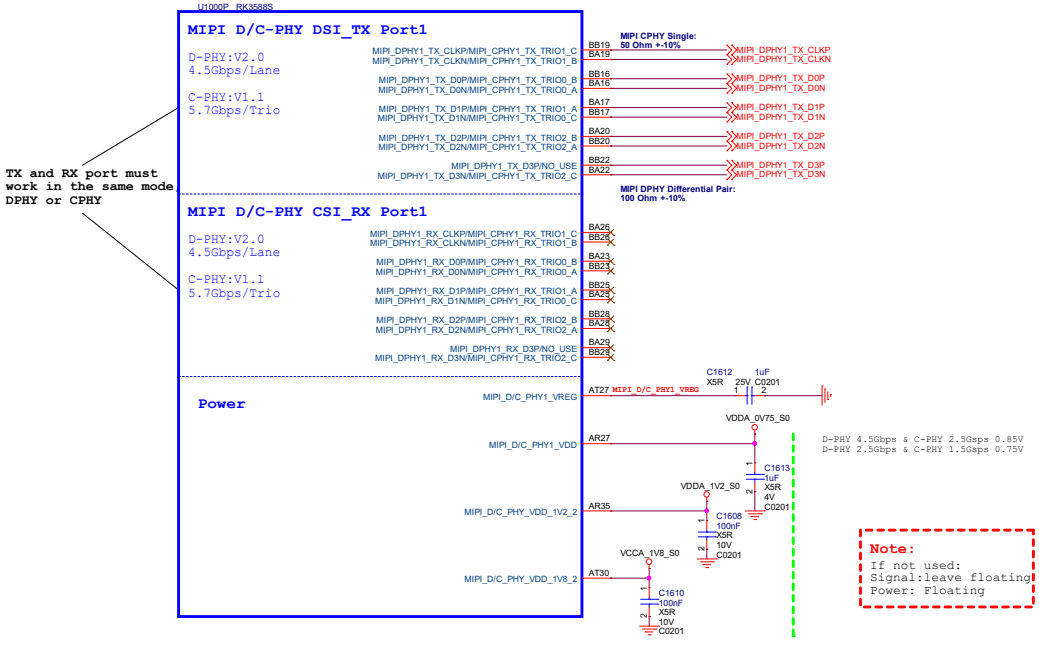
Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



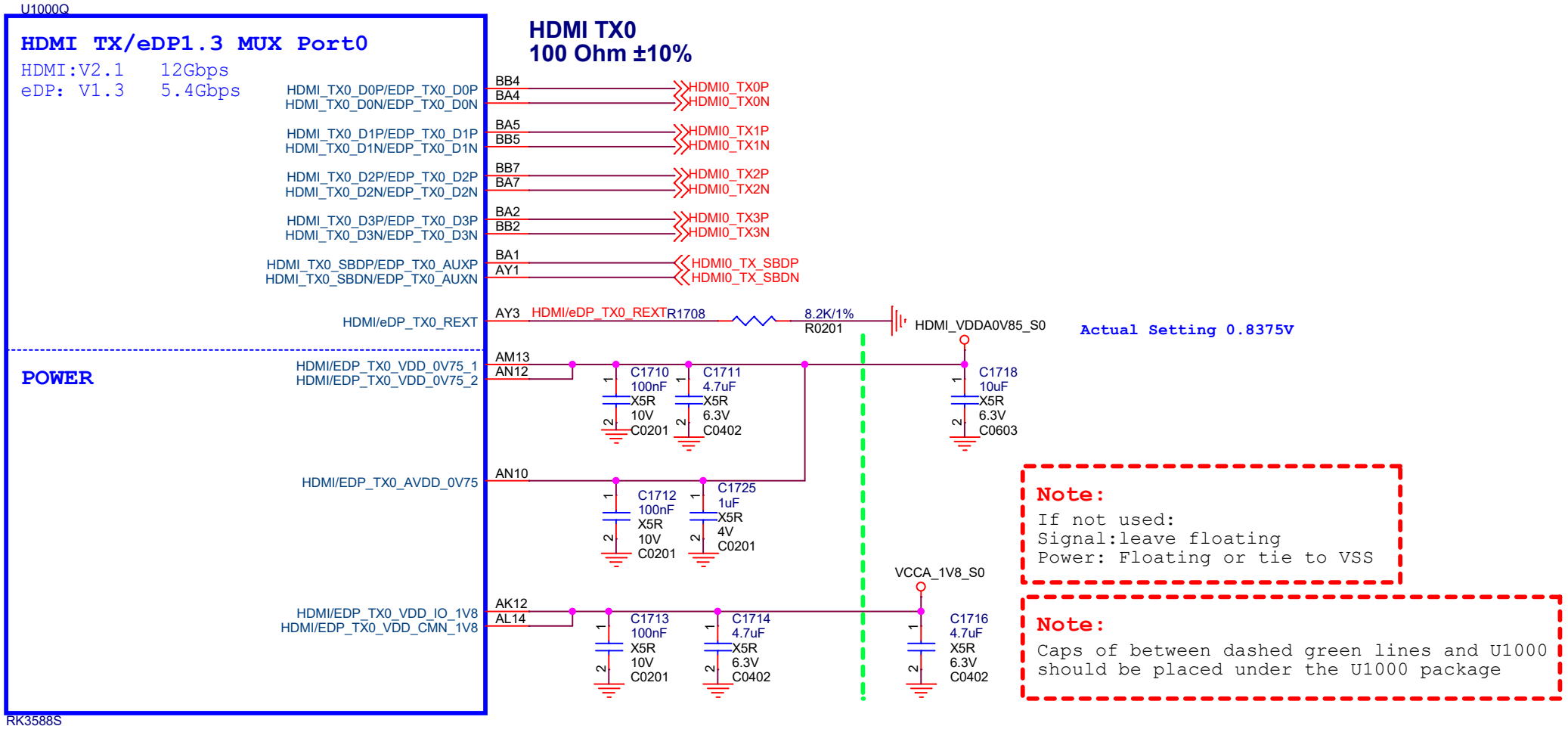
RK3588S(MIPI_D/C PHY1)



Size	Title: CM5		REV
A2	Page Name: 15_RK3588S_MIPI_Interface		X2.1
Date: Wednesday, October 11, 2023	Sheet 14 of 19		

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



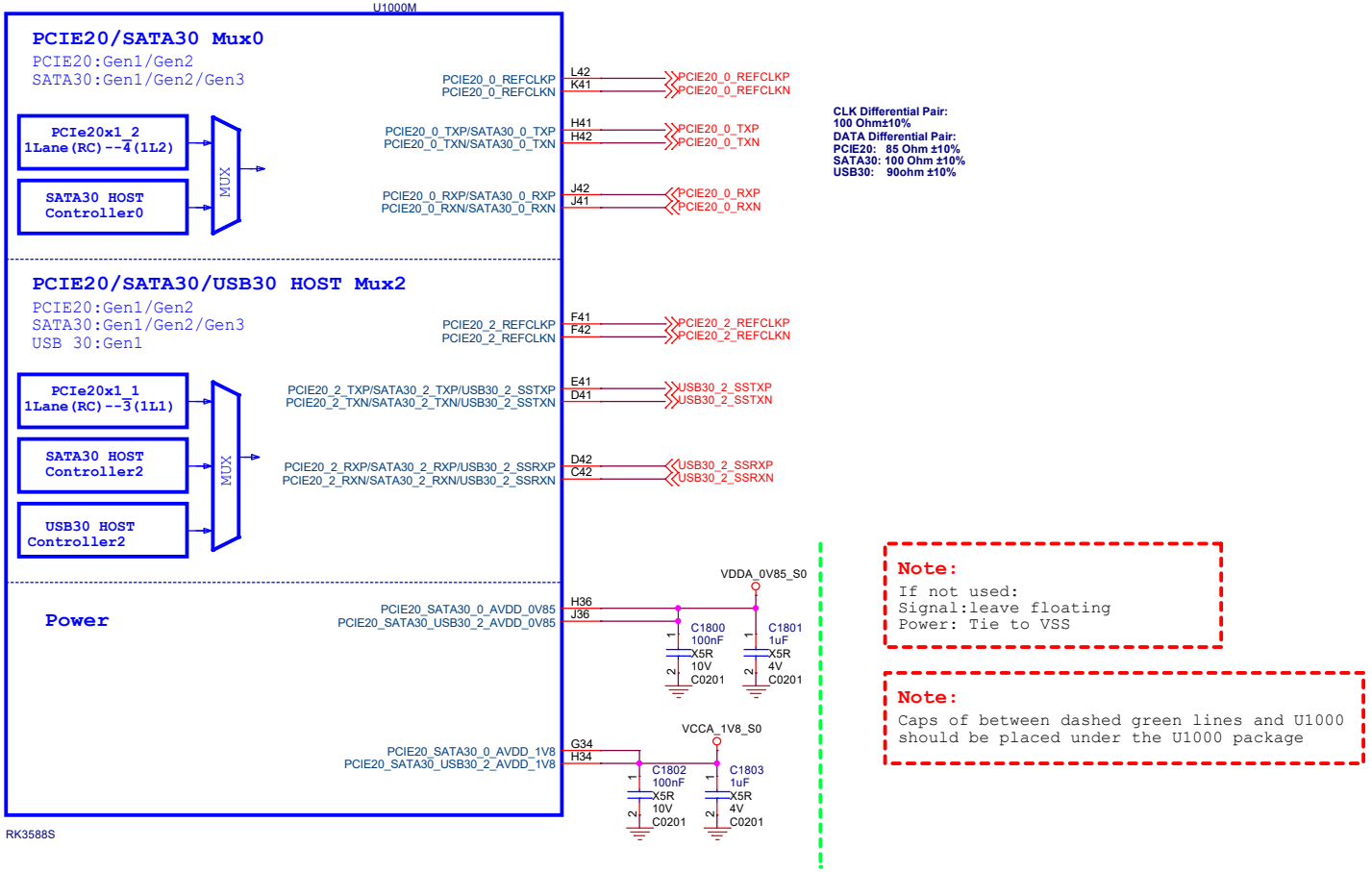
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

radxa

Size	Title:	CM5	REV
A4	Page Name:	16_RK3588S_HDMI_eDP_Interface	X2.1
Date:	Wednesday, October 11, 2023	Sheet 15 of 19	

RK3588S(PCIE20/SATA30/USB30)



Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

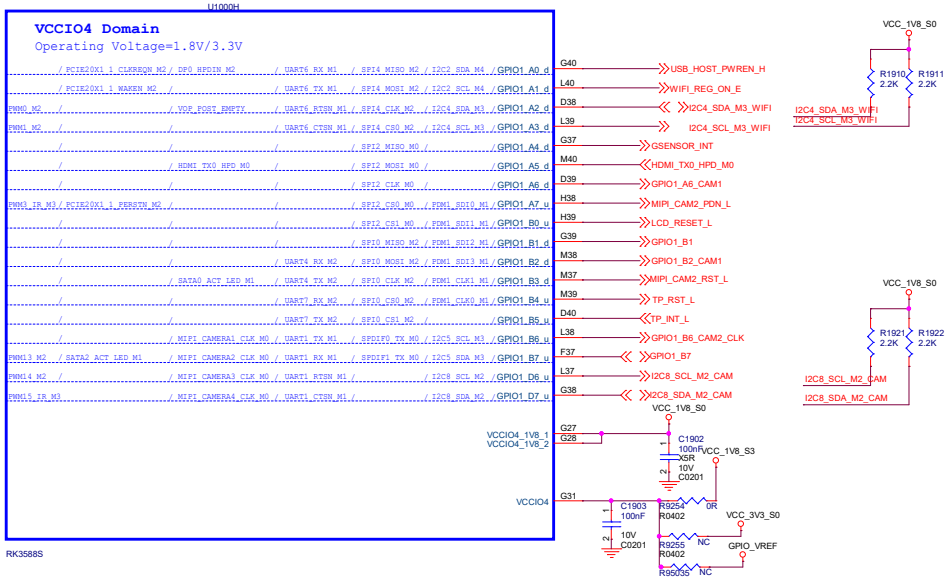
PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

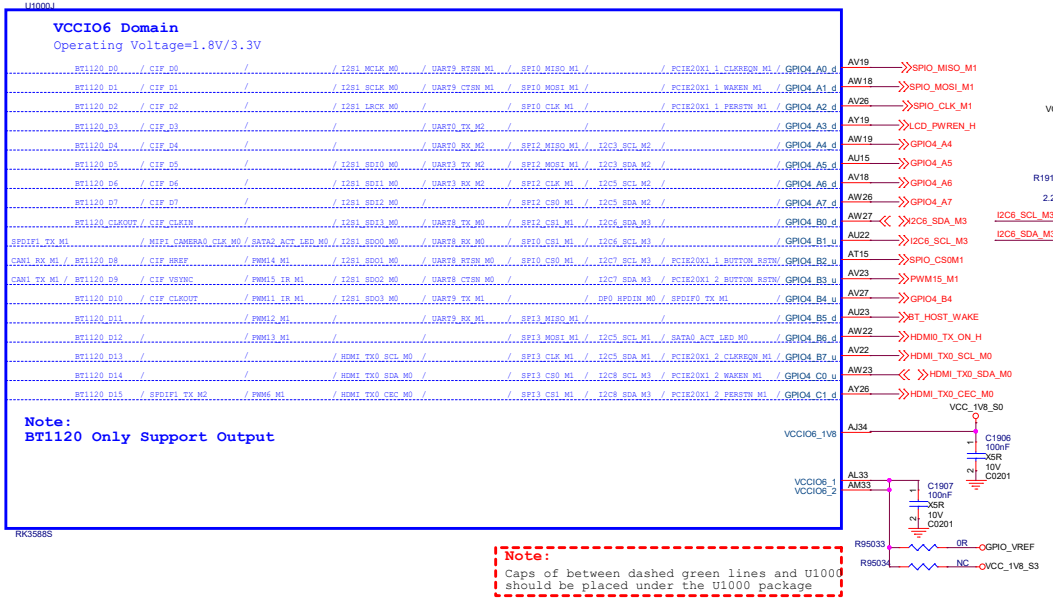
radxa

Size	Title: CM5	REV
A3	Page Name: 17_RK3588S PCIE2_SATA3_USB3_PHY	X2.1
Date: Wednesday, October 11, 2023	Sheet 16 of 19	

RK3588S(VCCIO4 Domain)

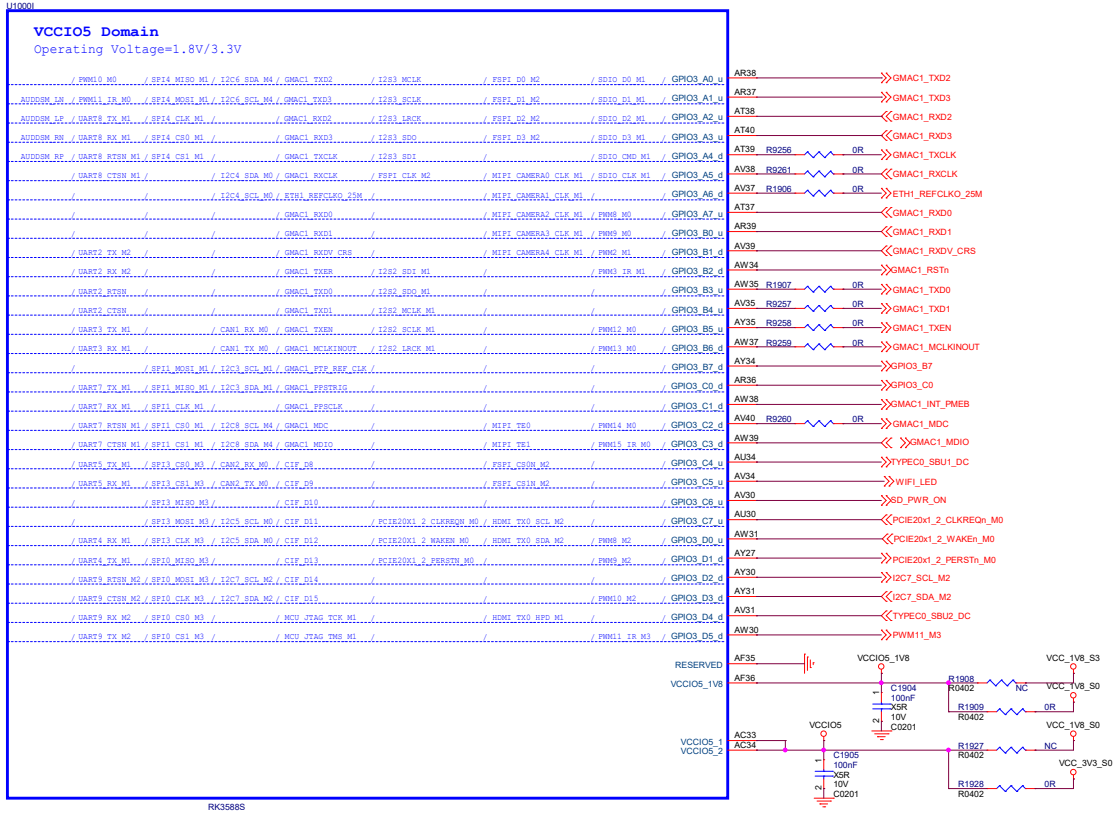


RK3588S(VCCIO6 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(VCCIO5 Domain)



Size	Title: CM5	REV
A2	Page Name: 18_RK3588S GPIO	X2.1
Date: Wednesday, October 11, 2023	Sheet 17 of 19	

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1
PMIC_PWR_CTRL2_SOC
PMIC_INT_L
PWRON_L
PMIC_RESET_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI

VCC_SYSIN
ED2200
AZ5825-01F
ESD0402

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

PMIC_PWR_CTRL2_SOC — R2242 R0402 100K — PMIC_PWR_CTRL2
3.3V
R2244 120K
1.8V

PMIC RK806-1 BUCK

U2200A

VDD_DDR_S0 — Default:0.85V Low frequency: 0.85V-->0.75V — C2200 22uF X5R 10V C0603 — L2200 0.47uH IND_201610 — PMIC_SW5 — BUCK5 2.5A — VOUT5 — FB5 (FB=0.5V)
C2202 22uF X5R 10V C0603 — C2203 22uF X5R 10V C0603 — R2200 100R 5% R0402 — C9922 1uF X5R 10V C0402
Feedback from RK3588S

VCC_SYSIN — C2201 22uF 10V X5R C0603 — VCC1_1 VCC1_2 — SW1_1 SW1_2 — BUCK1 6.5A — VOUT1 — PMIC_SW1 — L2201 0.24uH IND_322512 — PMIC_VOUT1 — VDD_GPU_S0
C2209 1uF X5R 10V C0402 — R2208 100R 5% R0402 — C2210 47uF X5R 6.3V C0805 — C2205 47uF X5R 6.3V C0805 — C2280 22uF X5R 10V C0603
Feedback from RK3588S
(FB=0.5V) FB1

VDD2_DDR_S3 — C2213 22uF 10V X5R C0603 — VCC2_1 VCC2_2 — SW2_1 SW2_2 — BUCK2 5A — VOUT2 — PMIC_SW2 — L2203 0.24uH IND_322512 — PMIC_VOUT2 — VDD_CPU_LIT_S0
C2214 22uF X5R 10V C0603 — C2215 22uF X5R 10V C0603 — C2216 100pF C0G 50V C0402 — L2202 0.47uH IND_201610 — PMIC_SW6 — BUCK6 2.5A — VOUT6 — PMIC_VOUT6 — R2218 120K 1% R0402 — PMIC_FB6 — FB6 (FB=0.5V)
C2221 1uF X5R 10V C0402 — R2219 100R 5% R0402 — C2217 22uF X5R 10V C0603 — C2218 22uF X5R 10V C0603 — C2281 22uF X5R 10V C0603
Feedback from RK3588S
(FB=0.5V) FB2
R2227 100K 1% R0402

LPDDR4/4x=1.1V	120K	
LPDDR5=1.05V	110K	

VDDQ_DDR_S0 — C2225 10uF X5R 10V C0603 — VCC_SYSIN — VCC9 — SW9 — BUCK9 2.5A — VOUT9 — PMIC_SW9 — L2204 0.47uH IND_201610 — PMIC_VOUT9 — R2236 20K 1% R0402 — PMIC_FB9 — FB9 (FB=0.5V)
C2228 22uF X5R 10V C0603 — C2227 22uF X5R 10V C0603 — C2229 100pF C0G 50V C0402 — R2241 100K 1% R0402

VCC_SYSIN — C2226 22uF 10V X5R C0603 — VCC3 — SW3 — BUCK3 5A — VOUT3 — PMIC_SW3 — L2205 0.24uH IND_322512 — VDD_LOGIC_S0
C2230 1uF X5R 10V C0402 — R2238 100R 5% R0402 — C2231 22uF X5R 10V C0603 — C2232 22uF X5R 10V C0603 — C2282 22uF X5R 10V C0603
Feedback from RK3588S

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VCC_SYSIN — C2235 10uF X5R 10V C0603 — VCC8 — SW8 — BUCK8 2.5A — VOUT8 — PMIC_SW8 — L2206 0.47uH IND_201610 — PMIC_VOUT8
VCC_3V3_S3 — C2238 22uF X5R 10V C0603 — C2239 22uF X5R 10V C0603

VCC_SYSIN — C2236 22uF 10V X5R C0603 — VCC4 — SW4 — BUCK4 5A — VOUT4 — PMIC_SW4 — L2207 0.24uH IND_322512 — VDD_VDENC_S0
C2291 1uF X5R 10V C0402 — R2209 100R 5% R0402 — C2240 22uF X5R 10V C0603 — C2237 22uF X5R 10V C0603 — C2283 22uF X5R 10V C0603
Feedback from RK3588
VDD_VDENC_S0

VCC1V8_PMU_DDR_S3 — R95378 NC — R0603 — VCC_1V8_S3_PLDO6
Default:1.8V
R2211 0R R0603

VCC_SYSIN — C2241 22uF X5R 10V C0603 — VCC10 — SW10 — BUCK10 2.5A — VOUT10 — PMIC_SW10 — L2208 0.47uH IND_201610 — PMIC_VOUT10
VCC_1V8_S3 — C2242 22uF X5R 10V C0603 — C2243 22uF X5R 10V C0603

VCC_SYSIN — VCC7 — SW7 — BUCK7 2.5A — VOUT7 — PMIC_SW7 — L2209 0.47uH IND_201610 — PMIC_VOUT7 — VCC_2V0_PLDO_S3
C2244 22uF X5R 10V C0603 — C2245 22uF X5R 10V C0603

RK806-1

PMIC RK806-1 Managerment

VCC_1V8_S3_PLDO6 — C2248 1uF 10V X5R C0402 — U2200C — VCCIO
VCC_SYSIN — R95029 0R R0402 — VCCA — C2254 1uF C0402
C90408 4.7uF
1<VDC<VCCA
R95379 200K — R2265 200K — C2260 1nF C0402 — D2600 B5819WS — C2261 100nF X5R 16V C0402
PWRON_L

VCCIO: (IIC/SPI)CS — PMIC_SPI_CS; (SDA)MOSI — PMIC_SPI_MOSI; (SCL)CLK — PMIC_SPI_CLK; (PWRCTRL3)SO; PWRCTRL2 — PMIC_PWR_CTRL2; PWRCTRL1 — SLEEP1_RESET1_DEVOFF1_VSEL1
R2258 100K R0402
VCC_1V8_S3 — R2261 10K R0402 — R2263 10K R0402
VCCA: SYNC_CLK; SYNC; VDC; PWRON
(M/S)EXT_EN — PMIC_EXT_EN_OUT; INT — PMIC_INT_L; RESETB — PMIC_RESET_L; ePAD
C2262 100nF X5R 16V C0402
RK806-1

RK3588S nPOR — TSADC_SHUT
RK806-1 RESETB
Reset Key

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

VCC_2V0_PLDO_S3 — C2247 1uF X5R 10V C0402 — VCC11 — PLDO1 0.5A — VCC_1V8_S0 — C2246 1uF 2 10V C0402 X5R — Default:1.8V
PLDO2 0.3A — VCCA_1V8_S0 — C2249 1uF 2 10V C0402 X5R — Default:1.8V
PLDO3 0.3A — VDDA_1V2_S0 — C2250 1uF 2 10V C0402 X5R — Default:1.2V
VCC_SYSIN — C2252 1uF X5R 10V C0402 — VCC12 — PLDO4 0.5A — VCCA_3V3_S0 — C2251 1uF 2 10V C0402 X5R — Default:3.3V
PLDO5 0.3A — VCCIO_SD_S0 — C2253 1uF 2 10V C0402 X5R — Default:3.3V
PLDO

VCCA_1V8_S0 — R2274 0R R0402 — AVDD1V8_DDR_PLL_S0 — C2290 1uF X5R 10V C0402

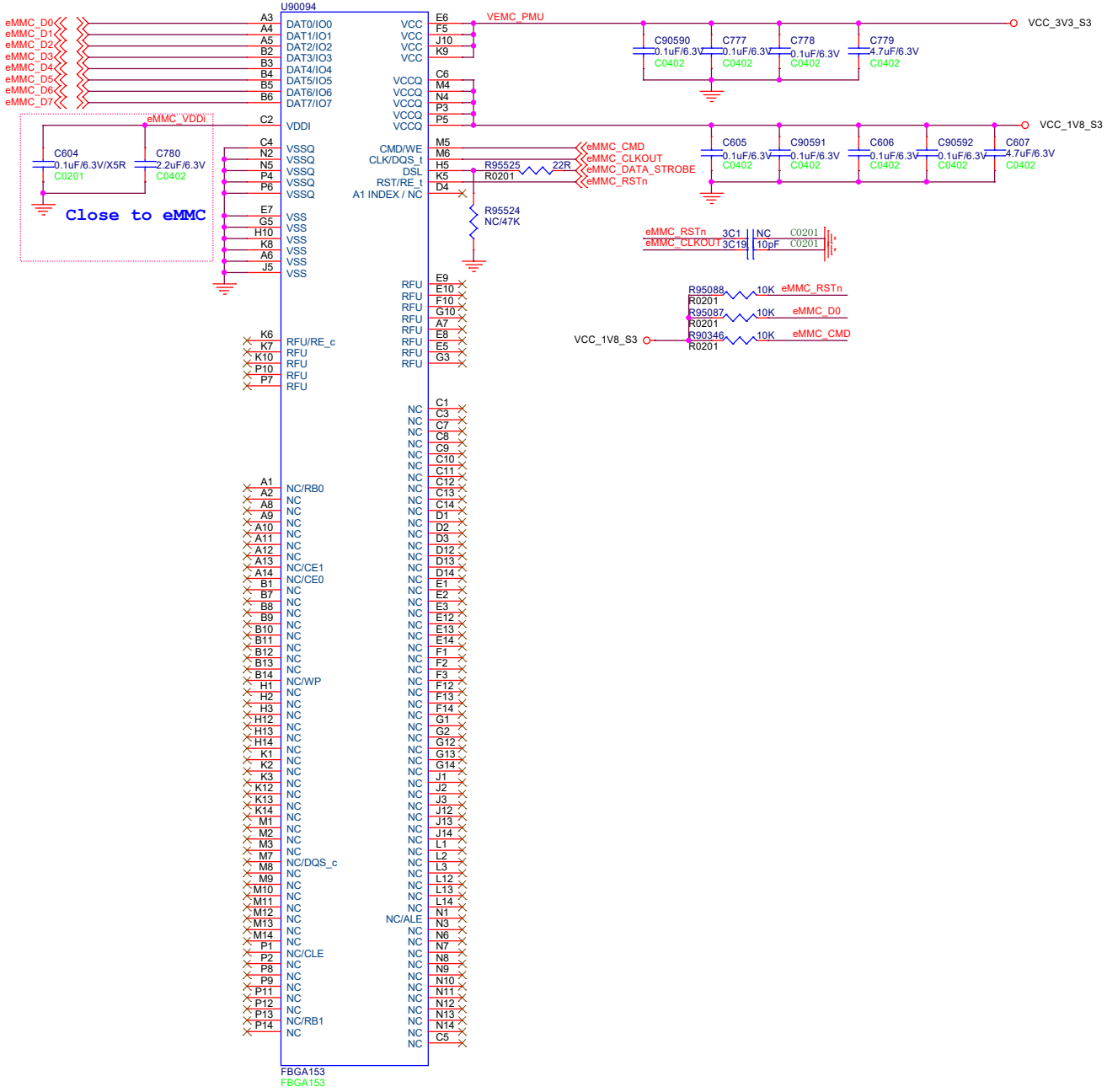
VCC_1V1_NLDO_S3 — C2257 1uF X5R 10V C0402 — VCC13 — NLDO1 0.3A — VDD_0V75_S3 — C2255 2.2uF 2 6.3V C0402 X5R — Default:0.75V
NLDO2 0.3A — VDDA_DDR_PLL_S0 — C2258 2.2uF 2 6.3V C0402 X5R — Default:0.85V; Low frequency:0.85V-->0.75V
NLDO3 0.5A — VDDA_0V75_S0 — C2259 2.2uF 2 6.3V C0402 X5R — Default:0.75V
VCC_1V1_NLDO_S3 — C2264 1uF X5R 10V C0402 — VCC14 — NLDO4 0.5A — VDDA_0V85_S0 — C2263 2.2uF 2 6.3V C0402 X5R — Default:0.85V
NLDO5 0.3A — HDMI_VDDA0V85_S0 — C2265 2.2uF 2 6.3V C0402 X5R — Default:0.75V Reserved
NLDO

RK806-1

radxa

Size	Title:	REV
C	CM5	X2.1
Page Name:	18_Power_PMIC_RK806_1	
Date: Wednesday, October 11, 2023	Sheet 18 of 19	

eMMC



Size	Title: CM5		REV
A3	Page Name: 19_eMMC		X2.1
Date: Wednesday, October 11, 2023	Sheet 19 of 19		