Key Features

Processor

- Dual-core Arm® Cortex®-A76 and Hexa-core Arm® Cortex®-A55, up to 2.0 GHz
- Single-core RISC-V E902, up to 200 MHz
- IMG BXM-4-64 MC1
- NPU, up to 3 TOPs

Memory

- External 32-bit LPDDR4/LPDDR4x/LPDDR5, up to 16 GB
- 192 KB SRAM +512 KB shared SRAM
- SD 2.0/3.0, eMMC 5.0/5.1
- 1x 2-lane UFS3.0
- 1x 8-bit RAW NAND Flash
- 1x SPI Flash, supporting up to Octal-I/O SPI mode and DTR mode

Graphics & Display

- DE, supporting independent/synchronous output on the dual display
  - Main display: up to 4K@60fps VI/UI output, 4K VI input or 4K UI input
  - Secondary display: up to 2K VI/UI input
- DI, up to 1920x1080@60fps
- G2D, up to 7680x7680 pixel layer size
- E-ink, up to 2560x1650@106fps

Image

- ISP
  - Supports multiple sensors input
  - Performance of one sensor: linear 8M@60fps online, 2f-wdr 8M@30fps online, linear 24M@25fps offline, and 2f-wdr 8M@30fps offline
  - Supports multiple data stream out
  - Supports ISP adjustment on the PC (online/offline/remote debugging)
- ENCPP, up to 8K x 8K resolution

Video Engine

- Video decoding
  - H.265 MP, VP9, AVS2, supporting up to 8K@24fps
  - H.264 BL/MP/HP, supporting up to 4K@30fps
  - H.263 BP, MPEG-1/2/4, AVS+/AVS, VP8, MJPEG, XVID, WMV9, VC-1, Sorenson Spark, supporting up to 1080P@60fps
- Video encoding
  - H.265/H.264, supporting up to 4K@30fps
  - MJPEG encoder up to 4K@15fps
- Image encoding & decoding
  - JPEG encoder up to 4K@15fps
  - JPEG decoder up to 1080P@60fps

Video Output

- 1x RGB, up to 1920x1080@60fps
- 1x dual-link LVDS, up to 1920x1080@60fps
- 2x 4-lane MIPI DSI output
  - Up to 2K@120fps for single link, and 2.5K@60fps or 4K@45fps for dual link
  - MIPI DSI0 supports DSC1.1, up to 2000x1200@120fps
- 1x eDP1.4b/DP1.4
  - Up to 4K@60fps
  - Supports HDCP1.4 and HDCP2.3
- 1x HDMI 2.0b TX, supporting HDMI1.4/HDMI2.0
  - Up to 4K@60fps
  - Supports HDCP1.4 and HDCP2.2

Video Input

- 2x Parallel CSI
  - 8/10/12/16-bit data width
  - Up to 4*1280x720@30fps for BT.656 and up to 4*1920x1080@30fps for BT.1120
- 3x MIPI CSI
  - 4 + 4 + 2-lane MIPI CSI, up to 2.0 Gbit/s per lane
  - Up to 6-channel BK output online

Audio

- 5x I2S

- 1x 8-channel DMIC, up to 8 KHz-48 KHz sampling rate
- 1x OWA input and 1x OWA output

Peripheral Interfaces

- 1x PCIe3.0 DM, supporting RC and DM
- 1x USB3.1 GEN2 DRD, forming a combo PHY with eDP1.4b/DP1.4 or PCIe3.0 DM
- 1x USB2.0 DRD
- 1x USB2.0 Host
- 1x SDIO3.0
- 1x GMAC
- 3x 10-channel PWM
- 5x SPI
- 9x UART
- 16x TWI
- 1x 7-channel GPADC
- 1x 1-channel LRADC
- 1x LEDC
- 2x IR_RX
- 1x IR_TX

Security

- AES/DES/3DES/XTS/SM4 symmetrical algorithm
- MD5/SHA/HMAC/SM3 hash algorithm
- RSA/ECC/SM2 asymmetrical algorithm
- PRNG/TRNG random bit generate algorithm
- Supports secure boot
- Supports secure memory isolation

Package

- ED-FCCSP 570 balls
- Body size: 15 mm x 15 mm size
- Maximum height: 0.951 mm
- Ball pitch: 0.5 mm & 0.4 mm mixed
- Ball size: 0.3 mm

NOTE

Some modules and specifications shown in the document are not offered for all orderable devices, please refer to Table 2-1 for details.

Revision History

Revision	Date	Author	Description
0.90	October 25, 2024	KPA0570	Initial Version Release
0.91	December 6, 2024	KPA0570	**Chapter 2 Ordering Information** Update Table 2-1 Ordering Information **Chapter 3 Features** Update the features of DE and DI in section 3.4.1 and 3.4.2 **Chapter 5 Electrical Characteristics** 1. Update Table 5-2 Recommended Operating Conditions 2. Add section 5.9.5 MIPI CSI Interface Timing **Chapter 6 Temperature and Thermal Characteristics** Add the A733MX-1XX Package Thermal Characteristics **Chapter 7 Pin Assignment** 1. Add the pin numbers of inner circles in Figure 7-1 Pin Map 2. Add the A733MX-1XX Package Dimension in section 7.1.2 Package Dimension **Chapter 10 Part Marking** Add the part marking of A733MX-1XX
0.92	February 18, 2025	AWA1896	1. Modify package type from FCCSP to ED-FCCSP. 2. Add operating frequency for RISC-V E902 **Chapter 2 Ordering Information** Update Table 2-1 Ordering Information **Chapter 5 Electrical Characteristics** Update note3-6 for Table 5-1 Absolute Maximum Ratings.

Revision	Date	Author	Description
0.93	June 3, 2025	AWA1896	**Chapter 4 Pin Description** Update section 4.1 Pin Characteristics. **Chapter 5 Electrical Characteristics** 1. Update section 5.9.2 SMHC Interface Timing 2. Update section 5.9.8 SPI Interface Timing 3. Update section 5.9.12 TWI Interface Timing

Content

Figures

Tables

About This Document

Purpose and Target Readers

This document details the features, logical structures, functional description, programming guidelines, and related registers of each module about the SoC. A basic knowledge of digital circuits, logical circuits, SoCs, and so on is necessary to use this manual. Particular attention should be paid to the cautions and notes within the body of the text.

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

The A733 family features high-performance platform processors targeted for mid-to-high-end tablets and interactive display applications. It can also be applied in tablet PCs and Arm® PCs.

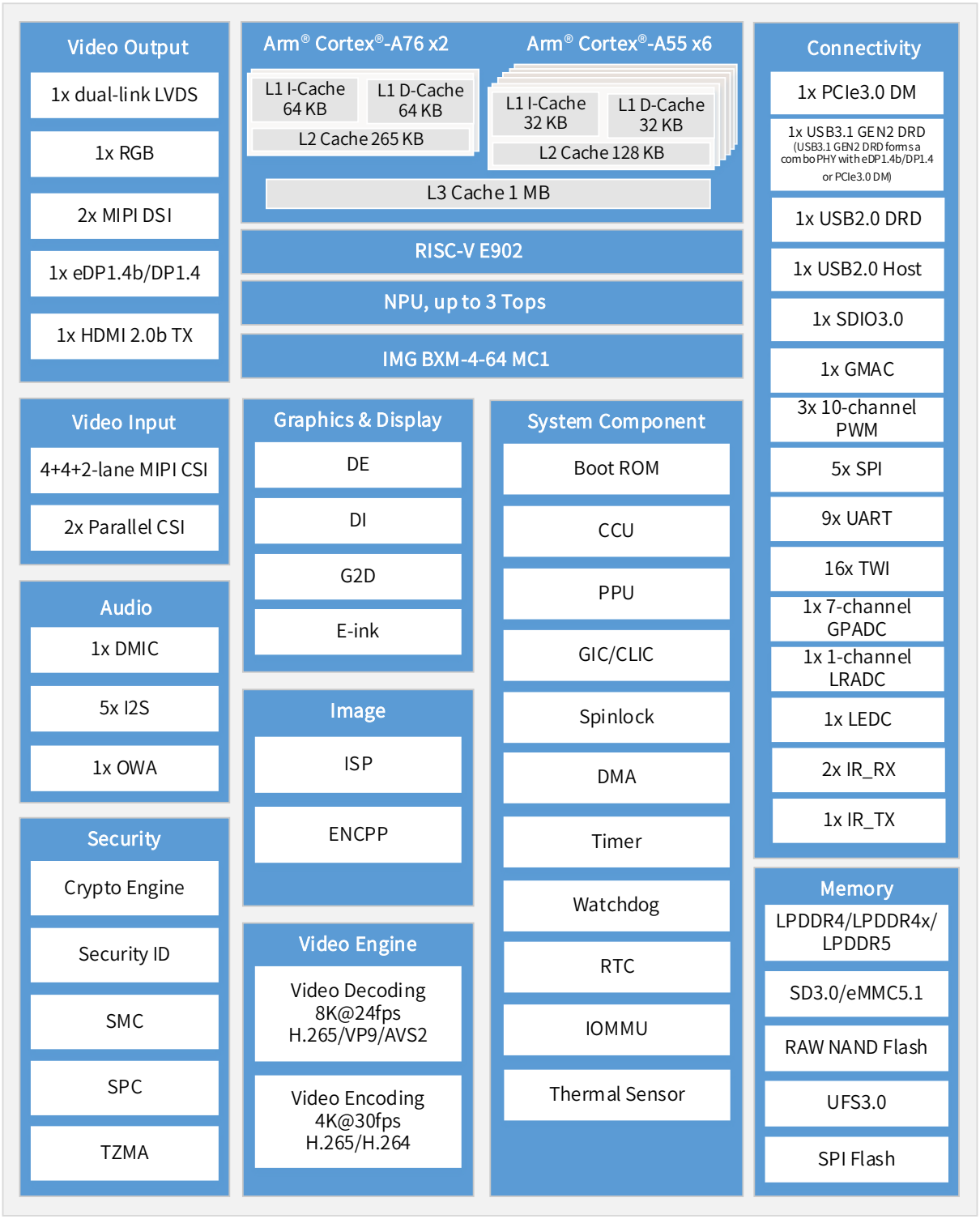
It integrates dual-core Arm® Cortex®-A76+hexa-core Arm® Cortex®-A55, BXM-4-64 MC1, 3 Tops NPU, LPDDR4/LPDDR4x/LPDDR5 to ensure rapid response and smooth operation for daily applications like online video, web browsing, 3D games, and so on.

It supports rich peripheral interfaces including high-speed interfaces such as PCIe3.0 DM, USB3.1 GEN2 DRD, GMAC, video input interfaces such as MIPI CSI and Parallel CSI, and video output interfaces such as HDMI, RGB, LVDS, MIPI-DSI, eDP1.4b/DP1.4, and E-ink, greatly facilitating product expansion.

It supports independent/synchronous output on dual display, H.265/VP9/AVS2 video decoding up to 8K@24fps, H.265/H.264 video encoding up to 4K@30fps, and ISP Allwinner SmartColor5.0 display enhancement technology to provide excellent video experience for users. Besides, the digital audio interfaces like I2S, DMIC, and OWA enable this chip family to meet the requirements of mainstream audio recognition solutions.

The following figure shows the system block diagram for the device.

Figure 1-1 System Block Diagram



2 Ordering Information

The following table provides the differences of orderable device(s) covered by this document.

Table 2-1 Ordering Information

Devices / Features	A733MX-HN3	A733MX-N3X	A733MX-1XX
Arm® CPU	2xA76+6xA55, up to 2 GHz		
RISC-V CPU	Single E902, up to 200 MHz		
NPU	Support	Support	Not support
HDMI2.0	Support	Not support	Not support
BK	6 channel	6 channel	4 channel
Package	ED-FCCSP 570 balls, 15 mm x 15 mm		

NOTE

The terms “A733” and “A733 family” in the document indicate all the orderable devices listed in Table 2-1 .

3 Features

3.1 Processors

- DynamIQ big.LITTLE Architecture Arm® CPU, up to 2.0 GHz
  - Dual-core Arm® Cortex®-A76, with 64 KB L1 I-cache, 64 KB L1 D-cache, and 256 KB L2 cache per core
  - Hexa-core Arm® Cortex®-A55, with 32 KB L1 I-cache, 32 KB L1 D-cache, and 128 KB L2 cache per core
  - Shared 1 MB L3 cache
- RISC-V E902 CPU, up to 200 MHz
- IMG BXM-4-64 MC1
- NPU, up to 3 TOPS

3.2 Memory & Storage

3.2.1 BROM

- On-chip memory
- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - RAW NAND Flash
  - UFS
  - SPI NOR Flash (Quad Mode and Single Mode)
  - SPI NAND Flash
- Supports mandatory upgrade process through USB or SD card
- Supports GPADC pin and eFuse module to select the boot media type
- Supports normal booting and secure booting

3.2.2 DRAM

- Supports external 32-bit LPDDR4/LPDDR4x/LPDDR5, up to 16 GB
- LPDDR4/LPDDR4x clock frequency up to 2133 MHz
- LPDDR5 clock frequency up to 2400 MHz

3.2.3 SMHC

- Four SD/MMC Host Controller (SMHC) interfaces
  - SMHC0 controls the devices that comply with the protocol Secure Digital Memory (SD3.0)

- SMHC1 controls the devices that comply with the protocol Secure Digital I/O (SDIO3.0)
- SMHC2/3 control the devices that comply with the protocol Multimedia Card (eMMC5.1)

- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 and the SMHC3 support the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports HS400 mode and HS200 mode
  - Maximum performance:
    - SDR mode 200 MHz@1.8V IO pad
    - DDR mode 200 MHz@1.8V IO pad
    - SDR mode 50 MHz@3.3V IO pad
    - DDR mode 50 MHz@3.3V IO pad
- Supports block size of 1 to 65535 bytes
- Internal 1024-Byte RX FIFO and 1024-Byte TX FIFO for data transfer
- Supports hardware CRC generation and error detection

3.2.4 UFSHC

- Supports the following features of UFS3.0
  - Supports PA_INIT error codes
  - Supports QOS indicators of TX, RX and PA_INIT
- Supports all the features of UniPro1.8 and MPHY4.1, including:
  - Supports QOS indicators
- Supports M-PHY rate mode
  - High speed: Gear 1/2/3/4 (Rate A or B)
  - Low speed: PWM Gear 1/2/3/4

3.2.5 RAW NAND Flash

- 1K/2K/4K/8K/16K/32K bytes per page
- Up to 8-bit data bus width
- Supports SLC/MLC NAND and EF-NAND memory
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 Raw NAND flash
  - SDR: Maximum IO rate up to 50 MHz
  - ONFI DDR1.0 and Toggle DDR1.0: Maximum IO rate up to 100 MHz
  - ONFI DDR2.0 and Toggle DDR2.0: Maximum IO rate up to 150 MHz

3.2.6 SPI Flash

- The SPI Flash is typically designed for higher-speed Flash devices and only works in master mode
- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports executing codes from FLASH memory in prefetch mode, which significantly reduces read time.
- Software Write Protection
  - Write protect all/portion of memory via software
  - Top/Bottom Block protection
- High-speed Clock Frequency
  - 150 MHz for STR Mode
  - 100 MHz for DTR Mode

3.3 Image

3.3.1 ISP

- Supports multiple sensors (up to 4) input
- Supports raw8/10/12/14/16
- Maximum resolution:
  - online: 3264x4224
  - offline: 5874x4224
- Performance of one sensor:
  - online: 8M@60fps (linear), 8M@30fps (2f-wdr)
  - offline: 24M@25fps (linear), 8M@30fps (2f-wdr)
- Supports multiple data streams (up to 16) output
  - Support YUV422/YUV420/RGB888/RGB565 output
  - Support graphics mirror and flip
  - Support 1/16~1x scaler down
  - Support rectangle bounding boxes
- Supports ISP adjustment tool on the PC (online/offline/remote debugging)
- Supports Algorithm Features:
  - Crop
  - 2F-WDR
  - Dynamic Range Compression (DRC)

- Local Tone Mapping
- Black Level Correction
- Digital Gain
- White Balance
- Len Shading Correction (LSC)
- Gamma Correction
- Defect Pixel Correction (DPC)
- Cross Talk Correction (CTC)
- Chromatic Aberration Correction (CAC)
- Noise Reduction (2D/3D)
- Bayer Interpolation
- Sharpness
- Color Enhancement (3D-LUT)
- Adjustable 3A functions: Automatic White Balance (AWB), Automatic Exposure (AE), and Automatic Focus (AF)
- Anti-flick Detection Statistics
- Histogram Statistics

3.3.2 ENCPP

- Input data format: 8-bit image, YUV420/YUV422/ARGB8888
- Input resolution
  - Minimum: 64 x 64
  - Maximum: 8192 x8192
  - 16x-aligned width and 16x-aligned height
- Output resolution
  - Minimum: 64 x 64
  - Maximum: 8192 x 8192
  - 16x-aligned width
- Rotation of 90/180/270 degrees clockwise and horizontal flip
- Watermark images overlaying
  - Four optional adaptive color inversion modes
  - Overlaying of maximum 64 watermark images
  - 16x-aligned width and 16x-aligned height
- Maximum unlimited 8x horizontal and vertical zoom-out
- Scaled image write back
  - Image format: NV12@8bits
  - Single entire image or multiple partial images
  - 1/(2^n) scaling down (n=1,2, or 3)
  - 16x-aligned width and 16x-aligned height

3.4 Display & Graphics

3.4.1 DE

- Supports output size up to 4096x4096.
- Supports up to 7 alpha blending channels and 2 display out.
- Supports four overlay layers in each channel, and has an independent scaler.
- Supports potter-duff compatible blending operation.
- VCH0 support AFBD & TFBD, VCH1/UCH0~1 support TFBD, VCH2 support restricted 2K AFBD.
- Supports input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/ YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565.
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- Supports 10-bit processing path for HDR video.
- Supports SDR/HDR10/Hybrid-log gamma EOTF and color space conversion.
- Supports AWonder1.1 for excellent display experience.
  - Adaptive de-noising for compression noise or mosquito noise for yuv420/422 input.
  - Adaptive edge-directive scaler.
  - Adaptive local dynamic contrast enhancement.
  - Adaptive detail/edge enhancement.
  - Adaptive color enhancement (Blue-stretch, Green-stretch and fresh tone correction) and
  - skin-tone protection.
  - 17x17x17 programmable LUT for display0.
  - Adaptive de-banding for color banding removal.
  - Hue gain, Saturation gain, and Value gain controlled.
  - Fully programmable color matrix.
  - Dynamic gamma.
  - Color temperature tuning / Auto white balance
  - Global dimming (Up to 2560x2048 for display0, 2048x2048 for display1)
- Supports write back for high efficient dual display and miracast.
- Supports output format YUV444/YUV422/YUV420/RGB444 for 10/8bit.
- Supports Register Configuration Queue for register update function.
- Supports 1/2/4 ppc (pix per cycle) output.
- Supports offline composition mode to increase bandwidth utilization.

3.4.2 DI

- Supports off-line processing mode only
- Supports 8bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined input data format

- Supports 8bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined output data format for DIT, and YV12/planar YUV422 output data format for TNR.
- Supports video resolution from 32x32 to 2048x1280 pixel
- Supports weave/pixel-motion-adaptive de-interlace method
- Supports horizontal motion compensate de-interlace
- Supports Field-Based Motion Detection
- Supports Temporal Noise Reduction function
- Supports Film Mode Detection with Video-On-Film Detection
- Supports interlace detection (ITD)
- Module clock 500MHz for 1080P@60Hz YUV420, 550MHz for 1080P@60Hz YUV422 with all functions enable

3.4.3 G2D

- Supports mixer layer size up to 7680x7680 pixels, and rotate size up to 4096x4096 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats including YUV420, YUV422, and YUV411, and multiple pixel formats (8/16/24/32-bit graphics layer)
- Supports memory scan order option
- Supports converting in any format
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter or 32-phase 4-tap vertical anti-alias filter.
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit.
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

3.4.4 E-ink

- Up to 2560x1650@106fps resolution
- Supports dual scan display
- Supports up to 5-bit screen with 32 levels of grayscale refresh
- Supports overlap refresh in arbitrary shapes
- Supports collision detection and refresh in arbitrary shapes
- Supports three kinds of dither including Floyd-Steinberg, Atkinson, and Ordered dither
- Supports auto mode selection

3.5 Video Engine

3.5.1 Video Decoding

- H.265 MP@L5.2, up to 8K@24fps
- VP9 Profile-2, up to 8K@24fps
- AVS2, up to 8K@24fps
- H.264 BP/MP/HP@L5.1, up to 4K@30fps
- VP8, up to 1080P@60fps
- H.263 BP, up to 1080P@60fps
- MPEG-4 SP/ASP L5.0, up to 1080P@60fps
- MPEG-2 MP/HL, up to 1080P@60fps
- MPEG-1 MP/HL, up to 1080P@60fps
- AVS/AVS+/MJPEG/JPEG/XVID/WMV9/VC-1/Sorenson Spark, up to 1080P@60fps

3.5.2 Video Encoding

- H.265 MP@L5.0, up to 4K@30fps
- H.264 BP/MP/HP@L4.2, up to 4K@30fps
- MJPEG/JPEG baseline, up to 4K@15fps
- Supports encoder pre-processing

3.6 Video Output Interfaces

3.6.1 RGB

- One RGB interface in CPUX domain
- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports BT.656 interface for NTSC and PAL

3.6.2 LVDS

- One dual-link LVDS interface in CPUX domain, up to 1920x1080@60fps

3.6.3 MIPI DSI

- Two MIPI DSI interfaces in CPUX domain: DSI0 and DSI1
- Compliant with MIPI DSI specification V1.02 and MIPI D-PHY specification V1.2
- Up to 4 lanes
- Single lane supports up to 2K@120fps resolution and dual lane support up to 2.5K@60fps or 4K@45fps

- DSI0 supports DSC1.1, up to 2000x1200@120fps

3.6.4 eDP1.4b/DP1.4

- One eDP1.4b/DP1.4 TX interface in CPUX domain, up to 4K@60fps output
- Supports 1-lane, 2-lane, or 4-lane transmission, up to 5.4 Gbps per lane
- Supports video formats including RGB, YCbCr4:4:4, YCbCr4:2:2, and YCbCr4:2:0
- Supports 6/8/10-bit color depth
- Supports HDCP1.4 and HDCP2.3
- Supports timing standards like VESA DMT and CVT
- Supports 8-lane I2S audio transmission, up to 192 KHz sampling rate

3.6.5 HDMI

- One HDMI2.0 TX interface in CPUX domain, supporting HDMI1.4/HDMI2.0
- Up to 4K@60fps output
- Supports several data formats including RGB888, YUV444, YUV422, and YUV420, and 8/10bit data width
- Supports HDCP1.4 and HDCP2.2
- Supports 8-channel I2S audio transmission, up to 192 KHz sampling rate

3.7 Video Input Interfaces

3.7.1 MIPI CSI

- 4+4+2-lane MIPI Interfaces in CPUX domain
  - Supports MIPI CSI2 V1.1
  - Supports MIPI DPHY V1.2
  - Supports 2 Gbps/lane
- Supports Crop Function
- Supports Frame Rate Down
- Maximum resolution: 3264x4224 in ISP online mode and 5664x4248 in ISP offline mode
- Supports sensor frame synchronization
- Up to 6-lane BK output
  - BK0/1 supports maximum 20M@30fps or 24M@25fps
  - BK2/3 supports maximum 2.5K@60fps
  - BK4/5 supports maximum 1080P@30fps
- BK0/1/2/3 supports 4-lane time division multiplexing
- Supports conversion from YUV422 to YUV420, YUV422 to YUV400, and YUV420 to YUV400
- Supports horizontal and vertical flip for YUV422/YUV420/RAW format

3.7.2 Parallel CSI

- Two parallel CSI interfaces in CPUX domain
- Supports 8/10/12/16-bit width
- Supports BT.656, BT.601, BT.1120, and Digital Camera (DC) protocol
- Supports ITU-R BT.656 up to 4*720P@30fps
- Supports ITU-R BT.1120 up to 4*1080P@30fps
- Supports BT.656 2/4-channel time-multiplexed format
- Dual Data Rate (DDR) sample mode with maximum pixel clock of 148.5MHz

3.8 Audio Interfaces

3.8.1 I2S

- Five I2S interfaces in CPUX domain
- Supports Left-justified, Right-justified, PCM mode, and TDM format
- Supports master/slave mode
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO,64 depth x 32-bit width RXFIFO

3.8.2 DMIC

- One DMIC interface in CPUX domain
- Supports maximum 8 channels
- Supports sample rate from 8 kHz to 48 kHz

3.8.3 OWA

- One OWA TX and one OWA RX in CPUX domain
- Compatible with IEC-60958 and IEC-61937
- Supports 44.1 kHz, 48 kHz, 96 kHz, 192 kHz, and 384 kHz sampling rate
- Supports 16-/20-/24-bit data width
- Transmit and Receive data FIFOs
  - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds

3.9 System Components

3.9.1 CCU

- Three clock sources: an on-chip 16 MHz RC oscillator, an external 26 MHz DCXO, and an external 32.768 kHz oscillator
- Supports clock configuration, clock generation, gating, reset for modules

3.9.2 PRCM

- AHBS/APBS clock configuration
- Bus gating, bus reset, and module clock configuration in CPUS domain
- VDD-SYS and analog power control
- RAM/ROM configuration

3.9.3 PPU

- Supports multiple power management configurations for automatic clock gating control and power domain on/off control
- Supports 8 independent voltage domain
- Supports 22 independent power domain

3.9.4 DMA

- Two 16-channel DMAs
- Programmable 8-/16-/32-bit data width
- Programmable DMA burst length
- DMA channel supports pause, bmode, timeout, and IOspeed mode
- DRQ response supports waiting mode and handshake mode
- Supports reading and writing 64 DMA requests respectively
- Supports link transfer

3.9.5 MSGBOX

- Supports two CPUs to transmit information through one-way channels. Each CPU has a MSGBOX and can only read or write in one communication
  - CPUX_MSGBOX: CPUS write, CPUX read
  - CPUS_MSGBOX: CPUX write, CPUS read
- The channel between two CPUs has 4 channels, and the FIFO depth of each is 8x32 bits.

3.9.6 Spinlock

- Provides hardware synchronization mechanism in the multi-core system
- 32 lock units

- Two lock statues: locked and unlocked
- Lock time of the processor is predictable, which is less than 200 cycles

3.9.7 RTC

- Provides a 16-bit counter for counting day, a 5-bit counter for counting hour, a 6-bit counter for counting minute, a 6-bit counter for counting second
- Uses a 32.768 kHz low-frequency oscillator as the count clock
- 1 kHz Counting frequency
- Supports fanout function of internal 32K clock
- Supports timing alarm, and generating interrupts and waking up the external devices

3.9.8 Thermal Sensor

- Five thermal sensors, respectively distributed in A76 core, A56 core, GPU, NPU and DDR.
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports ±3°C error limit from 60 to 125°C, and ±5°C from -40 to 60°C

3.9.9 Timer

Timer 0

- Fourteen timer 0: 10 in CPUX domain, and 4 in CPUS domain
- Configurable counting clock: 32KHz, 24MHz, 16MHz, or 200MHz
- Programmable 56-bit down counter
- Two working modes: periodic mode and single count mode
- Generates an interrupt when the count value is decreased to 0

Timer 1

- Four timer 1 in CPUX domain
- Configurable counting clock: RTC_32K and DCXO
- Configurable 8 pre-scalers
- Programmable 32-bit down counter
- Two working modes: periodic mode and single count mode
- Generates an interrupt when the count value is decreased to 0

3.9.10 Watchdog Timer

- Two watchdog timers: 1 in CPUX domain, and 1 in CPUS domain.
- Supports 12 programmable initial values
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports restart timing by watchdog

3.10 Peripheral Interfaces

3.10.1 USB

USB3.1 GEN2 DRD

- One USB3.1 GEN2 DRD interface in CPUX domain, forming a combo PHY with eDP1.4b/DP1.4 or PCIe3.0 DM
- Complaint with USB 3.1 Gen2 protocol and XHCI1.2 protocol
- Supports using 1-lane USB3.1/4-lane eDP1.4b/DP1.4 COMBO TYPE-C PHY or 1-lane USB3.1/PCIe3.0 COMBO PHY
- Supports using the independent USB2.0 PHY
- Data transfer rates in host mode
  - Compliant with eXtensible Host Controller Interface (xHCI) specification, version 1.2
  - Super-Speed Plus (SSP, 10 Gbps)
  - Super-Speed (SS, 5 Gbps)
  - High-Speed (HS, 480 Mbps)
  - Full-Speed (FS, 12 Mbps)
- Data transfer rates in device mode
  - Speed Plus (SSP, 10 Gbps)
  - Super-Speed (SS, 5 Gbps)
  - High-Speed (HS, 480 Mbps)
  - Full-Speed (FS, 12 Mbps)
  - Supports up to 16 Endpoints IN (including control endpoint 0) and 16 Endpoints OUT (including control endpoint 0)
  - 15 pairs of bulk/interrupt/isochronous endpoints (EP 1-15) share 21 KB TX FIFO, 8K RX FITO for synchronous transmission, and 8K RX FIFO for cyclic transmission. 1 pair of control endpoint (EP 0) uses 64 B RX/TX FIFO.

USB2.0 DRD

- One USB2.0 DRD interface in CPUX domain
- Compliant with USB2.0 Specification
- Data transfer rates in host mode
  - Complaint with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Complaint with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - High-Speed (HS,480 Mbps)
  - Full-Speed (FS,12 Mbps)
  - Low-Speed (LS,1.5 Mbps)
  - only 1 USB Root Port shared between EHCI and OHCI
- Data transfer rates in device mode
  - High-Speed (HS,480 Mbps)
  - Full-Speed (FS,12 Mbps)

- bi-directional Endpoint0 for control transfer
- Supports up to 9 Endpoints IN (including control endpoint 0) and 9 Endpoints OUT (including control endpoint 0)
- Supports up to (8KB+64Bytes) FIFO for endpoints (Including EP0)
- Supports interface to an external Normal DMA controller for bulk/interrupt/isochronous endpoints (EP1-8)

USB2.0 Host

- One USB2.0 Host interface in CPUX domain
- Compliant with USB2.0 protocol, EHCI 1.0 protocol, and OHCI 1.0a protocol
- Supports industry-standard AMBA High-Performance Bus (AHB), fully compliant with the AMBA Specification, Revision 2.0.
- Data transfer rates
  - High-Speed (HS, 480 Mbps)
  - Full-Speed (FS, 12 Mbps)
  - Low-Speed (LS, 1.5 Mbps)

3.10.2 PCIe3.0 DM

- One PCIe3.0 interface in CPUX domain
- Compliant with PCIe3.0 protocol
- Supports 1-lane link width
- Supports dual mode (DM): RC and EP; 4 Functions in EP mode
- Supports the transfer rate of Gen1 (2.5 Gbps), Gen2 (5 Gbps), and Gen3 (8 Gbps)
- Supports using USB3.1/PCIe3.0 1-lane COMBO PHY
- Embedded DMA with Hardware Flow Control supports 4 write/read channels
- Supports maximum 512-byte payload size
- Internal Address Translation Unit supports 16 Inbound Address Translation regions and 16 Outbound Address Translation regions

3.10.3 GMAC

- One GMAC interface in CPUX domain for connecting external Ethernet PHY
- Compliant with IEEE 802.3-2015 standard
- Supports both full-duplex and half-duplex modes
- Full-duplex flow control
- Supports IEEE 1588-2008 for precision networked clock synchronization
- Supports Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports Source Address field, VLAN insertion or replacement, and Double VLAN
- Transmits TCP/IP checksum offload

- Supports 4KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets
- Supports 16 Descriptors Descriptor Pre-fetch cache for TX DMA and RX DMA
- Supports MDIO interface for PHY device configuration and management
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- Supports Power Management Module (PMT) with remote wake-up packet and magic packet processing options
- Supports Energy Efficient Ethernet (EEE)
- Supports RMII/RGMII PHY interface
- Supports 10/100/1000 Mbps data transfer rates

3.10.4 UART

- Nine UART controllers: Seven in CPUX domain, two in CPUS domain
- Compatible with industry-standard 16450/16550 UARTs
- Transmit and Receive data FIFOs
  - UART0, S_UART0-1: RX 64 byte, TX 64 byte
  - UART1-6: RX 256 byte, TX 256 byte
- Supports baud rate generator from APB bus clock
  - Up to 10 Mbps with 160 MHz APB clock (exclude S_UART0, S_UART1)
  - Up to 5 Mbps with 80 MHz APB clock (exclude S_UART0, S_UART1)
  - Up to 3.75 Mbps with 60 MHz APB clock (exclude S_UART0, S_UART1)
  - Up to 1.5 Mbps with 24 MHz APB clock
- 5 to 8 data bits for RS-232 format or 9 bits RS-485 format, and 1, 1.5 or 2 stop bits
- Supports even, odd, or no parity
- Supports TX/RX DMA slave controller interface
- Support Auto-Flow by using CTS & RTS (exclude UART0, S_UART0, S_UART1)

3.10.5 PWM

- Three PWM controllers: two in CPUX domain and one in CPUS domain. Each has 10 channels.
- Output frequency range: 0 to 24 MHz or 0 to 100 MHz
- Adjustable duty cycle: 0% -100%
- Minimum resolution: 1/65536
- Supports PWM group mode (4 groups), the starting phase of each channel in same group is configurable
- Supports 10-channel input waveform capture and period calculation
- Supports 5 pairs of complementary pair output

3.10.6 SPI

- Five SPI controllers: Four in CPUX domain, and one in CPUS domain
  - SPI0, SPI2, SPI3 and S_SPI0 support SPI mode

- SPI1 supports both SPI mode and DBI mode

SPI mode

- Supports multiple SPI modes
  - Master mode and Slave mode Standard SPI (4wire)
  - Master mode Dual-Output/Dual-Input SPI/ Dual I/O SPI
  - Master mode Quad-Output/Quad-Input SPI
  - Master mode 3wire SPI, with programmable serial data frame length: 1bit to 32bits
- Supports the Maximum clock frequency: 100MHz
- Supports TX/RX DMA Slave interface
- Transmits and receives data FIFO with 8-bit wide and 64-entry respectively
- Transmits data buffer with 8-bit wide and 4-entry
- Receives data buffer with 8-bit wide and 128-entry
- Supports four Data Sample Mode: Mode0, Mode1, Mode2 and Mode3
- Supports Control signal configuration
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI mode

- Supports DBI Type C 3 Line/4 Line Interface Mode and 2 Data Lane Interface Mode
- Supports data source from CPU or DMA
- Supports RGB111/444/565/666/888 video format
- Supports Maximum resolution RGB666 240*320 @30Hz with Single Data Lane
- Supports Maximum resolution RGB888, 320*480 @30Hz or 240*320 @60Hz with Dual Data Lane
- Supports Tearing Effect
- Supports software flexible control video frame rate

3.10.7 TWI

- Sixteen TWI controllers: Thirteen in CPUX domain and three in CPUS domain
- Supports 7-bit standard address and 10-bit extended address
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s)
- Supports general call and start byte
- Supports master mode or slave mode
- The features in master mode
  - Supports the bus arbitration in the case of multiple master devices
  - Supports clock synchronization and bit and byte waiting
  - Supports packet transmission and DMA
  - Supports DVFS request adjust voltage
- The features in slave mode

- Interrupt on address detection

3.10.8 GPADC

- One GPADC in CPUX domain with 7 pads: 4 for boot detection and 3 for analog voltage input detection
- 12-bit resolution
- Analog Input Range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports three operation modes:
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

3.10.9 LRADC

- One LRADC in CPUX domain with 1 channel for analog voltage input
- 6-bit resolution and maximum 2 kHz sampling rate
- Supports hold key and general key
- Supports normal, continue and single work mode
- Power supply voltage:1.8 V; power reference voltage:1.35 V.
- Voltage input range between 0 to 1.35 V

3.10.10 LEDC

- One LEDC in CPUX domain
- Supports a maximum of 1024 LEDs serial connection
- Configurable interval time between data packets and frame data
- Configurable RGB display mode supports RGB/RBG/GRB/GBR/BRG/BGR modes
- Configurable default level of non-data output
- Configurable LED output high/low level width and reset time
- LEDC data supports DMA configuration mode and CPU configuration mode

3.10.11IR_TX

- One IR_TX interface in CPUX domain
- Supports industry-standard AMBA Peripheral Bus (APB), which is fully compliant with the AMBA Specification, Revision 2.0
- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Supports Interrupt and DMA

- Supports DMA handshake and waiting mode
- Supports arbitrary wave generator

3.10.12IR_RX

- Two IR_RX interfaces: One in CPUX domain and one in CPUS domain
- Supports CIR remote control receiver
- Sample clock up to 1 MHz
- Supports 64-byte RX FIFO
- Programmable FIFO thresholds

3.11 Security

3.11.1 CE

- Symmetrical algorithms including AES, DES, 3DES, SM4, RC4.
- Hash algorithms
  - Supports MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Supports HMAC-SHA1, HMAC-SHA256
- Random bit generator algorithms
  - Support PRNG, 175 bits seed width, and output with multiple of 5 words
  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
  - Support TRNG single/double entropy source mode
  - Support TRNG healthy test
- Asymmetrical algorithms including up to 4096-bit RSA and 521-bit ECC public key algorithms and SM2 algorithms
- Supports keyladder to guarantee key secure

3.11.2 SID

- The SID is mainly used for one-time programming the eFuse on the chip
- 4 Kbits eFuse
- Supports secure and non-secure world in eFuse
- Backup eFuse information by using SID_SRAM
- Enable double-bit check by parameter definition
- Supports data scrambling
- Supports reading and writing protection
- 64-bit available secure OEM space and 160-bit available non-secure OEM space

3.11.3 SMC

- The SMC is always secure and can only be accessed by secure CPU

- Sets the secure area of DRAM

3.11.4 SPC

- The SPC is always secure and can only be accessed by secure CPU
- Sets the secure area of peripherals

3.11.5 TZMA

- The TZMA is always secure and can only be accessed by secure CPU
- Sets the secure area of SRAM

3.12 Package

ED-FCCSP 570 balls, 15 mm x 15 mm body size, 0.951 mm height (maximum), 0.5 mm & 0.4 mm mixed ball pitch, 0.3 mm ball size

4 Pin Description

4.1 Pin Characteristics

The following tables list the characteristics of the device pins from the following seven aspects.

[1] **Ball#**: Package ball numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground),

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pull-up

PD: Internal pull-down

PU/PD: Internal pull-up and pull-down

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

[8] **COMB0-PHY-SERDES:** It is the combo PHY of DP1.4b, eDP1.4, and USB3.1. USB3.1 interacts with external devices through COMB0-PHY-SERDES or COMB1-PHY-SERDES.

[9] **COMB1-PHY-SERDES:** It is the combo PHY of PCIe3.0 and USB3.1. USB3.1 interacts with external devices through COMB0-PHY-SERDES or COMB1-PHY-SERDES.

4.1.1 DRAM

Table 4-1 DRAM Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1AF10	SCA3-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT15	SCKN-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT14	SCKP-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE16	SCA5-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB16	SCA4-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF16	SCA2-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC16	SCA3-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE10	SCA2-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE14	SCA1-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC14	SCA0-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF12	SCA0-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC10	SCA5-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF14	SCS1-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB10	SCA4-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE12	SCA1-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT23	SCKP-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT22	SCKN-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT19	SATO	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB12	SDTO	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT21	SCS0-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT16	SCKE0-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU16	SCKE1-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT18	SCS1-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AU18	SCS0-B	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU24	SCKE0-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU21	SCKE1-A	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC12	SRST	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU33	WCK0N-A	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT33	WCK0P-A	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT31	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT32	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT34	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF22	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU31	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC20	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE22	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT35	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU36	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB20	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE24	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT28	WCK1N-A	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU28	WCK1P-A	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU27	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT27	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF20	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF18	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU25	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE18	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT25	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE20	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT29	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC18	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU30	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1AE6	WCK0P-B	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF6	WCK0N-B	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT11	SDQS2N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT10	SDQS2P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC8	SDQM2	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC6	SDQ23	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT9	SDQ22	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB8	SDQ21	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU9	SDQ20	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF8	SDQ19	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU12	SDQ18	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU13	SDQ17	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE8	SDQ16	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU6	WCK1P-B	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT6	WCK1N-B	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU7	SDQS3N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT7	SDQS3P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF2	SDQM3	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT3	SDQ31	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE2	SDQ30	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AU4	SDQ29	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT4	SDQ28	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AC4	SDQ27	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AB6	SDQ26	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AF4	SDQ25	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1AE4	SDQ24	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AT20	SZQ	AI	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
1W10	VCC-DRAM	P	N/A	N/A	N/A	N/A
1W11	VCC-DRAM	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1W15	VCC-DRAML	P	N/A	N/A	N/A	N/A
1Y14	VCC-DRAML	P	N/A	N/A	N/A	N/A
1V14	VCC-DRAML	P	N/A	N/A	N/A	N/A
1U13	VDD-DRAM	P	N/A	N/A	N/A	N/A
1V8	VDD-DRAM	P	N/A	N/A	N/A	N/A
1W17	VDD-DRAM	P	N/A	N/A	N/A	N/A
1W18	VDD-DRAM	P	N/A	N/A	N/A	N/A
1U8	VDD-DRAM	P	N/A	N/A	N/A	N/A
1V12	VDD18-DRAM	p	N/A	N/A	N/A	N/A

4.1.2 RTC

Table 4-2 RTC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
W37	X32KIN	AI	N/A	N/A	N/A	VCC-RTC
V37	X32KOUT	AO	N/A	N/A	N/A	VCC-RTC
U36	X32KFOUT	AO, OD	N/A	N/A	N/A	VCC-PM
1P25	VCC-RTC	P	N/A	N/A	N/A	N/A
1P23	RTC-VIO	P	N/A	N/A	N/A	N/A

4.1.3 PLL

Table 4-3 PLL Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1T26	PLLTEST	AO, OD	N/A	N/A	N/A	VCC-DCXO
1P26	CPU-PLLTEST	AO, OD	N/A	N/A	N/A	VCC-DCXO

4.1.4 DCXO

Table 4-4 DCXO Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
Y36	DXIN	AI	N/A	N/A	N/A	VCC-DCXO
AA36	DXOUT	AO	N/A	N/A	N/A	VCC-DCXO
AB37	REFCLK-OUT	AO	N/A	N/A	N/A	VCC-DCXO
1T24	WREQIN	I	N/A	N/A	N/A	VCC-IO
1T21	DXLDO-OUT	P	N/A	N/A	N/A	N/A
1T20	VCC-DCXO	P	N/A	N/A	N/A	N/A
1J21	VCC-DCXO1	P	N/A	N/A	N/A	N/A
1J11	VCC-DCXO2	P	N/A	N/A	N/A	N/A

4.1.5 GPIO Groups

4.1.5.1 Port B

Table 4-5 Port B Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AE1	PB0	I/O	Z	PU/PD	4 mA	VCC-IO
AE2	PB1	I/O	Z	PU/PD	4 mA	VCC-IO
1U2	PB2	I/O	Z	PU/PD	4 mA	VCC-IO
1U3	PB3	I/O	Z	PU/PD	4 mA	VCC-IO
AF2	PB4	I/O	Z	PU/PD	4 mA	VCC-IO
AG2	PB5	I/O	Z	PU/PD	4 mA	VCC-IO
AH1	PB6	I/O	Z	PU/PD	4 mA	VCC-IO
AH2	PB7	I/O	Z	PU/PD	4 mA	VCC-IO
AJ2	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
1W4	PB9	I/O	Z	PU/PD	4 mA	VCC-IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1W3	PB10	I/O	Z	PU/PD	4 mA	VCC-IO

4.1.5.2 Port C

Table 4-6 Port C Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1AD26	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
1AD25	PC1	I/O	Z	PU/PD	4 mA	VCC-PC
1AB23	PC2	I/O	Z	PU/PD	4 mA	VCC-PC
1AB24	PC3	I/O	PU	PU/PD	4 mA	VCC-PC
1Y22	PC4	I/O	PU	PU/PD	4 mA	VCC-PC
AK36	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
AL36	PC6	I/O	PU	PU/PD	4 mA	VCC-PC
1Y23	PC7	I/O	PU	PU/PD	4 mA	VCC-PC
AT37	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
AT36	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
AR36	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
AP36	PC11	I/O	Z	PU/PD	4 mA	VCC-PC
1AB26	PC12	I/O	Z	PU/PD	4 mA	VCC-PC
AP37	PC13	I/O	Z	PU/PD	4 mA	VCC-PC
AN37	PC14	I/O	Z	PU/PD	4 mA	VCC-PC
AN36	PC15	I/O	Z	PU/PD	4 mA	VCC-PC
AM36	PC16	I/O	Z	PU/PD	4 mA	VCC-PC
1Y21	VCC-PC	P	N/A	N/A	N/A	N/A

4.1.5.3 Port D

Table 4-7 Port D Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D2	PD0	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
E2	PD1	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
F2	PD2	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
F1	PD3	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
G1	PD4	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
G2	PD5	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
J1	PD6	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
J2	PD7	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
K1	PD8	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
K2	PD9	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1J4	PD10	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1J3	PD11	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1G2	PD12	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1G1	PD13	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1J1	PD14	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1J2	PD15	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
M2	PD16	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
M1	PD17	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
N2	PD18	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
N1	PD19	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS
1L3	PD20	I/O	Z	PU/PD	4 mA	VCC-PD
1L2	PD21	I/O	Z	PU/PD	4 mA	VCC-PD
1L1	PD22	I/O	Z	PU/PD	4 mA	VCC-PD
P2	PD23	I/O	Z	PU/PD	4 mA	VCC-PD
1N6	VCC-LVDS	P	N/A	N/A	N/A	N/A
1N7	VCC-PD	P	N/A	N/A	N/A	N/A

4.1.5.4 Port E

Table 4-8 Port E Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A6	PE0	I/O	Z	PU/PD	4 mA	VCC-PE
B6	PE1	OD	Z	PU/PD	4 mA	VCC-PE
B5	PE2	I/O	Z	PU/PD	4 mA	VCC-PE
B4	PE3	I/O	Z	PU/PD	4 mA	VCC-PE
A4	PE4	OD	Z	PU/PD	4 mA	VCC-PE
1B5	PE5	I/O	Z	PU/PD	4 mA	VCC-PE
1C5	PE6	I/O	Z	PU/PD	4 mA	VCC-PE
B3	PE7	I/O	Z	PU/PD	4 mA	VCC-PE
B2	PE8	I/O	Z	PU/PD	4 mA	VCC-PE
A2	PE9	I/O	Z	PU/PD	4 mA	VCC-PE
1A3	PE10	I/O	Z	PU/PD	4 mA	VCC-PE
1A1	PE11	I/O	Z	PU/PD	4 mA	VCC-PE
B1	PE12	I/O	Z	PU/PD	4 mA	VCC-PE
1C3	PE13	I/O	Z	PU/PD	4 mA	VCC-PE
C2	PE14	I/O	Z	PU/PD	4 mA	VCC-PE
D1	PE15	I/O	Z	PU/PD	4 mA	VCC-PE
1G7	VCC-PE	P	N/A	N/A	N/A	N/A

4.1.5.5 Port F

Table 4-9 Port F Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1U1	PF0	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
AD2	PF1	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
AD1	PF2	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
AB2	PF3	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
1R1	PF4	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1R4	PF5	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
1R3	PF6	I/O	Z	PU/PD	4 mA	VCC18-PF/VCC-IO
1U5	VCC-IO	P	N/A	N/A	N/A	N/A
1U6	VCC18-PF	P	N/A	N/A	N/A	N/A

4.1.5.6 Port G

Table 4-10 Port G Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1N3	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
1N2	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
1N1	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
R2	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
R1	PG4	I/O	Z	PU/PD	4 mA	VCC-PG
T2	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
T1	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
V2	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
V1	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
W2	PG9	I/O	Z	PU/PD	4 mA	VCC-PG
W1	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
Y2	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
AA2	PG12	I/O	Z	PU/PD	4 mA	VCC-PG
AB1	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
AA1	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
1R5	VCC-PG	P	N/A	N/A	N/A	N/A

4.1.5.7 Port H

Table 4-11 Port H Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AK1	PH0	I/O	Z	PU/PD	4 mA	VCC-PH
AK2	PH1	I/O	Z	PU/PD	4 mA	VCC-PH
1AA2	PH2	I/O	Z	PU/PD	4 mA	VCC-PH
1AA1	PH3	I/O	Z	PU/PD	4 mA	VCC-PH
AL1	PH4	I/O	Z	PU/PD	4 mA	VCC-PH
AM2	PH5	I/O	Z	PU/PD	4 mA	VCC-PH
AN1	PH6	I/O	Z	PU/PD	4 mA	VCC-PH
AL2	PH7	I/O	Z	PU/PD	4 mA	VCC-PH
AP1	PH8	I/O	Z	PU/PD	4 mA	VCC-PH
1AC1	PH9	I/O	Z	PU/PD	4 mA	VCC-PH
1AE1	PH10	I/O	Z	PU/PD	4 mA	VCC-PH
1AC2	PH11	I/O	Z	PU/PD	4 mA	VCC-PH
AT2	PH12	I/O	Z	PU/PD	4 mA	VCC-PH
AP2	PH13	I/O	Z	PU/PD	4 mA	VCC-PH
AR2	PH14	I/O	Z	PU/PD	4 mA	VCC-PH
AT1	PH15	I/O	Z	PU/PD	4 mA	VCC-PH
AU2	PH16	I/O	Z	PU/PD	4 mA	VCC-PH
1W6	VCC-PH	P	N/A	N/A	N/A	N/A

4.1.5.8 Port J

Table 4-12 Port J Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1E2	PJ22	I/O	Z	PU/PD	4 mA	VCC-PJ
1E1	PJ23	I/O	Z	PU/PD	4 mA	VCC-PJ
1C2	PJ24	I/O	Z	PU/PD	4 mA	VCC-PJ
1C1	PJ25	I/O	Z	PU/PD	4 mA	VCC-PJ

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1E3	PJ26	I/O	Z	PU/PD	4 mA	VCC-PJ
1E4	PJ27	I/O	Z	PU/PD	4 mA	VCC-PJ
1L6	VCC-PJ	P	N/A	N/A	N/A	N/A

4.1.5.9 Port K

Table 4-13 Port K Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1D11	PK0	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1C11	PK1	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1B11	PK2	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1A11	PK3	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1B7	PK4	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1A7	PK5	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1B9	PK6	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1A9	PK7	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1E9	PK8	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1D9	PK9	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B16	PK10	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B17	PK11	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A15	PK12	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A16	PK13	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B13	PK14	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B14	PK15	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A12	PK16	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A13	PK17	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B11	PK18	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B12	PK19	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A10	PK20	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B10	PK21	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B9	PK22	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A9	PK23	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B7	PK24	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B8	PK25	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
1H11	VCC-PK	P	N/A	N/A	N/A	N/A
1G9	VCC-MCSI	P	N/A	N/A	N/A	N/A

4.1.5.10Port L

Table 4-14 Port L Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
M37	PL0	I/O	PU	PU/PD	4 mA	VCC-PL
M36	PL1	I/O	PU	PU/PD	4 mA	VCC-PL
L36	PL2	I/O	Z	PU/PD	4 mA	VCC-PL
K36	PL3	I/O	Z	PU/PD	4 mA	VCC-PL
K37	PL4	I/O	Z	PU/PD	4 mA	VCC-PL
J37	PL5	I/O	Z	PU/PD	4 mA	VCC-PL
H36	PL6	I/O	Z	PU/PD	4 mA	VCC-PL
G36	PL7	I/O	Z	PU/PD	4 mA	VCC-PL
G37	PL8	I/O	Z	PU/PD	4 mA	VCC-PL
F37	PL9	I/O	Z	PU/PD	4 mA	VCC-PL
1B26	PL10	I/O	Z	PU/PD	4 mA	VCC-PL
1B25	PL11	I/O	Z	PU/PD	4 mA	VCC-PL
1H26	PL12	I/O	Z	PU/PD	4 mA	VCC-PL
1H25	PL13	I/O	Z	PU/PD	4 mA	VCC-PL
1M23	VCC-PL	p	N/A	N/A	N/A	N/A

4.1.5.11Port M

Table 4-15 Port M Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
T37	PM0	I/O	Z	PU/PD	4 mA	VCC-PM
R37	PM1	I/O	Z	PU/PD	4 mA	VCC-PM
P36	PM2	I/O	Z	PU/PD	4 mA	VCC-PM
R36	PM3	I/O	Z	PU/PD	4 mA	VCC-PM
N37	PM4	I/O	Z	PU/PD	4 mA	VCC-PM
N36	PM5	I/O	Z	PU/PD	4 mA	VCC-PM
1P22	VCC-PM	p	N/A	N/A	N/A	N/A

4.1.6 USB2.0 DRD

Table 4-16 USB2.0 DRD Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D36	USB0-DM	AI/O	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB
D37	USB0-DP	AI/O	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB
1B23	USB0-REXT	AO	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB
1D21	VDD08-USB	P	N/A	N/A	N/A	N/A
1E19	VCC33-USB	P	N/A	N/A	N/A	N/A
1F19	VCC33-18-USB	P	N/A	N/A	N/A	N/A

4.1.7 USB2.0 Host

Table 4-17 USB2.0 Host Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
F36	USB1-DM	AI/O	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB
E36	USB1-DP	AI/O	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB
1A25	USB1-REXT	AO	N/A	N/A	N/A	VCC33-USB/ VCC33-18-USB

4.1.8 USB2.0 PHY

Table 4-18 USB2.0 PHY Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B37	USB2-DM	AI/O	N/A	N/A	N/A	VCC33-USB2-U2/ VCC33-18-USB2-U2
C36	USB2-DP	AI/O	N/A	N/A	N/A	VCC33-USB2-U2/ VCC33-18-USB2-U2
1A23	USB2-REXT	AO	N/A	N/A	N/A	VCC33-USB2-U2/ VCC33-18-USB2-U2
1F17	VCC33-USB2-U2	P	N/A	N/A	N/A	N/A
1D19	VCC33-18-USB2-U2	P	N/A	N/A	N/A	N/A

4.1.9 COMB0-PHY-SERDES

Table 4-19 COMB0-PHY-SERDES[8] Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B25	COMB0-TX0P	AO	N/A	N/A	N/A	VDD-SYS
A25	COMB0-TX0N	AO	N/A	N/A	N/A	VDD-SYS

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B32	COMB0-TX3P	AO	N/A	N/A	N/A	VDD-SYS
B31	COMB0-TX3N	AO	N/A	N/A	N/A	VDD-SYS
B29	COMB0-REF-CLKP	AI/O	N/A	N/A	N/A	VDD-SYS
B28	COMB0-REF-CLKN	AI/O	N/A	N/A	N/A	VDD-SYS
1A19	COMB0-CMN-REXT	AI/O	N/A	N/A	N/A	VDD-SYS
A27	COMB0-TX1P	AI/O	N/A	N/A	N/A	VDD-SYS
B27	COMB0-TX1N	AI/O	N/A	N/A	N/A	VDD-SYS
A30	COMB0-TX2P	AI/O	N/A	N/A	N/A	VDD-SYS
B30	COMB0-TX2N	AI/O	N/A	N/A	N/A	VDD-SYS
1F15	AVDD-C-COMB0	P	N/A	N/A	N/A	N/A
1G15	AVDD-D-COMB0	P	N/A	N/A	N/A	N/A
1E15	AVDD-H-COMB0	P	N/A	N/A	N/A	N/A

4.1.10 eDP1.4b/DP1.4 AUX PHY

Table 4-20 eDP1.4b/DP1.4 AUX PHY Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A24	EDP-AUXP	AI/O	N/A	N/A	N/A	AVDD-H-COMB0
B24	EDP-AUXN	AI/O	N/A	N/A	N/A	AVDD-H-COMB0
1A15	AUX-HPD	AI	N/A	N/A	N/A	VCC-IO
1H13	AVDD-HPD-AUX	P	N/A	N/A	N/A	N/A

4.1.11 COMB1-PHY-SERDES

Table 4-21 COMB1-PHY-SERDES [9] Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A36	COMB1-TX0P	AO	N/A	N/A	N/A	VDD-SYS
B36	COMB1-TX0N	AO	N/A	N/A	N/A	VDD-SYS
B35	COMB1-RX0P	AI	N/A	N/A	N/A	VDD-SYS
B34	COMB1-RX0N	AI	N/A	N/A	N/A	VDD-SYS
A34	COMB1-REF-CLKP	AI/O	N/A	N/A	N/A	VDD-SYS
A33	COMB1-REF-CLKN	AI/O	N/A	N/A	N/A	VDD-SYS
1C19	COMB1-REXT	AI/O	N/A	N/A	N/A	VDD-SYS

4.1.12 HDMI

Table 4-22 HDMI Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B21	HTX0P	AO	N/A	N/A	N/A	VCC18-HDMI
A21	HTX0N	AO	N/A	N/A	N/A	VCC18-HDMI
B19	HTX1P	AO	N/A	N/A	N/A	VCC18-HDMI
B20	HTX1N	AO	N/A	N/A	N/A	VCC18-HDMI
B18	HTX2P	AO	N/A	N/A	N/A	VCC18-HDMI
A18	HTX2N	AO	N/A	N/A	N/A	VCC18-HDMI
A22	HTXCP	AO	N/A	N/A	N/A	VCC18-HDMI
B22	HTXCN	AO	N/A	N/A	N/A	VCC18-HDMI
1A13	HSCL	OD	N/A	N/A	N/A	OD-PAD
1B13	HSDA	OD	N/A	N/A	N/A	OD-PAD
1C13	HCEC	OD	N/A	N/A	N/A	OD-PAD

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1E13	HHPD	AI	N/A	N/A	N/A	OD-PAD
1D13	HREXT	AO	N/A	N/A	N/A	VCC18-HDMI
1F13	VCC18-HDMI	P	N/A	N/A	N/A	N/A
1G13	VDD08-HDMI	P	N/A	N/A	N/A	N/A

4.1.13 UFS

Table 4-23 UFS Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AE37	UFS-TX0-P	AO	N/A	N/A	N/A	VDD-SYS
AE36	UFS-TX0-N	AO	N/A	N/A	N/A	VDD-SYS
AG36	UFS-RX0-P	AI	N/A	N/A	N/A	VDD-SYS
AG37	UFS-RX0-N	AI	N/A	N/A	N/A	VDD-SYS
AD37	UFS-TX1-P	AO	N/A	N/A	N/A	VDD-SYS
AD36	UFS-TX1-N	AO	N/A	N/A	N/A	VDD-SYS
AH36	UFS-RX1-P	AI	N/A	N/A	N/A	VDD-SYS
AH37	UFS-RX1-N	AI	N/A	N/A	N/A	VDD-SYS
1V26	UFS-REXT	AO	N/A	N/A	N/A	VDD-SYS
1Y25	UFS-REFM	AI	N/A	N/A	N/A	VDD-SYS
1Y26	UFS-REFP	AI	N/A	N/A	N/A	VDD-SYS
1Y24	UFS-RST-N	OD	N/A	N/A	N/A	VCC-PC
1V20	VCC-UFS	P	N/A	N/A	N/A	N/A
1V22	VDD-UFS	P	N/A	N/A	N/A	N/A

4.1.14 CK-ST

Table 4-24 CK-ST Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1K25	CK-SEL0	I	PU	PU	N/A	VCC-RTC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1K26	CK-SEL1	I	PU	PU	N/A	VCC-RTC

4.1.15 GPADC

Table 4-25 GPADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1D24	BOOT-SEL-GPADC0-0	AI	N/A	N/A	N/A	VCC-ADC
1D25	BOARD-ID-GPADC0-1	AI	N/A	N/A	N/A	VCC-ADC
1D26	BOARD-ID-GPADC0-2	AI	N/A	N/A	N/A	VCC-ADC
1F24	GPADC0-3	AI	N/A	N/A	N/A	VCC-ADC
1F25	GPADC0-4	AI	N/A	N/A	N/A	VCC-ADC
1H23	GPADC0-5	AI	N/A	N/A	N/A	VCC-ADC
1H24	GPADC0-6	AI	N/A	N/A	N/A	VCC-ADC
1H22	VCM-ADC	AO	N/A	N/A	N/A	VCC-ADC
1F21	VREFP-ADC	P	N/A	N/A	N/A	N/A
1F22	VREFN-ADC	G	N/A	N/A	N/A	AGND

4.1.16 LRADC

Table 4-26 LRADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1D23	LRADC0-0	AI	N/A	N/A	N/A	VCC-ADC

4.1.17 IBIAS

Table 4-27 IBIAS Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1H21	VCC-ADC	P	N/A	N/A	N/A	N/A
1F23	AGND	G	N/A	N/A	N/A	AGND

4.1.18 System Control

Table 4-28 System Control Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1W1	FEL	I	PU	PU	N/A	VCC-IO
1W2	JTAG-SEL	I	PU	PU	N/A	VCC-IO
1M25	TEST	I	PD	PD	N/A	VCC-RTC
1M26	NMI	OD	N/A	N/A	N/A	VCC-RTC
1M24	RESET	OD	N/A	N/A	N/A	VCC-RTC
1W5	VCC-EFUSE	P	N/A	N/A	N/A	N/A

4.1.19 Power

Table 4-29 Power Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1M20	VDD-CPUS	P	N/A	N/A	N/A	N/A
1J18	VDD-CPUB	P	N/A	N/A	N/A	N/A
1J19	VDD-CPUB	P	N/A	N/A	N/A	N/A
1K14	VDD-CPUB	P	N/A	N/A	N/A	N/A
1K15	VDD-CPUB	P	N/A	N/A	N/A	N/A
1K16	VDD-CPUB	P	N/A	N/A	N/A	N/A
1K17	VDD-CPUB	P	N/A	N/A	N/A	N/A
1K19	VDD-CPUB	P	N/A	N/A	N/A	N/A
1L15	VDD-CPUB	P	N/A	N/A	N/A	N/A
1L16	VDD-CPUB	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1K21	VDD-CPUBFB	P	N/A	N/A	N/A	N/A
1P21	VDD-CPULFB	P	N/A	N/A	N/A	N/A
1L18	VDD-CPUL	P	N/A	N/A	N/A	N/A
1M16	VDD-CPUL	P	N/A	N/A	N/A	N/A
1M17	VDD-CPUL	P	N/A	N/A	N/A	N/A
1M18	VDD-CPUL	P	N/A	N/A	N/A	N/A
1M19	VDD-CPUL	P	N/A	N/A	N/A	N/A
1P17	VDD-CPUL	P	N/A	N/A	N/A	N/A
1P18	VDD-CPUL	P	N/A	N/A	N/A	N/A
1P19	VDD-CPUL	P	N/A	N/A	N/A	N/A
1T15	VDD-GPU	P	N/A	N/A	N/A	N/A
1T16	VDD-GPU	P	N/A	N/A	N/A	N/A
1T17	VDD-GPU	P	N/A	N/A	N/A	N/A
1T18	VDD-GPU	P	N/A	N/A	N/A	N/A
1U18	VDD-GPU	P	N/A	N/A	N/A	N/A
1R13	VDD-GPUFB	P	N/A	N/A	N/A	N/A
1R8	VDD-VE	P	N/A	N/A	N/A	N/A
1P9	VDD-VE	P	N/A	N/A	N/A	N/A
1J9	VDD-SYS	P	N/A	N/A	N/A	N/A
1J10	VDD-SYS	P	N/A	N/A	N/A	N/A
1K9	VDD-SYS	P	N/A	N/A	N/A	N/A
1L9	VDD-SYS	P	N/A	N/A	N/A	N/A
1L10	VDD-SYS	P	N/A	N/A	N/A	N/A
1M10	VDD-SYS	P	N/A	N/A	N/A	N/A
1R12	VDD-SYS	P	N/A	N/A	N/A	N/A
1U10	VDD-SYS	P	N/A	N/A	N/A	N/A
1V18	VDD-SYS	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1K13	VDD-SYSFB	P	N/A	N/A	N/A	N/A

4.1.20 Ground

Table 4-30 Ground Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]
A1, A7, A19, A28, A31, A37, B15, B23, B26, B33, H2, J36, L2, T36, U2, V36, W36, AA37, AB36, AC2, AC36, AF36, AG1, AJ36, AK37, AL37, AN2, AT5, AT8, AT12, AT13, AT17, AT24, AT26, AT30, AU1, AU10, AU15, AU19, AU22, AU34, AU37, 1A5, 1A17, 1A21, 1B3, 1B15, 1B17, 1B19, 1B21, 1C7, 1C9, 1C15, 1C17, 1C21, 1C23, 1D5, 1D7, 1E5, 1E7, 1E11, 1E21, 1F7, 1F9, 1F11, 1F26, 1G3, 1G4, 1G5, 1G11, 1G17, 1G19, 1H14, 1H17, 1H19, 1J5, 1J6, 1J13, 1K12, 1K22, 1K23, 1K24, 1L4, 1L5, 1L7, 1L8, 1L11, 1L12, 1L13, 1M11, 1M13, 1M14, 1M21, 1M22, 1N4, 1N5, 1N8, 1N9, 1N12, 1N14, 1N15, 1P14, 1P15, 1P24, 1R2, 1R6, 1R7, 1R9, 1R14, 1T12, 1T22, 1T23, 1T25, 1U4, 1U12, 1U21, 1V10, 1V11, 1V16, 1V21, 1V23, 1V24, 1V25, 1W9, 1W16, 1W20, 1Y8, 1Y10, 1Y11, 1Y12, 1Y16, 1Y17, 1AA3, 1AA4, 1AA5, 1AA6, 1AA8, 1AA10, 1AA12, 1AA14, 1AA16, 1AA17, 1AA18, 1AA20, 1AB14, 1AB18, 1AB25, 1AC3, 1AC22, 1AD4, 1AD6, 1AD8, 1AD10, 1AD12, 1AD14, 1AD16, 1AD18, 1AD20, 1AD22, 1AD24, 1AF24, 1AF26, 1D15, 1D17, 1E17	GND	G

4.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.

NOTE

(1) For each GPIO, Function0 is input function; Function1 is output function; Function10 to Function13 are reserved.

(2) If I2S3 needs to be used, please ensure that the peripheral devices connected to I2S3 signals will not be used with eDP and HDMI interfaces simultaneously. If you have any question, please contact Allwinner FAE.

(3) If I2S4 needs to be used, please ensure that the peripheral devices connected to I2S4 signals will not be used with eDP interfaces simultaneously. If you have any question, please contact Allwinner FAE.

4.2.1 Port B

Table 4-31 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PB0	I/O	UART2-TX	UART0-TX	SPI2-CS0	DSI-TRIG-LCD-TE1	LCD0-D0	JTAG-MS			PB-EINT0
PB1	I/O	UART2-RX	UART0-RX	SPI2-CLK		LCD0-D1	JTAG-CK			PB-EINT1
PB2	I/O	UART2-RTS		SPI2-MOSI	HDMI-SCL	LCD0-D8	JTAG-DO	TWI0-SCK		PB-EINT2
PB3	I/O	UART2-CTS		SPI2-MISO	HDMI-SDA	LCD0-D9	JTAG-DI	TWI0-SDA		PB-EINT3
PB4	I/O	PWM0-0	I2S0-MCLK	SPI2-CS1	HDMI-CEC	LCD0-D16		TWI1-SCK		PB-EINT4
PB5	I/O		I2S0-BCLK	SPI2-CS2	PWM0-1	LCD0-D17		TWI1-SDA		PB-EINT5
PB6	I/O	CLK-FANOUT1	I2S0-LRCK	SPI2-CS3	PWM0-2	PWM0-8				PB-EINT6
PB7	I/O	CLK-FANOUT2	I2S0-DOUT0	I2S0-DIN1	PWM0-9	OWA0-IN		TWI1-SCK		PB-EINT7
PB8	I/O	CLK-FANOUT3	I2S0-DIN0	I2S0-DOUT1	PWM1-0	OWA0-OUT		TWI1-SDA		PB-EINT8
PB9	I/O	UART0-TX	I2S0-DIN2	I2S0-DOUT2	PWM1-1	WATCHDOG-SIG	LCD0-D16	TWI8-SCK	TWI0-SCK	PB-EINT9
PB10	I/O	UART0-RX	I2S0-DIN3	I2S0-DOUT3	PWM1-2		LCD0-D17	TWI8-SDA	TWI0-SDA	PB-EINT10

4.2.2 Port C

Table 4-32 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PC0	I/O	NAND-WE	SDC2-DS	SDC3-DS						PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST	SDC3-RST						PC-EINT1
PC2	I/O	NAND-CLE			SPI0-MOSI	SPIF0-MOSI				PC-EINT2
PC3	I/O	NAND-CE1			SPI0-CS0	SPIF0-CS0				PC-EINT3
PC4	I/O	NAND-CE0			SPI0-MISO	SPIF0-MISO				PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK	SDC3-CLK						PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD	SDC3-CMD						PC-EINT6
PC7	I/O	NAND-RB1			SPI0-CS1	SPIF0-DQS				PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3	SDC3-D3		SPIF0-D7				PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4	SDC3-D4		SPIF0-D6				PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0	SDC3-D0		SPIF0-D5				PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5	SDC3-D5		SPIF0-D4				PC-EINT11
PC12	I/O	NAND-DQS			SPI0-CLK	SPIF0-CLK				PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1	SDC3-D1						PC-EINT13

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PC14	I/O	NAND-DQ2	SDC2-D6	SDC3-D6						PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SDC3-D2	SPI0-WP	SPIF0-WP<SPIF0-D2>				PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SDC3-D7	SPI0-HOLD	SPIF0-HOLD<SPIF0-D3>				PC-EINT16

4.2.3 Port D

Table 4-33 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI0-D0P	EINK-D0		PWM0-0			PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI0-D0N	EINK-D1		PWM0-1			PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI0-D1P	EINK-D2		PWM0-2			PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI0-D1N	EINK-D3		PWM0-3			PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI0-CKP	EINK-D4		PWM0-4			PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI0-CKN	EINK-D5		PWM0-5			PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI0-D2P	EINK-D6		PWM0-6			PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI0-D2N	EINK-D7		PWM0-7			PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI0-D3P	EINK-D8		PWM0-8			PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI0-D3N	EINK-D9		PWM0-9			PD-EINT9
PD10	I/O	LCD0-D14	LVDS1-D0P	DSI1-D0P	EINK-D10	SPI1-CS0 /DBI-CSX	PWM1-0			PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	DSI1-D0N	EINK-D11	SPI1-CLK /DBI-SCLK	PWM1-1			PD-EINT11
PD12	I/O	LCD0-D18	LVDS1-D1P	DSI1-D1P	EINK-D12	SPI1-MOSI /DBI-SDO	PWM1-2			PD-EINT12
PD13	I/O	LCD0-D19	LVDS1-D1N	DSI1-D1N	EINK-D13	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-3			PD-EINT13
PD14	I/O	LCD0-D20	LVDS1-D2P	DSI1-CKP	EINK-D14	SPI1-HOLD/DBI-DCX/DBI-WRX	UART3-RTS			PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	DSI1-CKN	EINK-D15	SPI1-CS1	UART3-CTS			PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DSI1-D2P	EINK-OEH	TWI2-SCK	UART3-TX			PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DSI1-D2N	EINK-LEH	TWI2-SDA	UART3-RX			PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DSI1-D3P	EINK-CKH	SPI1-WP /DBI-TE	UART4-RTS			PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DSI1-D3N	EINK-STH	PWM1-5	UART4-CTS			PD-EINT19
PD20	I/O	LCD0-HSYNC	DSI-TRIG-LCD-TE1	TWI0-SCK	EINK-CKV	PCIE-CLKREQN	UART4-TX	TWI3-SCK	PWM0-2	PD-EINT20
PD21	I/O	LCD0-VSYNC		TWI0-SDA	EINK-MODE	PCIE-WAKEN	UART4-RX	TWI3-SDA	PWM0-3	PD-EINT21
PD22	I/O	PWM0-4			EINK-STV	PCIE-PERSTN	TWI0-SCK	TWI2-SCK	PWM1-4	PD-EINT22
PD23	I/O	PWM0-5				PCIE-CLKREQN	TWI0-SDA	TWI2-SDA	PWM1-5	PD-EINT23

4.2.4 Port E

Table 4-34 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PE0	I/O	MCSI0-MCLK	CSI0-XHS		SPI3-CS0		NCSI0-HSYNC	UART6-TX		PE-EINT0
PE1	OD	TWI2-SCK	CSI1-XHS		SPI3-CLK		NCSI0-VSYNC	UART6-RX		PE-EINT1
PE2	I/O	TWI2-SDA	CSI0-XVS-FSYNC		SPI3-MOSI		NCSI0-PCLK	UART6-RTS		PE-EINT2
PE3	I/O	TWI3-SCK	CSI1-XVS-FSYNC	PWM0-0	SPI3-MISO		NCSI0-D1	UART6-CTS		PE-EINT3
PE4	OD	TWI3-SDA	LEDC	PWM0-1	SPI3-CS1		NCSI0-D0	UART6-DCD		PE-EINT4
PE5	I/O	MCSI1-MCLK			PWM0-2		NCSI0-MCLK	UART6-DSR		PE-EINT5
PE6	I/O	CLK-FANOUT1	HDMI-CEC	I2S3-DIN0<MUX-HDMI-EDP>	I2S3-DOUT1<MUX-HDMI-EDP>		NCSI0-D2	UART6-DTR		PE-EINT6
PE7	I/O	CLK-FANOUT2	HDMI-SCL	I2S3-BCLK<MUX-HDMI-EDP>			NCSI0-D3	TWI11-SCK		PE-EINT7
PE8	I/O	CLK-FANOUT3	HDMI-SDA	I2S3-LRCK<MUX-HDMI-EDP>			NCSI0-D4	TWI11-SDA		PE-EINT8
PE9	I/O	MCSI2-MCLK	TCON-FSYNC0	I2S3-MCLK<MUX-HDMI-EDP>			NCSI0-D5	UART6-RI		PE-EINT9
PE10	I/O	TWI4-SCK	TCON-FSYNC1	I2S3-DIN3<MUX-HDMI-EDP>	I2S3-DOUT3<MUX-HDMI-EDP>		NCSI0-D6	UART1-RTS		PE-EINT10
PE11	I/O	TWI4-SDA	SPI3-MISO	I2S3-DIN2<MUX-HDMI-EDP>	I2S3-DOUT2<MUX-HDMI-EDP>	PCIE-CLKREQN	NCSI0-D7	UART1-CTS		PE-EINT11
PE12	I/O		SPI3-CS0	I2S3-DOUT0<MUX-HDMI-EDP>	I2S3-DIN1<MUX-HDMI-EDP>	PCIE-WAKEN		UART1-TX		PE-EINT12
PE13	I/O		SPI3-CLK			PCIE-PERSTN		UART1-RX		PE-EINT13
PE14	I/O		SPI3-MOSI		PWM1-8	PCIE-CLKREQN	IR-RX	TWI9-SCK		PE-EINT14
PE15	I/O		SPI3-CS1		PWM1-9	IR-RX		TWI9-SDA		PE-EINT15

4.2.5 Port F

Table 4-35 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PF0	I/O	SDC0-D1	JTAG-MS		UART5-RTS	TWI2-SCK				PF-EINT0
PF1	I/O	SDC0-CMD	JTAG-DO							PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX							PF-EINT2
PF3	I/O	SDC0-D0	JTAG-DI		UART5-CTS	TWI2-SDA				PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		UART5-RX					PF-EINT4

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PF5	I/O	SDC0-D2	JTAG-CK		UART5-TX					PF-EINT5
PF6	I/O									PF-EINT6

4.2.6 Port G

Table 4-36 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PG0	I/O	SDC1-CLK	LCD0-D0	PWM1-1						PG-EINT0
PG1	I/O	SDC1-CMD	LCD0-D1	PWM1-2						PG-EINT1
PG2	I/O	SDC1-D0	LCD0-D8	PWM1-3						PG-EINT2
PG3	I/O	SDC1-D1	LCD0-D9	PWM1-4						PG-EINT3
PG4	I/O	SDC1-D2	LCD0-D16	PWM1-5						PG-EINT4
PG5	I/O	SDC1-D3	LCD0-D17	PWM1-6						PG-EINT5
PG6	I/O	UART1-TX	UART4-TX	PWM1-7						PG-EINT6
PG7	I/O	UART1-RX	UART4-RX	PWM1-8						PG-EINT7
PG8	I/O	UART1-RTS	UART4-RTS	UART5-TX		TWI0-SCK				PG-EINT8
PG9	I/O	UART1-CTS	UART4-CTS	UART5-RX		TWI0-SDA				PG-EINT9
PG10	I/O	I2S1-MCLK	CLK-FANOUT0	PWM1-9		DMIC-CLK				PG-EINT10
PG11	I/O	I2S1-BCLK	TWI12-SCK	TWI9-SCK		DMIC-DATA3	HDMI-CEC			PG-EINT11
PG12	I/O	I2S1-LRCK	TWI12-SDA	TWI9-SDA		DMIC-DATA2	HDMI-SCL			PG-EINT12
PG13	I/O	I2S1-DOUT0	I2S1-DIN1	TWI6-SCK		DMIC-DATA1	HDMI-SDA			PG-EINT13
PG14	I/O	I2S1-DIN0	I2S1-DOUT1	TWI6-SDA		DMIC-DATA0				PG-EINT14

4.2.7 Port H

Table 4-37 Port H Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PH0	I/O	TWI0-SCK	I2S2-DOUT2	I2S2-DIN2	RGMII0-RXD1/RMII0-RXD1	TWI3-SCK	SPI1-HOLD			PH-EINT0
PH1	I/O	TWI0-SDA	I2S2-DOUT3	I2S2-DIN3	RGMII0-RXD0/RMII0-RXD0	TWI3-SDA	SPI1-WP			PH-EINT1
PH2	I/O	TWI1-SCK		I2S2-MCLK	RGMII0-RXCTL/RMII0-CRS-DV		SPI1-CS1			PH-EINT2
PH3	I/O	TWI1-SDA		I2S2-BCLK	RGMII0-CLKIN/RMII0-RXER		SPI1-MISO			PH-EINT3
PH4	I/O	UART3-TX	SPI2-CS3	I2S2-LRCK	RGMII0-TXD1/RMII0-TXD1		SPI1-CS0			PH-EINT4
PH5	I/O	UART3-RX	I2S2-DIN1	I2S2-DOUT0	RGMII0-TXD0/RMII0-TXD0		SPI1-MOSI			PH-EINT5

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PH6	I/O	UART3-RTS	I2S2-DOUT1	I2S2-DIN0	RGMII0-TXCK/RMII0-TXCK		SPI1-CLK			PH-EINT6
PH7	I/O	UART3-CTS	SPI2-CS2	DSI-TRIG-LCD-TE1	RGMII0-TXCTL/RMII0-TXEN					PH-EINT7
PH8	I/O	DMIC-CLK	SPI2-CLK		RGMII0-MDC					PH-EINT8
PH9	I/O	DMIC-DATA0	SPI2-CS0		RGMII0-MDIO					PH-EINT9
PH10	I/O	DMIC-DATA1	SPI2-MOSI		RGMII0-RXD3/RMII0-NULL					PH-EINT10
PH11	I/O	DMIC-DATA2	SPI2-MISO		RGMII0-RXD2/RMII0-NULL					PH-EINT11
PH12	I/O	DMIC-DATA3	SPI2-CS1		RGMII0-RXCK/RMII0-NULL					PH-EINT12
PH13	I/O	UART5-TX			RGMII0-TXD3/RMII0-NULL	TWI7-SDA				PH-EINT13
PH14	I/O	UART5-RX			RGMII0-TXD2/RMII0-NULL	TWI7-SCK				PH-EINT14
PH15	I/O	UART5-RTS	LEDC	DSI-TRIG-LCD-TE1	RGMII0-EPHY-25/50M					PH-EINT15
PH16	I/O	UART5-CTS			IR-TX					PH-EINT16

4.2.8 Port J

Table 4-38 PJ Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PJ22	I/O		PWM1-4	UART3-TX	UART2-RTS	TWI7-SCK	TWI3-SCK	TWI11-SCK	LCD0-D8	PJ-EINT22
PJ23	I/O		PWM1-5	UART3-RX	UART2-CTS	TWI7-SDA	TWI3-SDA	TWI11-SDA	LCD0-D9	PJ-EINT23
PJ24	I/O		PWM1-6	UART4-TX			TWI4-SCK	SPI3-CLK		PJ-EINT24
PJ25	I/O		PWM1-7	UART4-RX			TWI4-SDA	SPI3-MOSI		PJ-EINT25
PJ26	I/O		PWM1-8	UART4-RTS	UART2-TX		TWI5-SCK	SPI3-MISO	LCD0-D16	PJ-EINT26
PJ27	I/O		PWM1-9	UART4-CTS	UART2-RX	DSI-TRIG-LCD-TE1	TWI5-SDA	SPI3-CS0	LCD0-D17	PJ-EINT27

4.2.9 Port K

Table 4-39 PK Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PK0	I/O	MCSIA-D0N	UART6-DCD	I2S4-BCLK<MUX-EDP>	HDMI-CEC	TWI1-SDA	NCSI1-HSYNC			PK-EINT0
PK1	I/O	MCSIA-D0P	UART6-DSR	I2S4-MCLK<MUX-EDP>	HDMI-SCL	TWI1-SCK	NCSI1-VSYNC			PK-EINT1
PK2	I/O	MCSIA-D1N	UART6-DTR	I2S4-LRCK<MUX-	HDMI-SDA	TWI5-SDA	NCSI1-PCLK			PK-EINT2

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
				EDP>						
PK3	I/O	MCSIA-D1P	UART6-RI	I2S4-DIN0<MUX-EDP>	I2S4-DOUT1<MUX-EDP>	TWI5-SCK	NCSI1-MCLK			PK-EINT3
PK4	I/O	MCSIA-CKN	PCIE-WAKEN	I2S4-DOUT0<MUX-EDP>	I2S4-DIN1<MUX-EDP>	SPI3-CS0	NCSI1-D15			PK-EINT4
PK5	I/O	MCSIA-CKP	PCIE-CLKREQN	PWM1-8	PWM1-9	SPI3-CLK	NCSI1-D14			PK-EINT5
PK6	I/O	MCSIA-D2N	TWI2-SCK	UART4-TX	UART2-RTS	SPI3-MOSI	NCSI1-D13			PK-EINT6
PK7	I/O	MCSIA-D2P	TWI2-SDA	UART4-RX	UART2-CTS	SPI3-MISO	NCSI1-D12			PK-EINT7
PK8	I/O	MCSIA-D3N	MCSI0-MCLK	UART4-RTS	UART2-TX	SPI3-CS1	NCSI1-D11			PK-EINT8
PK9	I/O	MCSIA-D3P	MCSI2-MCLK	UART4-CTS	UART2-RX		NCSI1-D10			PK-EINT9
PK10	I/O	MCSIB-D0N	UART6-TX		PWM0-3		NCSI1-D9			PK-EINT10
PK11	I/O	MCSIB-D0P	UART6-RX		PWM0-4		NCSI1-D8			PK-EINT11
PK12	I/O	MCSIB-D1N	UART6-RTS		PWM0-5		NCSI1-D7			PK-EINT12
PK13	I/O	MCSIB-D1P	UART6-CTS		PWM0-6		NCSI1-D6			PK-EINT13
PK14	I/O	MCSIB-CKN	PCIE-PERSTN		PWM0-7		NCSI1-D5			PK-EINT14
PK15	I/O	MCSIB-CKP			PWM0-8		NCSI1-D4			PK-EINT15
PK16	I/O	MCSIB-D2N	TWI3-SCK	UART2-TX	PWM0-9		NCSI1-D3			PK-EINT16
PK17	I/O	MCSIB-D2P	TWI3-SDA	UART2-RX	PWM1-0		NCSI1-D2			PK-EINT17
PK18	I/O	MCSIB-D3N	MCSI1-MCLK	UART2-RTS	PWM1-1		NCSI1-D1	TWI9-SCK		PK-EINT18
PK19	I/O	MCSIB-D3P	MCSI2-MCLK	UART2-CTS	PWM1-2		NCSI1-D0	TWI9-SDA		PK-EINT19
PK20	I/O	MCSIC-D0N	TWI2-SCK	UART3-TX	PWM0-1		NCSI1-PCLK	UART1-RTS		PK-EINT20
PK21	I/O	MCSIC-D0P	TWI2-SDA	UART3-RX	PWM0-2		NCSI1-MCLK	UART1-CTS		PK-EINT21
PK22	I/O	MCSIC-D1N	TWI3-SCK	UART3-RTS	PWM1-6		NCSI1-HSYNC	UART1-TX		PK-EINT22
PK23	I/O	MCSIC-D1P	TWI3-SDA	UART3-CTS	PWM1-7		NCSI1-VSYNC	UART1-RX		PK-EINT23
PK24	I/O	MCSIC-CKN	MCSI0-MCLK	PWM0-6	TWI12-SCK			TWI10-SDA		PK-EINT24
PK25	I/O	MCSIC-CKP	MCSI1-MCLK	PWM0-7	TWI12-SDA			TWI10-SCK		PK-EINT25

4.2.10 Port L

Table 4-40 PL Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PL0	I/O	S-TWI0-SCK	S-TWI1-SCK	S-TWI2-SCK						PL-EINT0
PL1	I/O	S-TWI0-SDA	S-TWI1-SDA	S-TWI2-SDA	S-IR-RX					PL-EINT1
PL2	I/O	S-UART1-TX	S-UART0-TX	S-TWI1-SDA		S-PWM0-0				PL-EINT2

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PL3	I/O	S-UART1-RX	S-UART0-RX	S-TWI1-SCK	S-IR-RX	S-PWM0-1				PL-EINT3
PL4	I/O	S-JTAG-MS	S-TWI2-SCK	S-SPI0-CS0	S-IR-RX	S-PWM0-2				PL-EINT4
PL5	I/O	S-JTAG-CK	S-TWI2-SDA	S-SPI0-CLK		S-PWM0-3				PL-EINT5
PL6	I/O	S-JTAG-DO	S-UART0-TX	S-SPI0-MOSI	S-IR-RX	S-PWM0-4				PL-EINT6
PL7	I/O	S-JTAG-DI	S-UART0-RX	S-SPI0-MISO		S-PWM0-5				PL-EINT7
PL8	I/O	S-TWI1-SCK	S-UART1-TX	S-TWI0-SCK	S-TWI2-SCK	S-PWM0-6				PL-EINT8
PL9	I/O	S-TWI1-SDA	S-UART1-RX	S-TWI0-SDA	S-TWI2-SDA	S-PWM0-7				PL-EINT9
PL10	I/O	S-UART0-TX	S-TWI2-SCK	S-UART1-TX		S-PWM0-8				PL-EINT10
PL11	I/O	S-UART0-RX	S-TWI2-SDA	S-UART1-RX	S-IR-RX	S-PWM0-9				PL-EINT11
PL12	I/O	S-UART1-TX	S-TWI1-SCK	S-TWI2-SCK	S-IR-RX					PL-EINT12
PL13	I/O	S-UART1-RX	S-TWI1-SDA	S-TWI2-SDA						PL-EINT13

4.2.11 Port M

Table 4-41 PM Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function9	Function14
PM0	I/O	S-JTAG-MS	S-SPI0-CS0	S-RJTAG-MS	S-TWI1-SCK	S-PWM0-2	S-IR-RX			PM-EINT0
PM1	I/O	S-JTAG-CK	S-SPI0-CLK	S-RJTAG-CK	S-TWI1-SDA	S-PWM0-3				PM-EINT1
PM2	I/O	S-JTAG-DO	S-SPI0-MOSI	S-UART0-TX	S-UART1-TX	S-PWM0-4				PM-EINT2
PM3	I/O	S-JTAG-DI	S-SPI0-MISO	S-UART0-RX	S-UART1-RX	S-PWM0-5				PM-EINT3
PM4	I/O	S-UART0-TX	S-TWI2-SCK	S-TWI1-SCK	S-UART1-TX	S-PWM0-0	S-IR-RX			PM-EINT4
PM5	I/O	S-UART0-RX	S-TWI2-SDA	S-TWI1-SDA	S-UART1-RX	S-PWM0-1	S-IR-RX			PM-EINT5

4.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name**: The name of every signal.

[2] **Description**: The detailed function description of every signal.

[3] **Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

4.3.1 DRAM

Table 4-42 DRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
SCA[5:0]-B	DRAM Command Address[5:0] channel B	O
SCKP-B	DRAM CK-P channel B	O
SCKN-B	DRAM CK-N channel B	O
SCA[5:0]-A	DRAM Command Address[5:0] channel A	O
SCS0-A	DRAM Chip Select Signal to the Memory Device for RANK0	O
SCS1-A	DRAM Chip Select Signal to the Memory Device for RANK1	O
SCKP-A	DRAM CK-P channel A	O
SCKN-A	DRAM CK-N channel A	O
SATO	DDRPHY Analog Debug Output	O
SDTO	DDRPHY Digital Debug Output	O
SCKE0-B	DRAM Clock Enable Signal to the Memory Device for Channel B	O
SCKE1-B	DRAM Clock Enable Signal to the Memory Device for Channel B	O

Signal Name[1]	Description[2]	Type[3]
SCS0-B	DRAM Chip Select Signal to the Memory Device for RANK0	O
SCS1-B	DRAM Chip Select Signal to the Memory Device for RANK1	O
SCKE0-A	DRAM Clock Enable Signal to the Memory Device for Channel B	O
SCKE1-A	DRAM Clock Enable Signal to the Memory Device for Channel B	O
SRST	DRAM Reset Signal to the Memory Device	O
WCK0N-A	LPDDR5 Data Clock WCK0-N for channel A	O
WCK0P-A	LPDDR5 Data Clock WCK0-P for channel A	O
SDQS[3:0]P	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	I/O
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
WCK1P-A	LPDDR5 Data Clock WCK1-P for channel A	O
WCK1N-A	LPDDR5 Data Clock WCK1-N for channel A	O
WCK0P-B	LPDDR5 Data Clock WCK0-P for channel B	O
WCK0N-B	LPDDR5 Data Clock WCK0-N for channel B	O
WCK1P-B	LPDDR5 Data Clock WCK1-P for channel B	O
WCK1N-B	LPDDR5 Data Clock WCK1-N for channel B	O
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
VCC-DRAM	Power Supply for DRAM PHY	P
VCC-DRAML	Power Supply for DRAM IO	P
VDD-DRAM	Power Supply for DRAM CORE&PHY	P
VDD18-DRAM	1.8 V Power Supply for DRAM PHY PLL	P

4.3.2 System Control

Table 4-43 System Control Signal Description

Signal Name[1]	Description[2]	Type[3]
FEL	Boot Select	I
JTAG-SEL	JTAG output select	I
TEST	Enable test mode	I
NMI	Non-Maskable Interrupt	I/O, OD

Signal Name[1]	Description[2]	Type[3]
RESET	Reset Signal (Low Active)	I/O, OD
WATCHDOG-SIG	Watchdog Restart Signal	O
VCC-EFUSE	Power Supply for eFuse	P

4.3.3 RTC

Table 4-44 RTC Signal Description

Signal Name[1]	Description[2]	Type[3]
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
X32KFOUT	32.768 kHz clock Fanout	AO,OD
VCC-RTC	Power Supply for RTC	P
RTC-VIO	Digital Power Supply for RTC	P

4.3.4 PLL

Table 4-45 PLL Signal Description

Signal Name[1]	Description[2]	Type[3]
CPU-PLLTEST	CPU PLL Test Signal	AO, OD
PLLTEST	Other PLLs’ Test Signal	AO, OD

4.3.5 DCXO

Table 4-46 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
WREQIN	Request signal of REFCLK-OUT	I
VCC-DCXO	Digital Compensated Crystal Oscillator (DCXO) Power Supply, COMB0_PHY_SERDES REFCLK, and COMB1_PHY_SERDES REFCLK	P
VCC-DCXO1	DCXO Reference Voltage 1	P
VCC-DCXO2	DCXO Reference Voltage 2	P

4.3.6 Clock Select

Table 4-47 Clock Select Signal Description

Signal Name[1]	Description[2]	Type[3]
CK-SEL0	Crystal Frequency Indicator Bit0	I
CK-SEL1	Crystal Frequency Indicator Bit1	I

4.3.7 SMHC

Table 4-48 SMHC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CLK	Clock for SD Card	O
SDC0-CMD	Command Signal for SD Card	I/O, OD
SDC0-D[3:0]	Data Input and Output for SD Card	I/O
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-D[3:0]	Data Input and Output for SD Card	I/O
SDC2-DS	Data Strobe for eMMC	I
SDC2-RST	Reset for eMMC	O
SDC2-CLK	Clock for eMMC	O
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-D[7:0]	Data Input and Output for SD Card	I/O
SDC3-DS	Data Strobe for eMMC	I
SDC3-RST	Reset for eMMC	O
SDC3-CLK	Clock for eMMC	O
SDC3-CMD	Command Signal for eMMC	I/O, OD
SDC3-D[7:0]	Data Input and Output for SD Card	I/O

4.3.8 UFS

Table 4-49 UFS Signal Description

Signal Name[1]	Description[2]	Type[3]
UFS-TX0-P	UFS Lane 0 differential output data signal	AO
UFS-TX0-N	UFS Lane 0 differential output data signal	AO
UFS-RX0-P	UFS Lane 0 differential input data signal	AI

Signal Name[1]	Description[2]	Type[3]
UFS-RX0-N	UFS Lane 0 differential input data signal	AI
UFS-TX1-P	UFS Lane 1 differential output data signal	AO
UFS-TX1-N	UFS Lane 1 differential output data signal	AO
UFS-RX1-P	UFS Lane 1 differential input data signal	AI
UFS-RX1-N	UFS Lane 1 differential input data signal	AI
UFS-REXT	UFS Reference resistance	AO
UFS-REFM	UFS Differential input clock signal	AI
UFS-REFP	UFS Differential input clock signal	AI
UFS-RST-N	UFS Hardware reset signal, active low	OD
VDD-UFS	Power Supply for UFS controller	P
VCC12-UFS	Power Supply for UFS 3.x CORE	P
VCC-UFS	Power Supply for UFS 3.x IO	P

4.3.9 RAW NAND Flash

Table 4-50 RAW NAND Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
NAND-WE	Nand Flash Write Enable	O
NAND-ALE	Nand Flash Address Latch Enable	O
NAND-CLE	Nand Flash Command latch Enable	O
NAND-CE[1:0]	Nand Flash Chip Select	O
NAND-RE	Nand Flash Read Enable	O
NAND-RB[1:0]	Nand Flash Ready/Busy Status Indicator Signal	I
NAND-DQ[7:0]	Nand Flash Data Bit	I/O

4.3.10 SPI Flash

Table 4-51 SPI Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
SPIF0-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF0-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF0-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF0-DQS	Data Strobe Signal	I

Signal Name[1]	Description[2]	Type[3]
SPIF0-D[7:4]	SPI Master Mode Data Input in octal mode. In single/dual/quad mode, this port should stay low.	I/O
SPIF0-CLK	SPI Master Mode Clock Output	O
SPIF0-WP/SPIF0-D2	SPI Write Protect, Low Active	I/O
SPIF0-HOLD/SPIF0-D3	SPI Hold Signal	I/O

4.3.11 E-ink

Table 4-52 E-ink Signal Description

Signal Name[1]	Description[2]	Type[3]
EINK-CKH	Eink Clock Source Driver	O
EINK-CKV	Eink Clock Gate Driver	O
EINK-STH	Eink Start Pulse Source Driver	O
EINK-STV	Eink Start Pulse Gate Driver	O
EINK-LEH	Eink latch Enable Source Driver	O
EINK-OEH	Eink Output Enable Source Driver	O
EINK-MODE	Eink Output Mode Selection Gate Driver	O
EINK-D[15:0]	Eink Data Signal Source Driver	O

4.3.12 RGB

Table 4-53 RGB Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD0-D[23:0]	LCD Data Input/Output	I/O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-DE	LCD Data Output Enable	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O

Signal Name[1]	Description[2]	Type[3]
TCON-FSYNC[1:0]	Frame Sync for TCON and sensor	O

4.3.13 LVDS

Table 4-54 LVDS Signal Description

Signal Name[1]	Description[2]	Type[3]
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-CKP	LVDS1 Negative Port of Clock	AO
LVDS1-CKN	LVDS1 Positive Port of Clock	AO
VCC-LVDS	Power supply for LVDS	P

4.3.14 MIPI DSI

Table 4-55 MIPI DSI Signal Description

Signal Name[1]	Description[2]	Type[3]
DSI0-CKN	DSI0 Differential Clock Negative Signal	AO
DSI0-CKP	DSI0 Differential Clock Positive Signal	AO
DSI0-D3N	DSI0 Differential Data 3 Negative Signal	AO
DSI0-D2N	DSI0 Differential Data 2 Negative Signal	AO
DSI0-D1N	DSI0 Differential Data 1 Negative Signal	AO
DSI0-D0N	DSI0 Differential Data 0 Negative Signal	AI/O
DSI0-D3P	DSI0 Differential Data 3 Positive Signal	AO
DSI0-D2P	DSI0 Differential Data 2 Positive Signal	AO
DSI0-D1P	DSI0 Differential Data 1 Positive Signal	AO
DSI0-D0P	DSI0 Differential Data 0 Positive Signal	AI/O
DSI1-CKN	DSI1 Differential Clock Negative Signal	AO
DSI1-CKP	DSI1 Differential Clock Positive Signal	AO

Signal Name[1]	Description[2]	Type[3]
DSI1-D[3:0]N	DSI1 Differential Data[3:0] Negative Signal	AO
DSI1-D[3:0]P	DSI1 Differential Data[3:0] Positive Signal	AO
DSI-TRIG-LCD-TE1	Screen Trigger Signal	AI

4.3.15 HDMI

Table 4-56 HDMI Signal Description

Signal Name[1]	Description[2]	Type[3]
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HSCL/HDMI-SCL	HDMI Serial Clock	OD
HSDA/HDMI-SDA	HDMI Serial Data	OD
HCEC/HDMI-CEC	HDMI Consumer Electronics Control	OD
HHPD	HDMI Hot Plug Detection Signal	AI
HREXT	HDMI Reference Resistance	AO
VCC18-HDMI	1.8V Analog Supply for HDMI IO	P
VDD08-HDMI	0.8V HDMI Digital Power Supply	P

4.3.16 MIPI CSI

Table 4-57 MIPI CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
MCSIA-D[3:0]N	MIPI CSI Controller A Data[3:0] Negative Signal	AI
MCSIA-D[3:0]P	MIPI CSI Controller A Data[3:0] Positive Signal	AI

Signal Name[1]	Description[2]	Type[3]
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D[3:0]N	MIPI CSI Controller B Data[3:0] Negative Signal	AI
MCSIB-D[3:0]P	MIPI CSI Controller B Data[3:0] Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D[1:0]N	MIPI CSI Controller C Data[1:0] Negative Signal	AI
MCSIC-D[1:0]P	MIPI CSI Controller C Data[1:0] Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
VCC-MCSI	Power supply for MIPI CSI	P

4.3.17 Parallel CSI

Table 4-58 Parallel CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
NCSI0-MCLK	Parallel CSI Master Clock	O
NCSI0-PCLK	Parallel CSI Pixel Clock	I
NCSI0-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI0-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI0-D[7:0]	Parallel CSI Data Bit	I
NCSI1-PCLK	Parallel CSI Master Clock	O
NCSI1-MCLK	Parallel CSI Pixel Clock	I
NCSI1-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI1-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI1-D[15:0]	Parallel CSI Data Bit	I
CSI0-XHS	Sensor External Hsync	I/O
CSI1-XHS	Sensor External Hsync	I/O

Signal Name[1]	Description[2]	Type[3]
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O

4.3.18 I2S/PCM

Table 4-59 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S1-LRCK	I2S1/PCM01Sample Rate Clock/Sync	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-DOUT[3:0]	I2S2/PCM2 Serial Data Output Channel [3:0]	O
I2S2-DIN[3:0]	I2S2/PCM2 Serial Data Input Channel [3:0]	I
I2S3-MCLK<MUX-HDMI-EDP>	I2S3 Master Clock	O
I2S3-BCLK<MUX-HDMI-EDP>	I2S3/PCM3 Bit Rate Clock	I/O
I2S3-LRCK<MUX-HDMI-EDP>	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-DIN[3:0]<MUX-HDMI-EDP>	I2S3/PCM3 Serial Data Output Channel [3:0]	O

Signal Name[1]	Description[2]	Type[3]
I2S3-DOUT[3:0]<MUX-HDMI-EDP>	I2S3/PCM3 Serial Data Input Channel [3:0]	I
I2S4-MCLK<MUX-EDP>	I2S4 Master Clock	O
I2S4-BCLK<MUX-EDP>	I2S4/PCM4 Bit Rate Clock	I/O
I2S4-LRCK<MUX-EDP>	I2S4/PCM4 Sample Rate Clock/Sync	I/O
I2S4-DIN[1:0]<MUX-EDP>	I2S4/PCM4 Serial Data Output Channel [1:0]	O
I2S4-DOUT[1:0]<MUX-EDP>	I2S4/PCM4 Serial Data Input Channel [1:0]	I

4.3.19 DMIC

Table 4-60 DMIC Signal Description

Signal Name[1]	Description[2]	Type[3]
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA[3:0]	Digital Microphone Data Input	I

4.3.20 OWA

Table 4-61 OWA Signal Description

Signal Name[1]	Description[2]	Type[3]
OWA0-IN	One Wire Audio Input	I
OWA0-OUT	One Wire Audio Output	O

4.3.21 USB2.0 DRD

Table 4-62 USB2.0 DRD Signal Description

Signal Name[1]	Description[2]	Type[3]
USB0-DM	USB0 Data Signal DM	AI/O
USB0-DP	USB0 Data Signal DP	AI/O

Signal Name[1]	Description[2]	Type[3]
USB0-REXT	USB0 External Reference Resistor	AI/O
VDD08-USB	0.8V Power Supply for USB0 and USB1 IO	P
VCC33-USB	3.3V Power Supply for USB0 and USB1 IO	P
VCC33-18-USB	3.3V/1.8V Power Supply for USB0 and USB1 IO	P

4.3.22 USB2.0 Host

Table 4-63 USB2.0 Host Signal Description

Signal Name[1]	Description[2]	Type[3]
USB1-DM	USB1 Data Signal DM	AI/O
USB1-DP	USB1 Data Signal DP	AI/O
USB1-REXT	USB2.0 External Reference Resistor	AI/O

4.3.23 USB2.0 PHY

Table 4-64 USB2.0 PHY Signal Description

Signal Name[1]	Description[2]	Type[3]
USB2-DM	USB2_U2 Data Signal DM	AI/O
USB2-DP	USB2_U2 Data Signal DP	AI/O
USB2-REXT	USB2_U2 External Reference Resistor	AI/O
VCC33-USB2-U2	3.3V Power Supply for USB2_U2 IO	P
VCC33-18-USB2-U2	3.3V/1.8V Power Supply for USB2_U2 IO	P

4.3.24 COMB0-PHY-SERDES

Table 4-65 COMB0-PHY-SERDES Signal Description

Signal Name[1]	Description[2]	Type[3]
COMB0-TX0P	COMB0 PHY Lane 0 differential Signal TX positive	AO
COMB0-TX0N	COMB0 PHY Lane 0 differential Signal TX negative	AO
COMB0-TX1P	COMB0 PHY Lane 1 differential Signal TX positive	AI/O
COMB0-TX1N	COMB0 PHY Lane 1 differential Signal TX negative	AI/O
COMB0-TX2P	COMB0 PHY Lane 2 differential Signal TX positive	AI/O
COMB0-TX2N	COMB0 PHY Lane 2 differential Signal TX negative	AI/O

Signal Name[1]	Description[2]	Type[3]
COMB0-TX3P	COMB0 PHY Lane 3 differential Signal TX positive	AO
COMB0-TX3N	COMB0 PHY Lane 3 differential Signal TX negative	AO
COMB0-REF-CLKP	COMB0 PHY differential Signal reference clock positive	AI/O
COMB0-REF-CLKN	COMB0 PHY differential Signal reference clock negative	AI/O
COMB0-CMN-REXT	COMB0 PHY PMA external calibration resistor	AI/O
AVDD-C-COMB0	Clean analog power for high speed clock applications	P
AVDD-D-COMB0	Analog power for non-high speed clock and digital applications	P
AVDD-H-COMB0	High voltage power for the bias and parts of the PLL	P

4.3.25 eDP1.4b/DP1.4 AUX PHY

Table 4-66 eDP1.4b/DP1.4 AUX PHY Signal Description

Signal Name[1]	Description[2]	Type[3]
EDP-AUXP	AUX Channel Positive Input/Output	AI/O
EDP-AUXN	AUX Channel Negative Input/Output	AI/O
AUX-HPD	AUX hot plug detect input signal	AI
AVDD-HPD-AUX	AUX HPD 3.3V high voltage power supply	P

4.3.26 COMB1-PHY-SERDES

Table 4-67 COMB1-PHY-SERDES Signal Description

Signal Name[1]	Description[2]	Type[3]
COMB1-TX0P	COMB1 PHY Lane 0 differential Signal TX positive	AO
COMB1-TX0N	COMB1 PHY Lane 0 differential Signal TX negative	AO
COMB1-RX0P	COMB1 PHY Lane 0 differential Signal RX positive	AI
COMB1-RX0N	COMB1 PHY Lane 0 differential Signal RX negative	AI
COMB1-REF-CLKP	COMB1 PHY differential Signal reference clock positive	AI/O
COMB1-REF-CLKN	COMB1 PHY differential Signal reference clock negative	AI/O
COMB1-REXT	COMB1 PHY PMA external calibration resistor	AI/O

4.3.27 PCIe3.0

Table 4-68 PCIe3.0 Signal Description

Signal Name[1]	Description[2]	Type[3]
PCIE-CLKREQN	PCIe Clock Request from PCIe Peripheral	I/O
PCIE-WAKEN	PCIe Wake Up	I/O
PCIE-PERSTN	PCIe Warm Reset	I/O

4.3.28 GMAC

Table 4-69 GMAC Signal Description

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXCK/RMII0-NULL	RGMII0 Receive Clock	I
RGMII0-TXCK/RMII0-TXCK	RGMII0/RMII0 50MHz Reference Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII0-CLKIN/RMII0-RXER	RGMII 125M Reference Clock Input/RMII0 Receive Error	I
RGMII0-RXCTL/RMII0-CRS-DV	RGMII0 Receive Control/RMII0 Carrier Sense Receive Data Valid	I
RGMII0-TXCTL/RMII0-TXEN	RGMII0 Transmit Control/RMII0 Transmit Enable	O
RGMII0-MDC	RGMII0 Management Data Clock	O
RGMII0-MDIO	RGMII0 Management Data Input/Output	I/O
RGMII0-EPHY-25/50M	GMAC PHY 25MHz or 50MHz Clock Output	O
RGMII0-RXD0/RMII0-RXD0	RGMII0/RMII0 Receive Data 0	I
RGMII0-RXD1/RMII0-RXD1	RGMII0/RMII0 Receive Data 1	I

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXD2/RMII0-NULL	RGMII0 Receive Data 2	I
RGMII0-RXD3/RMII0-NULL	RGMII0 Receive Data 3	I
RGMII0-TXD0/RMII0-TXD0	RGMII0/RMII0 Transmit Data 0	O
RGMII0-TXD1/RMII0-TXD1	RGMII0/RMII0 Transmit Data 1	O
RGMII0-TXD2/RMII0-NULL	RGMII0 Transmit Data 2	O
RGMII0-TXD3/RMII0-NULL	RGMII0 Transmit Data 3	O

4.3.29 PWM

Table 4-70 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM0-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O
PWM1-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O
S-PWM0-[9:0]	Pulse Width Modulation Output Channel [9:0]	I/O

4.3.30 SPI

Table 4-71 SPI Signal Description

Signal Name[1]	Description[2]	Type[3]
SPI0-CS[1:0]	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0-HOLD	SPI0 Hold Signal	I/O
SPI1-CS[1:0]	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active	I/O
SPI1-HOLD	SPI1 Hold Signal	I/O
SPI2-CS[3:0]	SPI2 Chip Select Signal, Low Active	I/O
SPI2-CLK	SPI2 Clock Signal	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI3-CS[1:0]	SPI3 Chip Select Signal, Low Active	I/O
SPI3-CLK	SPI3 Clock Signal	I/O
SPI3-MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3-MISO	SPI3 Master Data In, Slave Data Out	I/O
S-SPI0-CS0	S-SPI0 Chip Select Signal, Low Active	I/O
S-SPI0-CLK	S-SPI0 Clock Signal	I/O
S-SPI0-MOSI	S-SPI0 Master Data Out, Slave Data In	I/O
S-SPI0-MISO	S-SPI0 Master Data In, Slave Data Out	I/O

4.3.31 DBI

Table 4-72 DBI Signal Description

Signal Name[1]	Description[2]	Type[3]
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal	I/O
DBI-TE	Tearing Effect Input	I/O
DBI-DCX	DCX pin is the select output signal of data and command.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

4.3.32 UART

Table 4-73 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-TX	UART0 Data Transmitter	O
UART0-RX	UART0 Data Receiver	I
UART1-RTS	UART1 Data Request to Send	O
UART1-CTS	UART1 Data Clear to Send	I
UART1-TX	UART1 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART2-RTS	UART2 Data Request to Send	O
UART2-CTS	UART2 Data Clear to Send	I
UART2-TX	UART2 Data Transmitter	O
UART2-RX	UART2 Data Receiver	I
UART3-RTS	UART3 Data Request to Send	O
UART3-CTS	UART3 Data Clear to Send	I
UART3-TX	UART3 Data Transmitter	O
UART3-RX	UART3 Data Receiver	I
UART4-RTS	UART4 Data Request to Send	O
UART4-CTS	UART4 Data Clear to Send	I
UART4-TX	UART4 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART5-RTS	UART5 Data Request to Send	O
UART5-CTS	UART5 Data Clear to Send	I
UART5-TX	UART5 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I
UART6-RTS	UART6 Data Request to Send	O
UART6-CTS	UART6 Data Clear to Send	I
UART6-TX	UART6 Data Transmitter	O
UART6-RX	UART6 Data Receiver	I
UART6-DCD	UART6 Line State of Data Carrier Detect	I
UART6-DSR	UART6 Line State of Data Set Ready	I

Signal Name[1]	Description[2]	Type[3]
UART6-DTR	UART6 Data Terminal Ready	O
UART6-RI	UART6 Line State of Ring Indicator	I
S-UART0-TX	S-UART0 Data Transmitter	O
S-UART0-RX	S-UART0 Data Receiver	I
S-UART1-TX	S-UART1 Data Transmitter	O
S-UART1-RX	S-UART1 Data Receiver	I

4.3.33 TWI

Table 4-74 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI[12:0]-SCK	TWI0 Serial Clock Signal	I/O
TWI[12:0]-SDA	TWI0 Serial Data Signal	I/O
S-TWI[2:0]-SDA	S-TWI0 Serial Data Signal	I/O
S-TWI[2:0]-SCK	S-TWI0 Serial Clock Signal	I/O

4.3.34 GPADC

Table 4-75 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
BOOT-SEL-GPADC0-0	General Purpose ADC Input Channel 0 for BOOT SELECT	AI
BOARD-ID-GPADC0-1	General Purpose ADC Input Channel 1 for BOARD ID	AI
BOARD-ID-GPADC0-2	General Purpose ADC Input Channel 2 for BOARD ID	AI
GPADC0-3	General Purpose ADC Input Channel 3	AI
GPADC0-4	General Purpose ADC Input Channel 4	AI
GPADC0-5	General Purpose ADC Input Channel 5	AI
GPADC0-6	General Purpose ADC Input Channel 6	AI
VCM-ADC	GPADC Reference Voltage 0.9V	AI
VREFP-ADC	GPADC Reference Voltage 1.8V	P
VREFN-ADC	GPADC Reference Ground	G

4.3.35 LRADC

Table 4-76 LRADC Signal Description

Signal Name[1]	Description[2]	Type[3]
LRADC0-0	Low Rate ADC	AI

4.3.36 LEDC

Table 4-77 LEDC Signal Description

Signal Name[1]	Description[2]	Type[3]
LEDC	Intelligent Control LED Signal Output	O

4.3.37 IR-RX

Table 4-78 IR-RX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-RX	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared receiver	I

4.3.38 IR-TX

Table 4-79 IR-TX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-TX	Consumer Infrared Transmitter	O

4.3.39 IBIAS

Table 4-80 IBIAS Signal Description

Signal Name[1]	Description[2]	Type[3]
VCC-ADC	Power Supply for GPADC	P
AGND	Analog Ground	G

4.3.40 Power

Table 4-81 Power Signal Description

Signal Name[1]	Description[2]	Type[3]
VDD-CPUS	Power Supply for CPUS	P
VDD-CPUB	Power Supply for CPUB	P

Signal Name[1]	Description[2]	Type[3]
VDD-CPUBFB	CPUB Power Feedback Signal	P
VDD-CPUL	Power Supply for CPUL	P
VDD-CPULFB	CPUL Power Feedback Signal	P
VDD-GPU	Power Supply for GPU	P
VDD-GPUFB	GPU Power Feedback Signal	P
VDD-VE	Power Supply for VE	P
VDD-SYS	Power Supply for System	P
VCC-PC	Power Supply for PC	P
VCC-PD	Power Supply for PD	P
VCC-PE	Power Supply for PE	P
VCC18-PF	1.8 V Power Supply for PF	P
VCC-PG	Power Supply for PG	P
VCC-PH	Power Supply for PH	P
VCC-PJ	Power Supply for PJ	P
VCC-PK	Power Supply for PK	P
VCC-PL	Power Supply for PL	P
VCC-PM	Power Supply for PM	P
VCC-IO	Power Supply for IO 3.3V	P

4.3.41 Interrupt

Table 4-82 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PB-EINT[10:0]	Port B Interrupt	I
PC-EINT[16:0]	Port C Interrupt	I
PD-EINT[23:0]	Port D Interrupt	I
PE-EINT[15:0]	Port E Interrupt	I
PF-EINT[6:0]	Port F Interrupt	I
PG-EINT[14:0]	Port G Interrupt	I
PH-EINT[16:0]	Port H Interrupt	I
PJ-EINT[27:22]	Port J Interrupt	I
PK-EINT[25:0]	Port K Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PL-EINT[13:0]	Port L Interrupt	I
PM-EINT[5:0]	Port M Interrupt	I

4.3.42 CLK-FANOUT

Table 4-83 CLK-FANOUT Signal Description

Signal Name[1]	Description[2]	Type[3]
CLK-FANOUT0	Clock Fanout 0	O
CLK-FANOUT1	Clock Fanout 1	O
CLK-FANOUT2	Clock Fanout 2	O
CLK-FANOUT3	Clock Fanout 3	O

4.3.43 JTAG

Table 4-84 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
JTAG-MS	Arm® CPU JTAG Mode Selection	I
JTAG-CK	Arm® CPU JTAG Clock Signal	I
JTAG-DO	Arm® CPU JTAG Data Output	O
JTAG-DI	Arm® CPU JTAG Data Input	I
S-RJTAG-MS	RISC-V JTAG Mode Select	I
S-RJTAG-CK	RISC-V JTAG Clock Signal	I
S-JTAG-MS	CPUS JTAG Mode Selection	I
S-JTAG-CK	CPUS JTAG Clock Signal	I
S-JTAG-DO	CPUS JTAG Data Output	O
S-JTAG-DI	CPUS JTAG Data Input	I

5 Electrical characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature indicates the temperature of the surrounding environment.
- Junction Temperature indicates the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature indicates the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature indicates the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 5.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Signal Name	Description	Min(1)	Max(1)	Unit
VDD-CPUS	Power Supply for CPUS	-0.3	1.2	V
VDD-CPUB	Power Supply for CPUB	-0.3	1.2	V
VDD-CPUL	Power Supply for CPUL	-0.3	1.2	V
VDD-GPU	Power Supply for GPU	-0.3	1.2	V
VDD-SYS	Power Supply for System	-0.3	1.1	V
VCC-DRAM	Power Supply for DRAM PHY	-0.3	1.4	V
VCC-DRAML	Power Supply for DRAM IO	0.27	1.1	V
VDD-DRAM	Power Supply for DRAM CORE&PHY	-0.3	1.1	V
VDD18-DRAM	1.8 V Power Supply for DRAM PHY PLL	1.674	1.98	V
VCC-EFUSE	Power Supply for eFuse	-0.3	2.1	V
VCC-RTC	Power Supply for RTC	-0.3	2.1	V
RTC-VIO	Digital Power Bypass for RTC	-0.3	1.2	V
VCC-DCXO	Digital Compensated Crystal Oscillator power Supply	-0.3	2.1	V
VCC-DCXO1	DCXO Reference Voltage 1	-0.3	2.1	V
VCC-DCXO2	DCXO Reference Voltage 2	-0.3	2.1	V
VDD-UFS	Power Supply for UFS controller	0.744	0.88	V
VCC12-UFS	Power Supply for UFS 3.x CORE	-0.3	1.2	V
VCC-UFS	Power Supply for UFS 3.x IO	-0.3	2.5	V

Signal Name	Description	Min(1)	Max(1)	Unit
VCC-LVDS	Power Supply for LVDS	-0.3	2.1	V
VCC18-HDMI	1.8 V Analog Supply for HDMI IO	-0.3	2.1	V
VDD08-HDMI	0.8 V HDMI Digital power Supply	-0.3	1.2	V
VCC-MCSI	Power Supply for MCSI	-0.3	2.1	V
VCC33-USB2-U2	3.3 V Power Supply for USB2_U2 IO	-0.3	3.63	V
VCC33-18-USB2-U2	3.3 V/1.8 V Power Supply for USB2_U2 IO	-0.3	3.63	V
VDD08-USB	0.8V Power Supply for USB0 and USB1 IO	0.744	0.88	V
VCC33-USB	3.3V Power Supply for USB0 and USB1 IO	-0.3	3.63	V
VCC33-18-USB	3.3V/1.8V Power Supply for USB0 and USB1 IO	-0.3	3.63	V
AVDD-C-COMB0	Clean Analog Power for High Speed Clock Applications	-0.3	2.1	V
AVDD-HPD-AUX	AUX HPD 3.3V High Voltage Power Supply	-0.3	3.63	V
AVDD-D-COMB0	Power Supply for COMBO AVDD DATA	0.744	0.88	V
AVDD-H-COMB0	Power Supply for COMBO AVDD High Voltage	-0.3	2.1	V
VREFP-ADC	GPADC Reference Voltage	-0.3	2.1	V
VCC-ADC	Power Supply for GPADC	-0.3	2.1	V
VDD-VE	Power Supply for VE	0.744	1.1	V
VCC-PC	Power Supply for PC	-0.3	3.63	V
VCC-PD	Power Supply for PD	-0.3	3.63	V
VCC-PE	Power Supply for PE	-0.3	3.63	V
VCC18-PF	1.8 V Power Supply for PF	-0.3	2.1	V
VCC-PG	Power Supply for PG	-0.3	3.63	V
VCC-PH	Power Supply for PH	-0.3	3.63	V
VCC-PJ	Power Supply for PJ	-0.3	3.63	V
VCC-PK	Power Supply for PK	-0.3	3.63	V
VCC-PL	Power Supply for PL	-0.3	3.63	V
VCC-PM	Power Supply for PM	-0.3	3.63	V
VCC-IO	Power Supply for IO 3.3V	-0.3	3.63	V

Signal Name	Description	Min(1)	Max(1)	Unit
V_{ESD}(2)	Human Body Model (HBM)(3)	±2000		V
	Charged Device Model (CDM)(4)	±500		V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(6)	Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) is to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2023.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2022.

(5) Based on JESD78F, each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78F, each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

The following table describes operating conditions of the device.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Signal Name	Description	Min	Typ	Max	Unit
VDD-CPUS	Power Supply for CPUS	TBD	0.8	TBD	V
VDD-CPUB	Power Supply for CPUB	TBD	0.8	TBD	V
VDD-CPUL	Power Supply for CPUL	TBD	0.8	TBD	V
VDD-GPU	Power Supply for GPU	TBD	0.8	TBD	V
VDD-SYS	Power Supply for System	TBD	0.8	TBD	V
VCC-DRAM	Power Supply for LPDDR4/4X PHY	TBD	1.1	TBD	V
	Power Supply for LPDDR5 PHY	TBD	1.05	TBD	V
VCC-DRAML	Power Supply for LPDDR4 IO	TBD	0.8	TBD	V

Signal Name	Description	Min	Typ	Max	Unit
	Power Supply for LPDDR4X IO	TBD	0.6	TBD	V
	Power Supply for LPDDR5 IO	TBD	0.5	TBD	V
VDD-DRAM	Power Supply for DRAM CORE&PHY	TBD	0.8	TBD	V
VDD18-DRAM	1.8 V Power Supply for DRAM PHY PLL	TBD	1.8	TBD	V
VCC-EFUSE	Power Supply for eFuse	TBD	1.8	TBD	V
VCC-RTC	Power Supply for RTC	TBD	1.8	TBD	V
RTC-VIO	Digital Power Bypass for RTC	TBD	0.9	TBD	V
VCC-DCXO	Digital Compensated Crystal Oscillator power Supply	TBD	1.8	TBD	V
VCC-DCXO1	DCXO Reference Voltage 1	TBD	1.8	TBD	V
VCC-DCXO2	DCXO Reference Voltage 2	TBD	1.8	TBD	V
VDD-UFS	Power Supply for UFS controller	TBD	0.8	TBD	V
VCC12-UFS	Power Supply for UFS 3.x CORE	TBD	1.2	TBD	V
VCC-UFS	Power Supply for UFS 3.x IO	TBD	2.5	TBD	V
VCC-LVDS	Power Supply for LVDS	TBD	1.8	TBD	V
VCC18-HDMI	1.8V Analog Supply for HDMI IO	TBD	1.8	TBD	V
VDD08-HDMI	0.8V HDMI Digital power Supply	TBD	0.8	TBD	V
VCC-MCSI	Power Supply for MCSI	TBD	1.8	TBD	V
VCC33-USB2-U2	3.3V Power Supply for USB3.1 DRD IO	TBD	3.3	TBD	V
VCC33-18-USB2-U2	3.3V/1.8V Power Supply for USB3.1 DRD IO	TBD	3.3	TBD	V
VDD08-USB	0.8V Power Supply for USB2.0 DRD IO and USB2.0 Host IO	TBD	0.8	TBD	V
VCC33-USB	3.3V Power Supply for USB2.0 DRD and USB2.0 Host IO	TBD	3.3	TBD	V
VCC33-18-USB	3.3V/1.8V Power Supply for USB2.0 DRD and USB2.0 Host IO	TBD	3.3	TBD	V
AVDD-C-COMB0	Clean Analog Power for High Speed Clock Applications	TBD	0.8	TBD	V

Signal Name	Description	Min	Typ	Max	Unit
AVDD-HPD-AUX	AUX HPD 3.3V High Voltage Power Supply	TBD	3.3	TBD	V
AVDD-D-COMB0	Power Supply for COMBO AVDD DATA	TBD	0.8	TBD	V
AVDD-H-COMB0	Power Supply for COMBO AVDD High Voltage	TBD	1.8	TBD	V
VREFP-ADC	GPADC Reference Voltage	TBD	1.8	TBD	V
VCC-ADC	Power Supply for GPADC	TBD	1.8	TBD	V
VDD-VE	Power Supply for VE	TBD	0.8	TBD	V
VCC-PC	Digital GPIO C Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PD	Digital GPIO D Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PE	Digital GPIO E Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC18-PF	1.8 V Power Supply for PF	TBD	1.8	TBD	V
VCC-PG	Digital GPIO G Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PH	Digital GPIO H Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PJ	Digital GPIO J Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PK	Digital GPIO K Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PL	Digital GPIO L Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V
VCC-PM	Digital GPIO M Power 3.3V voltage 1.8V voltage	TBD	3.3	TBD	V
		TBD	1.8	TBD	V

Signal Name	Description	Min	Typ	Max	Unit
VCC-IO	Power Supply for VCCIO	TBD	3.3	TBD	V

5.4 GPIO Electrical Characteristics

Table 5-3 summarizes the GPIO electrical characteristics of the device.

Table 5-3 GPIO Electrical Characteristics

(VCC-IO/VCC-PC/VCC-PD/VCC-PE/VCC18-PF/VCC-PG/VCC-PH/VCC-PJ/VCC-PK/VCC-PL/VCC-PM)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-level Input Voltage		0.7*VCC	-	1.1*VCC	V
V_{IL}	Low-level Input Voltage		-0.3	-	0.3*VCC	V
R_{PU}	Output Pull-up Resistance	PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF1, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R_{PD}	Output Pull-down Resistance	PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF1, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I_{IH}	High-level Input Current		-	-	10	uA
I_{IL}	Low-level Input Current		-	-	10	uA
V_{OH}	High-level Output Voltage		VCC-IO – 0.3	-	VCC-IO	V
V_{OL}	Low-level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-state Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

5.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 5-1 SMHC Voltage Waveform

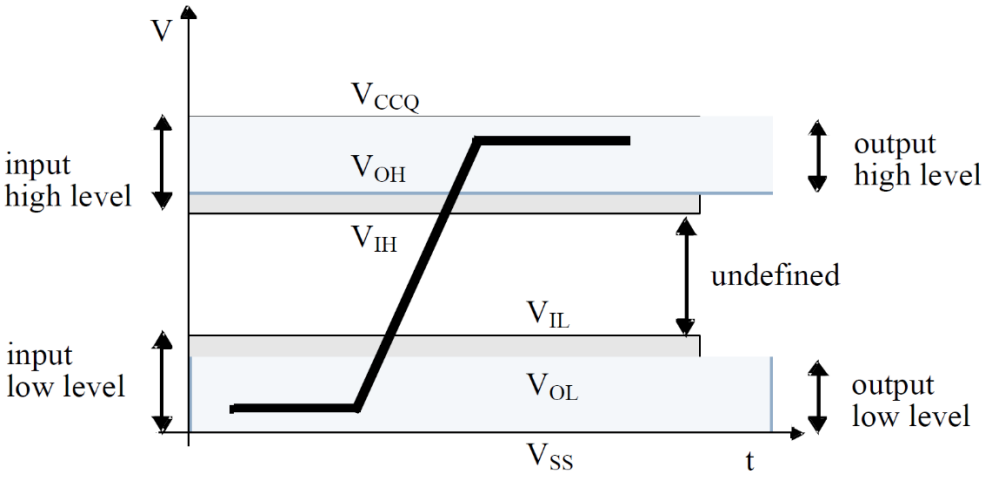


Table 5-4 shows 3.3 V SMHC electrical parameters.

Table 5-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8 V SMHC electrical parameters.

Table 5-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.65 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V

Symbol	Parameter	Min	Typ	Max	Unit
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6 GPADC Electrical Characteristics

Table 5-6 lists the GPADC electrical characteristics.

Table 5-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	VCC-ADC	V
Sampling Rate	-	-	1	MHz
Conversion Time	-	13	-	ADC Clock Cycles

5.7 LRADC Electrical Characteristics

The following table lists the LRADC electrical characteristics.

Table 5-7 LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Power Supply	-	-	VCC-ADC	V
Power Reference	-	1.35	-	V
ADC Resolution	-	6	-	bits
Full-scale Input Range	1		LEVELB(1)	V
Sampling Rate	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.286 V. For details, see the register description of LRADC in *A733_User_Manual*.				

5.8 External Clock Source Electrical Characteristics

5.8.1 High-frequency Crystal/Ceramic Resonator Characteristics

The high-frequency external clock can be supplied with a 26 MHz crystal resonator (oscillation mode). The 26 MHz crystal resonator provides 26 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-8 High-frequency 26 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X26M_IN}	Crystal parallel resonance frequency	-	26	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

(1) The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (26 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.

(2) The 6.5 pF is only a simulation value. The crystal shunt capacitance (C0) is given by the crystal manufacturer.

Table 5-9 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The sizes of C_1 and C_2 are usually the same.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

5.8.2 Low-frequency Crystal/Ceramic Resonator Characteristics

This device contains an RC oscillation circuit that generates a 32.768 kHz clock; meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be

omitted and the internal RC oscillation circuit can be adopted. In addition, the relevant clock configuration needs to be turned on by the software.

This device also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-10 Low-frequency 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C (1)	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	1.1	-	pF

(1) This device has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.

(2) The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

5.9 Interface Timing Characteristics

5.9.1 Raw NAND Flash Interface Timing

Figure 5-2 Conventional Serial Access Cycle Timing (SAM0)

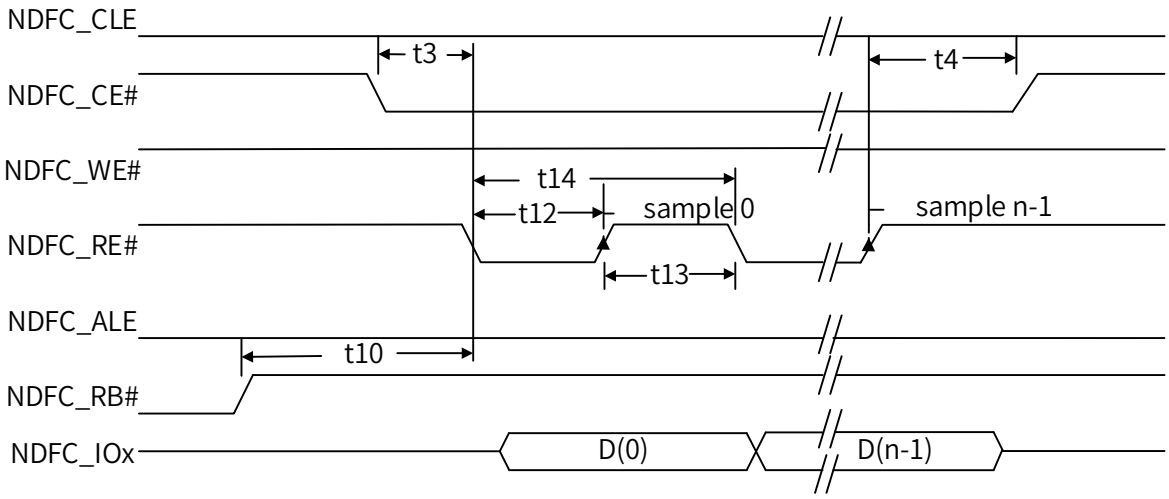


Figure 5-3 EDO Type Serial Access after Read Cycle Timing (SAM1)

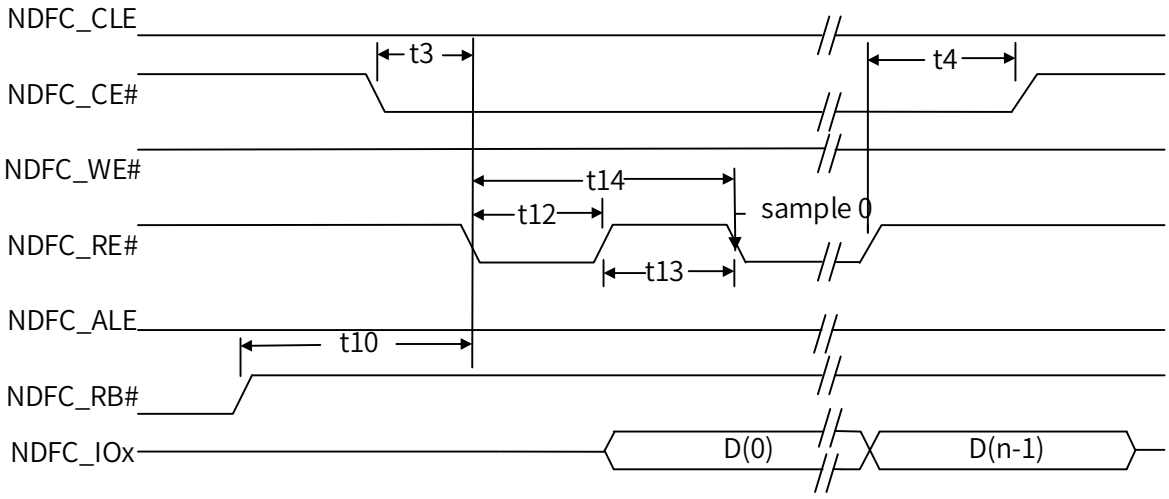


Figure 5-4 Extending EDO Type Serial Access Mode Timing (SAM2)

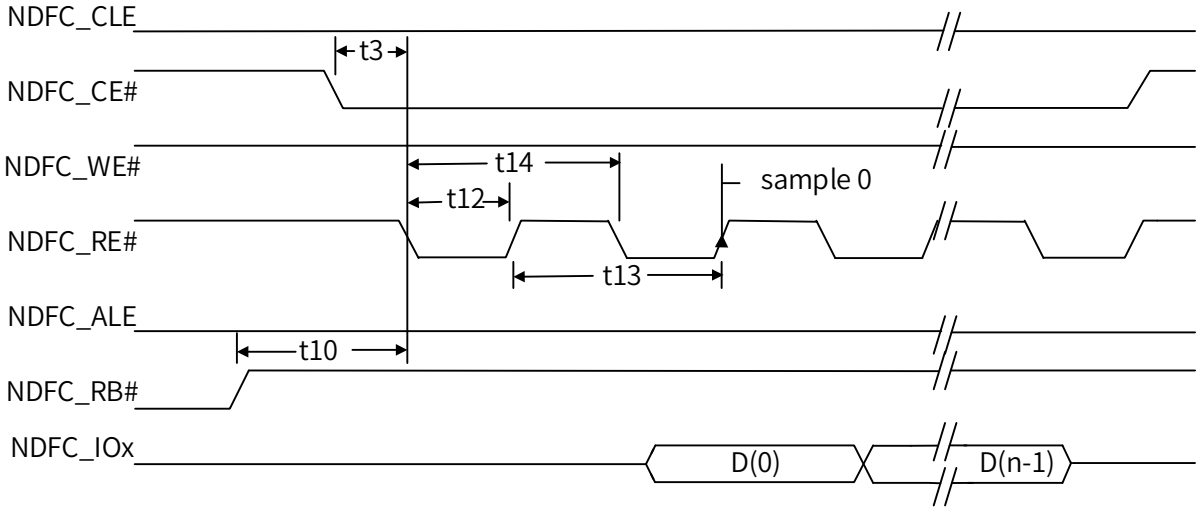


Figure 5-5 Command Latch Cycle Timing

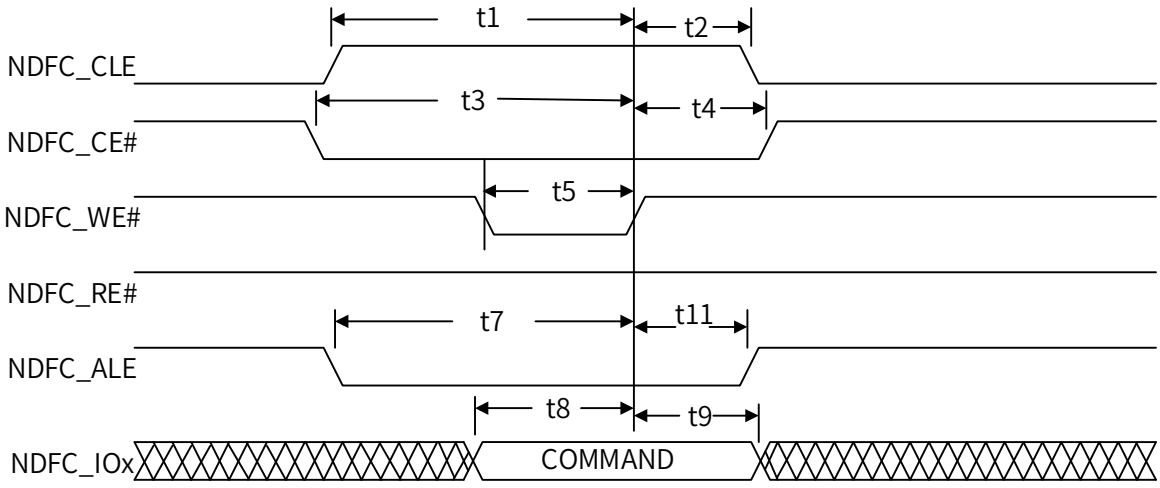


Figure 5-6 Address Latch Cycle Timing

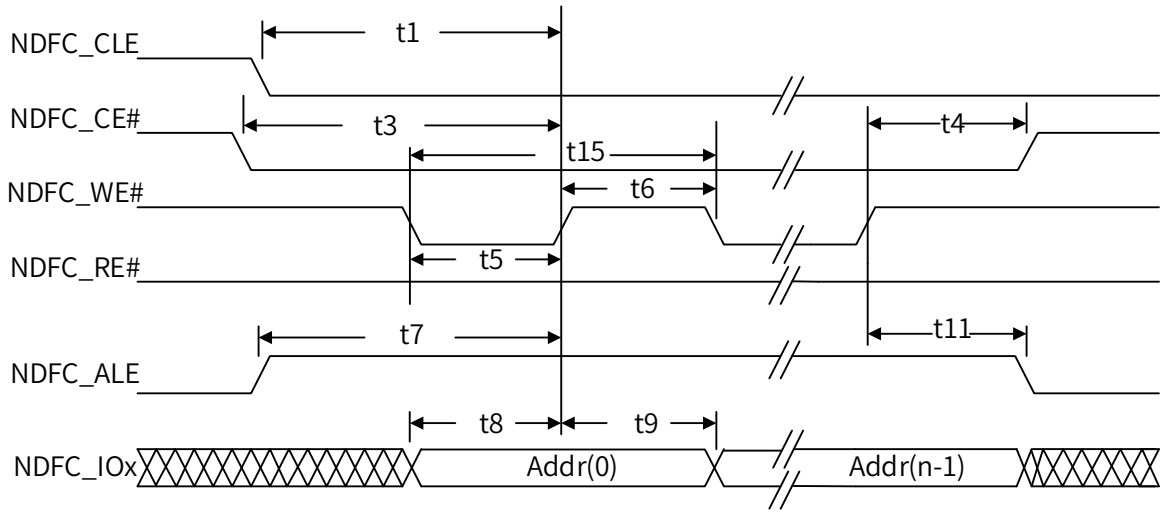


Figure 5-7 Write Data to Flash Cycle Timing

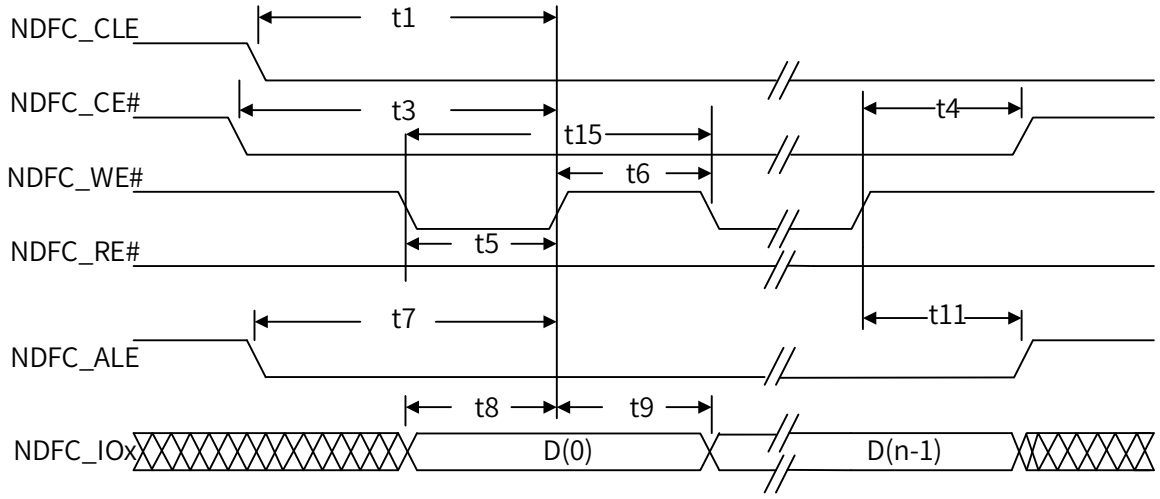


Figure 5-8 Waiting R/B# Ready Timing

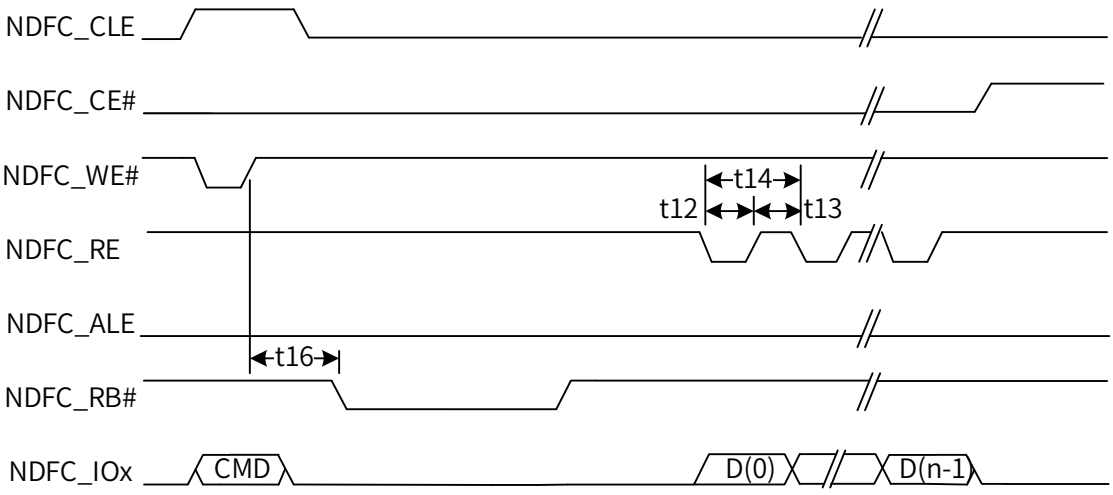


Figure 5-9 WE# High to RE# Low Timing

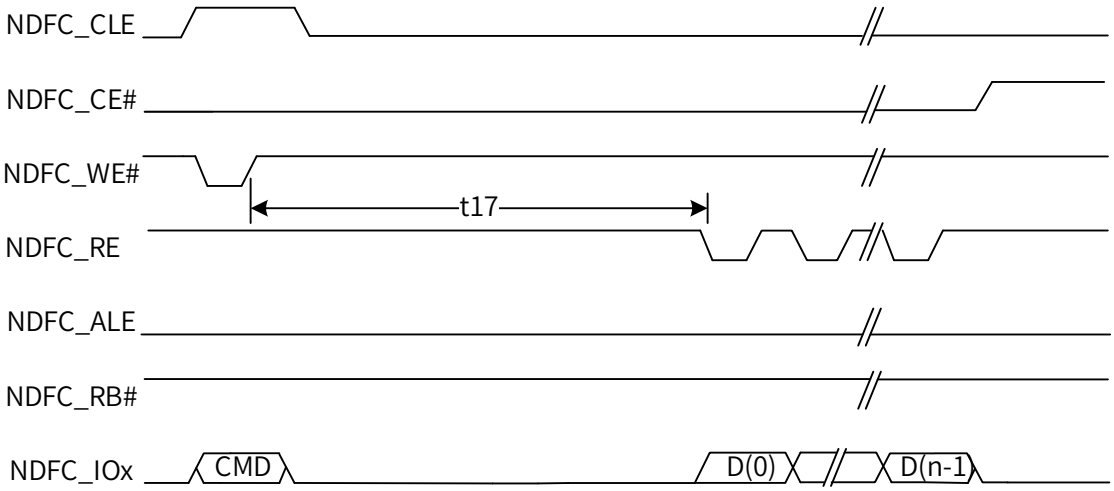


Figure 5-10 RE# High to WE# Low Timing

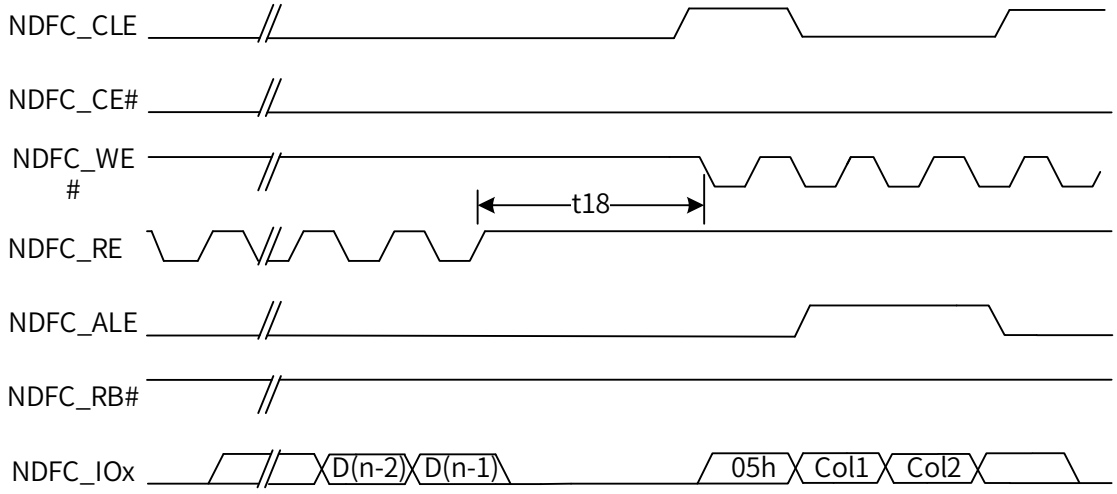


Figure 5-11 Address to Data Loading Timing

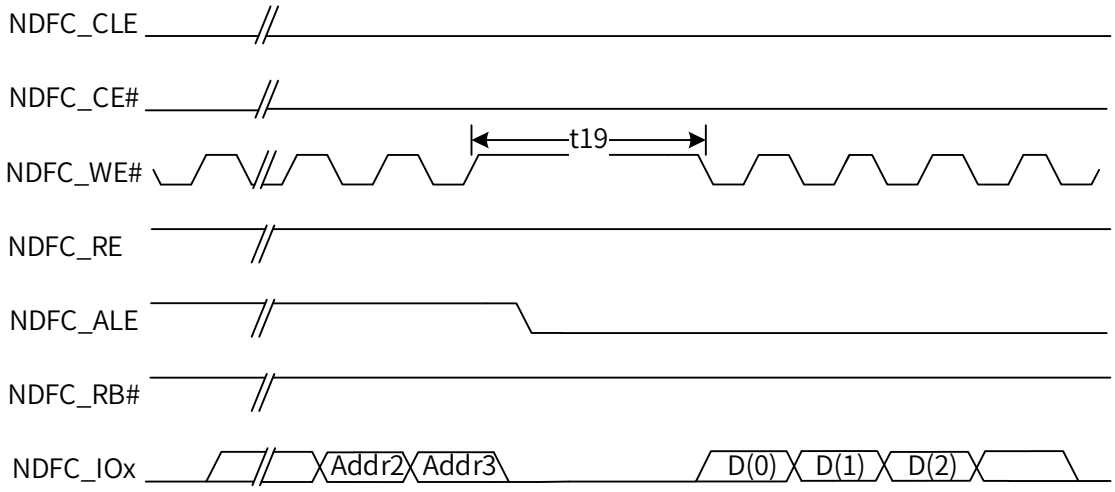


Table 5-11 Raw NAND Flash Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
NDFC_CLE setup time	t1	-	2T	-	ns
NDFC_CLE hold time	t2	-	2T	-	ns
NDFC_CE setup time	t3	-	2T	-	ns
NDFC_CE hold time	t4	-	2T	-	ns
NDFC_WE# pulse width	t5	-	T(1)	-	ns
NDFC_WE# hold time	t6	-	T	-	ns
NDFC_ALE setup time	t7	-	2T	-	ns
Data setup time	t8	-	T	-	ns
Data hold time	t9	-	T	-	ns
Ready to NDFC_RE# low	t10	-	3T	-	ns
NDFC_ALE hold time	t11	-	2T	-	ns
NDFC_RE# pulse width	t12	-	T	-	ns
NDFC_RE# hold time	t13	-	T	-	ns
Read cycle time	t14	-	2T	-	ns
Write cycle time	t15	-	2T	-	ns
NDFC_WE# high to R/B# busy	t16	-	T_WB(2)	-	ns
NDFC_WE# high to NDFC_RE# low	t17	-	T_WHR(3)	-	ns
NDFC_RE# high to NDFC_WE# low	t18	-	T_RHW(4)	-	ns
Address to Data Loading time	t19	-	T_ADL(5)	-	ns

Note:

1. (1) T is the cycle of internal clock.
2. (2), (3), (4), and (5) are configurable in NAND Flash controller, as shown below.

The value of T_WB could be 14*2T/22*2T/30*2T/38*2T.

The value of T_WHR could be 8*2T/16*2T/24*2T/32*2T.

The value of T_RHW could be 4*2T/8*2T/12*2T/20*2T.

The value of T_ADL could be 0*2T/8*2T/16*2T/24*2T.

5.9.2 SMHC Interface Timing

5.9.2.1 HS-SDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

Figure 5-12 SMHC HS-SDR Mode Output Timing Diagram

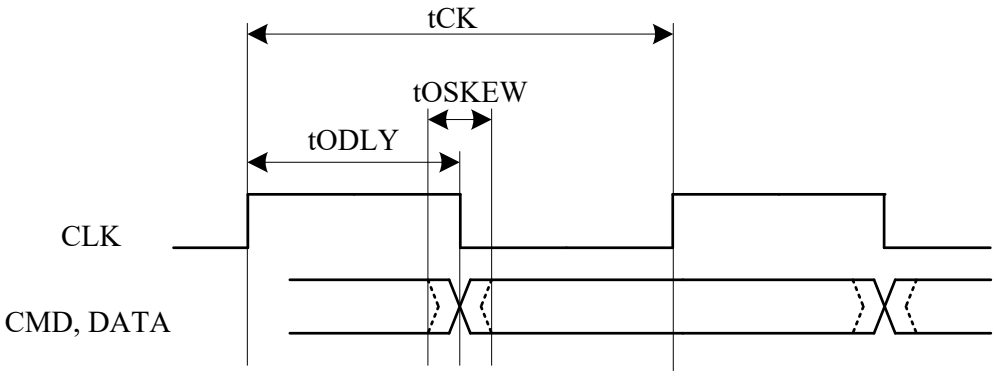


Table 5-12 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
Note: (1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-13 SMHC HS-SDR Mode Input Timing Diagram

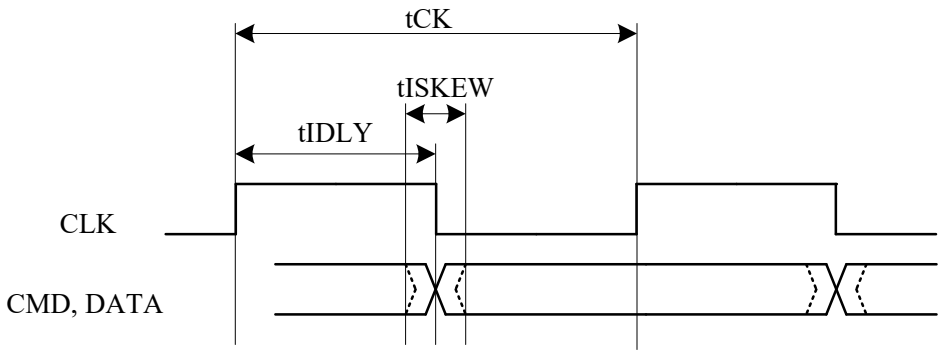


Table 5-13 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.9.2.2 HS-DDR Mode

Figure 5-14 SMHC HS-DDR Mode Output Timing Diagram

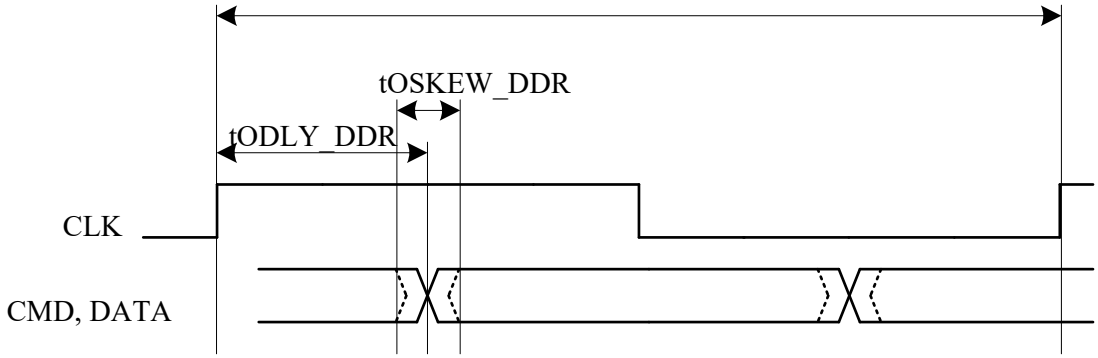


Table 5-14 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-15 SMHC HS-DDR Mode Input Timing Diagram

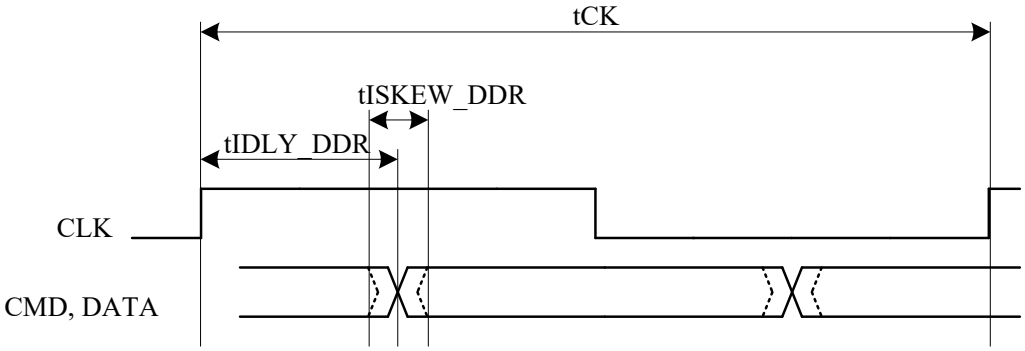


Table 5-15 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW-DDR	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.9.2.3 HS200/SDR104 Mode

Figure 5-16 SMHC HS200/SDR104 Mode Host Output and Device Input Timing Diagram

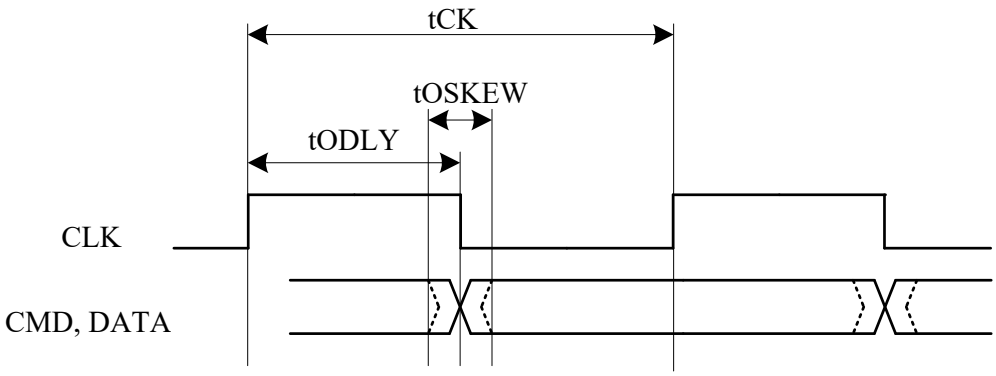


Table 5-16 SMHC HS200/SDR104 Mode Host Output and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	-	-	200	MHz
Duty Cycle	DC	45	50	55	%
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI
Host Output CMD, DATA (referenced to CLK)					
Host CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Host Data output delay skew time	tOSKEW	-	-	0.884	ns
Note: (1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.					

Figure 5-17 SMHC HS200/SDR104 Mode Host Input and Device Output Timing Diagram

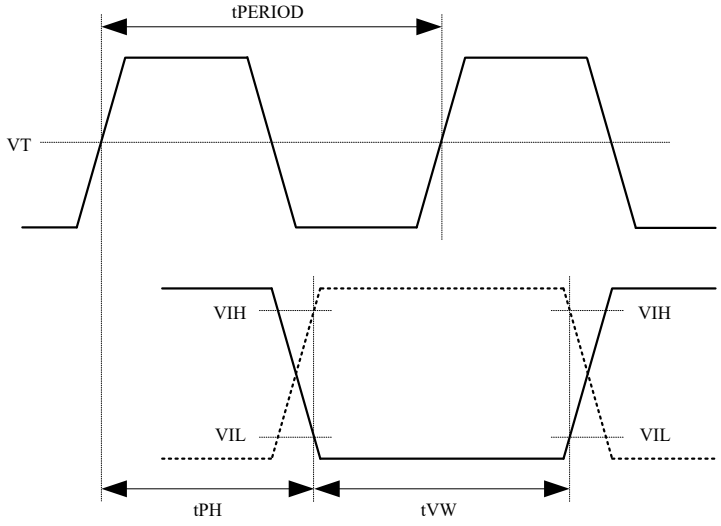


Table 5-17 SMHC HS200 Mode Host Input and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	5	-	-	ns	Max: 200 MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Host Input CMD, DATA (referenced to CLK)						
Device Output delay	tPH	0	-	2	UI	
Device Output delay variation due to temperature change after tuning	dPH	-350(3)	-	1550(4)	ps	
Device CMD, Data valid window	tVW	0.575	-	-	UI	

Note:

(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.

(2) The driver strength level of GPIO is 3 for test.

(3) Temperature variation: -20 °C.

(4) Temperature variation: 90 °C.

5.9.2.4 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 5-18 SMHC HS400 Mode Output Timing Diagram

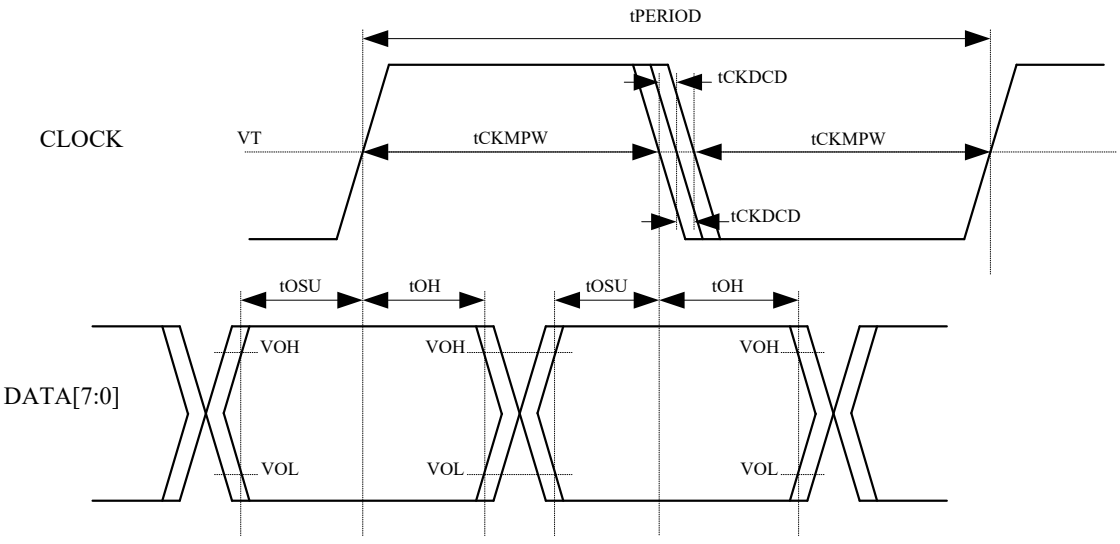


Table 5-18 SMHC HS400 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	5	-	-	ns	Max: 200 MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA (referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	
Note: (1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

Figure 5-19 SMHC HS400 Mode Input Timing Diagram

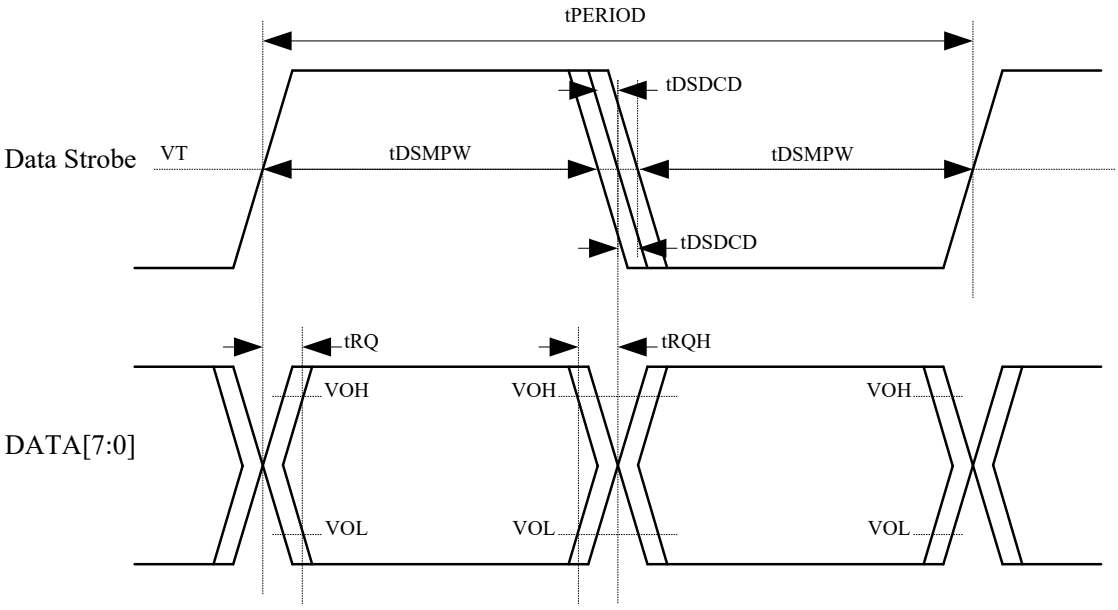


Table 5-19 SMHC HS400 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS (Data Strobe)						
DS period	tPERIOD	5	-	-	ns	Max: 200 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Input DATA (referenced to DS)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
Note: (1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

5.9.3 LCD Interface Timing

Figure 5-20 HV_IF Vertical Timing

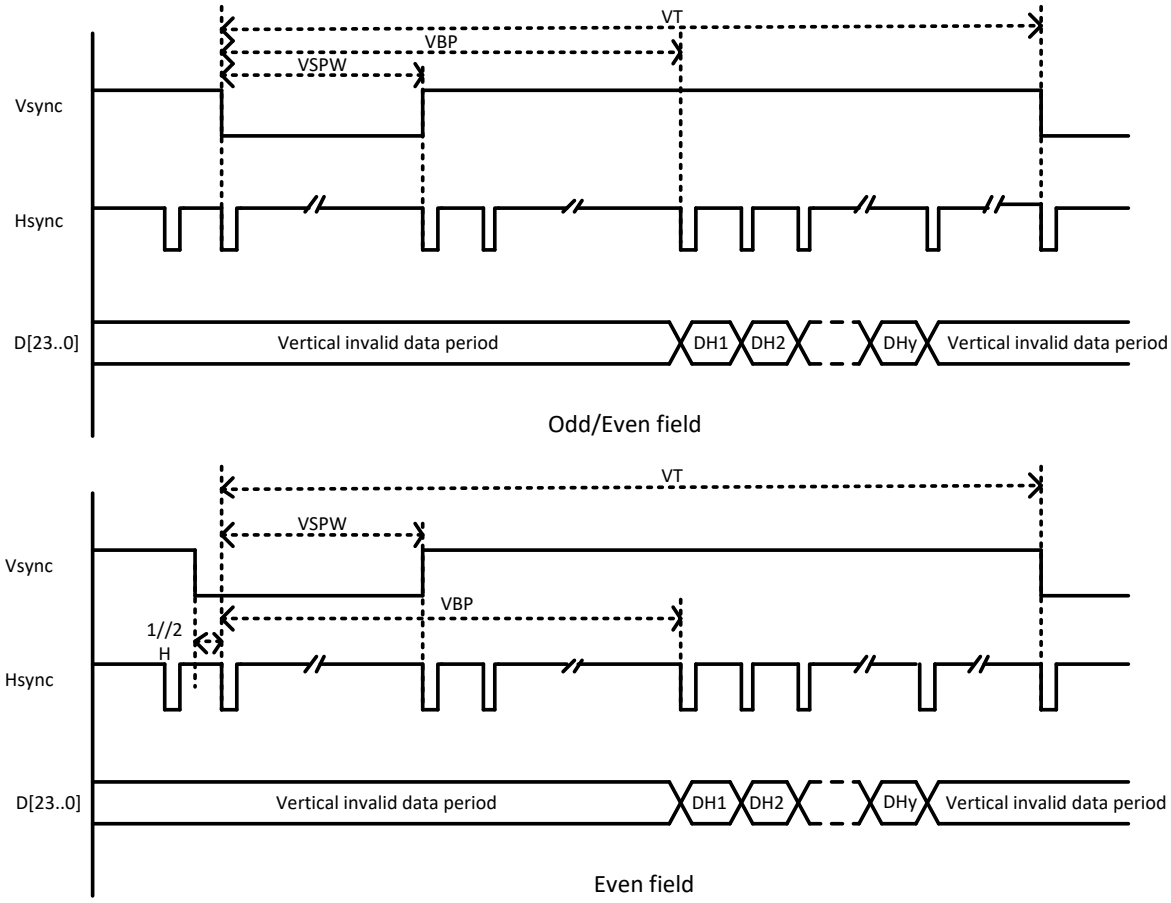
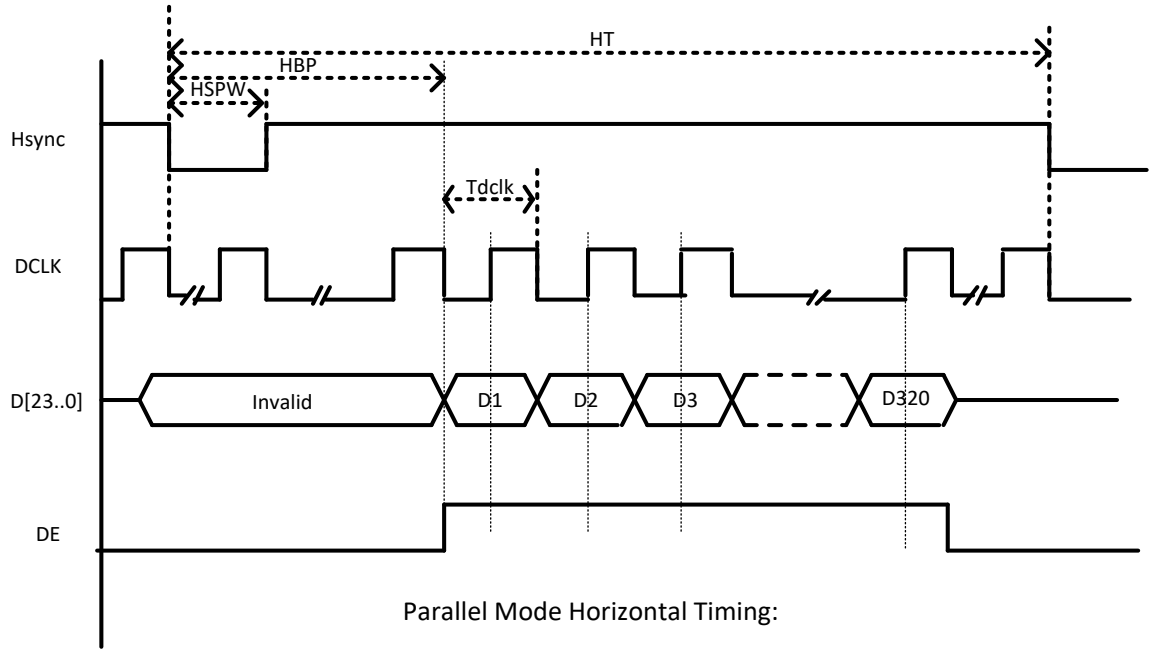
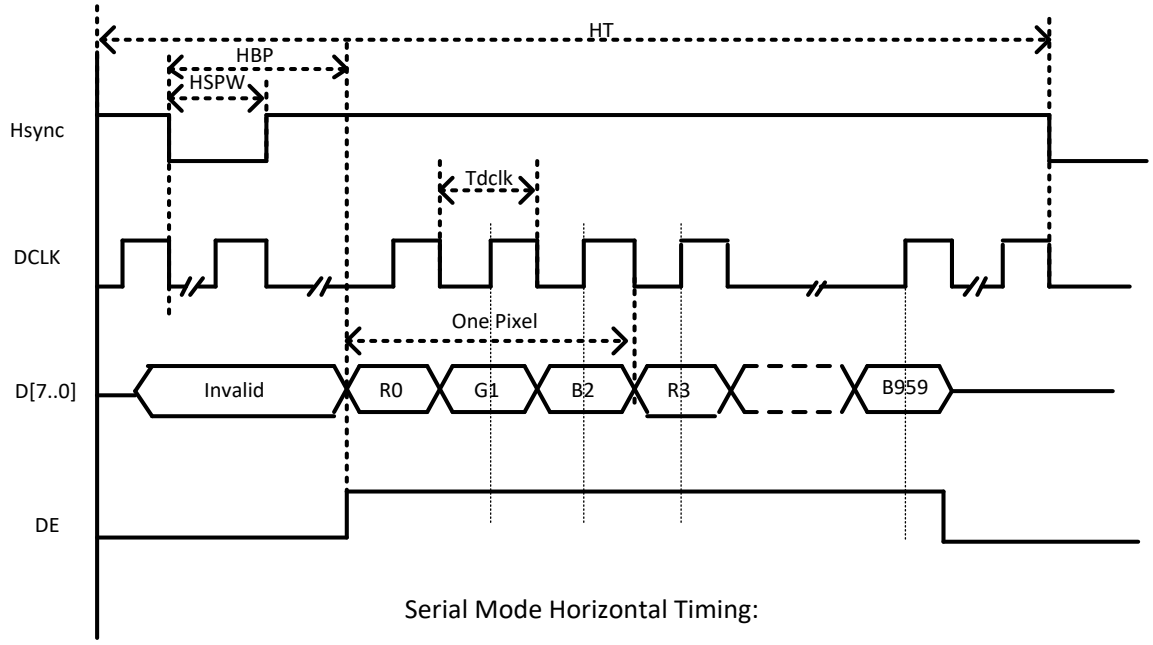


Figure 5-21 HV_IF Horizontal Timing



Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:

Table 5-20 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT
Note: (1) Vsync: Vertical sync, indicates one new frame. (2) Hsync: Horizontal sync, indicate one new scan line. (3) DCLK: Dot clock, pixel data are sync by this clock. (4) DE: LCD data enable. (5) D[23..0]: 24Bit RGB/YUV output from input FIFO for panel.					

5.9.4 Parallel CSI Interface Timing

Figure 5-22 Parallel CSI Data Sample Timing

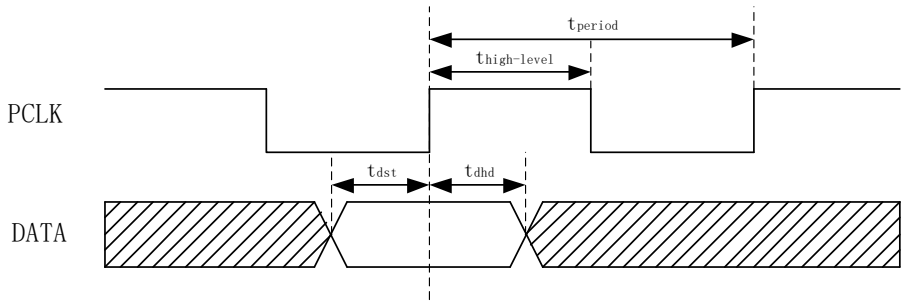


Table 5-21 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.9.5 MIPI CSI Interface Timing

Figure 5-23 MIPI CSI Interface Timing

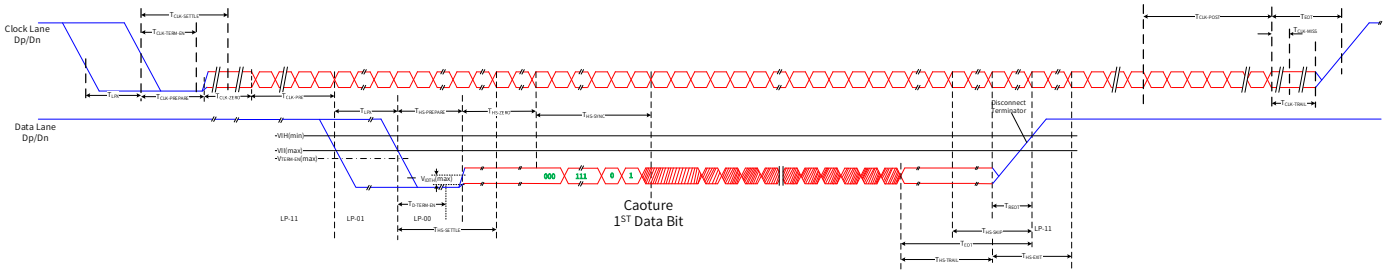


Table 5-22 MIPI CSI Interface Timing Constants

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns	5
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	5
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns	6, 7
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	6
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns + 4*UI		6
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start			105ns + n*12*UI		3, 5

Parameter	Description	Min	Typ	Max	Unit	Notes
	of the LP-11 state following a HS burst.					
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85ns + 6*UI	ns	5
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns	5
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI		145ns + 10*UI	ns	6
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40			ns	6
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60ns + n*4*UI)			ns	2, 3, 5
T_{INIT}		100			ns	5
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	4, 5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	ns	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns	5

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns	5
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2*T_{LPX}$	ns	5
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5

NOTE

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then max (a, b) = a otherwise max (a, b) = b.
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.
4. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter.
6. Receiver-specific parameter.
7. The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

5.9.6 MIPI DPHY Interface Timing

Figure 5-24 MIPI DPHY Timing

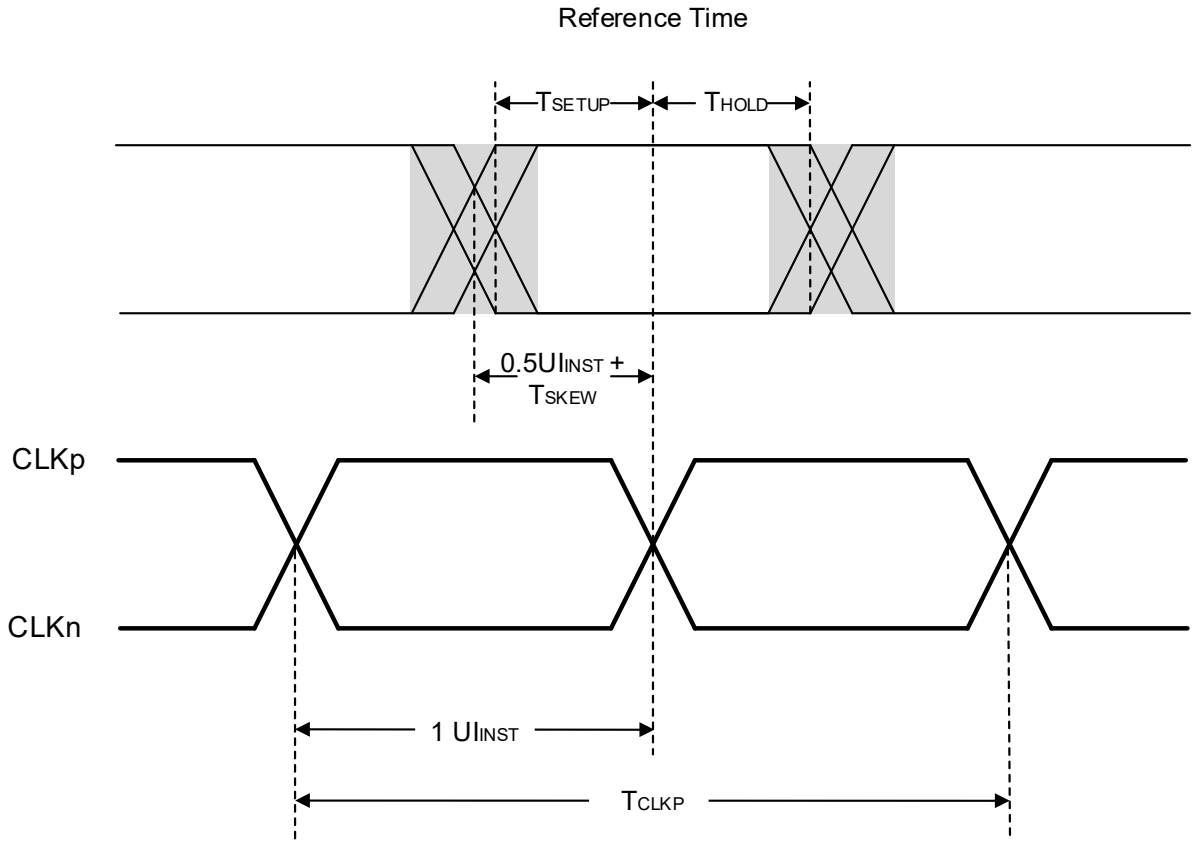


Table 5-23 MIPI DPHY Timing Constants

Parameter	Symbol	Units in Ulinst			Operational Frequency in Gbps	
		Min	Max	Total	Min	Max
Data to Clock Skew	$T_{skew[tx]}$	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	$T_{setup[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5
Clock to Data Hold Time	$T_{hold[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

5.9.7 GMAC Interface Timing

5.9.7.1 RGMII

Figure 5-25 RGMII Receive Timing

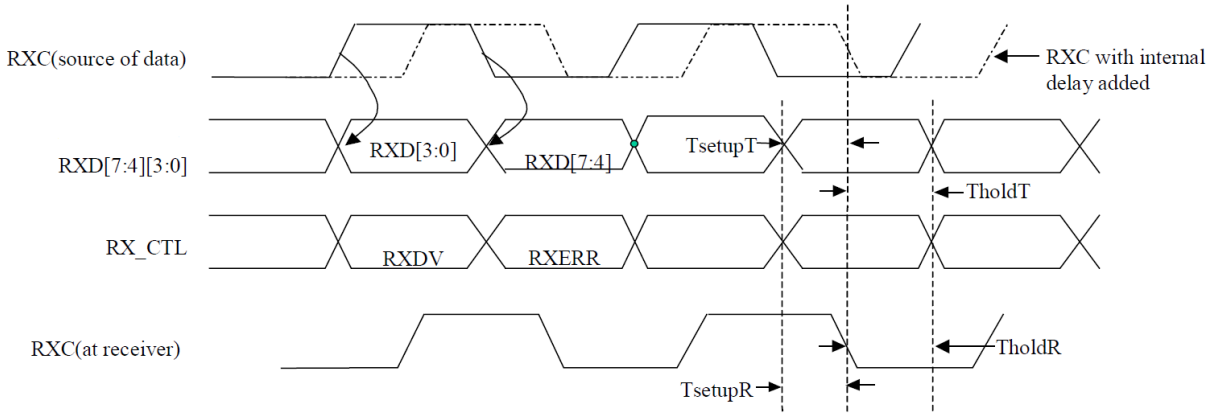


Figure 5-26 RGMII Transmit Timing

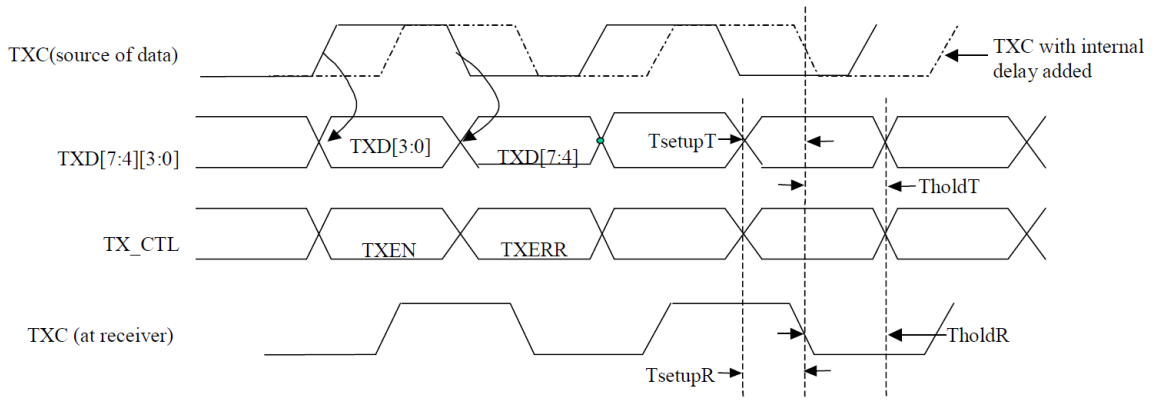


Table 5-24 RGMII Timing Constants

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration *note1	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns

Parameter	Description	Min	Typical	Max	Unit
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns
Note: For 10 Mbps and 100 Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.					

5.9.7.2 RMII

Figure 5-27 RMII Receive Timing

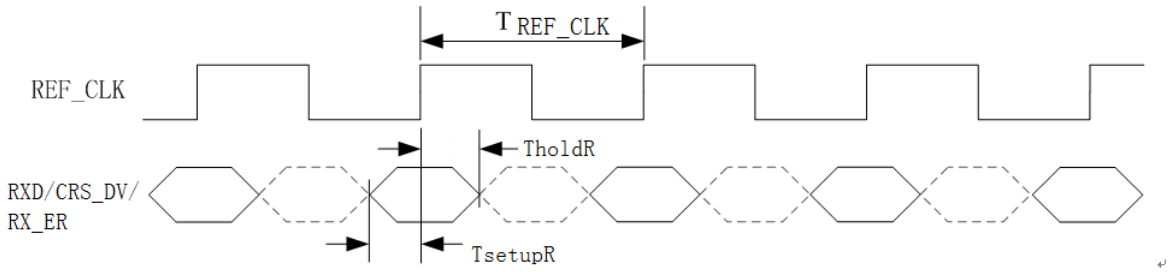


Figure 5-28 RMII Transmit Timing

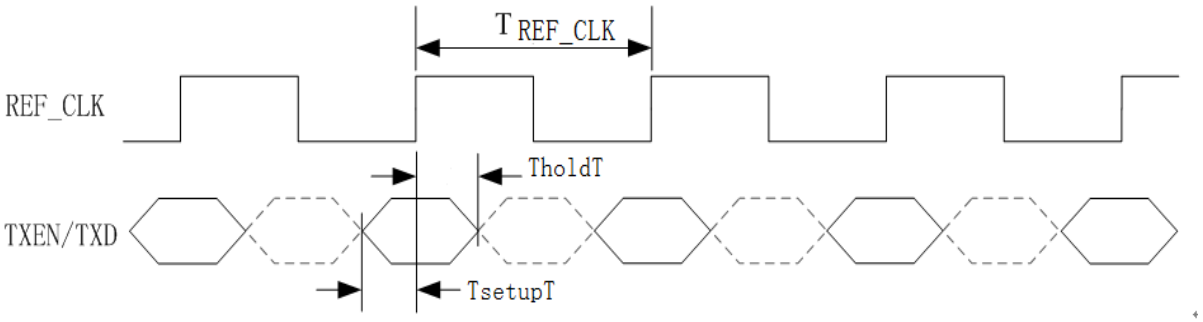


Table 5-25 RMII Timing Constants

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.9.8 SPI Interface Timing

Figure 5-29 SPI Writing Timing

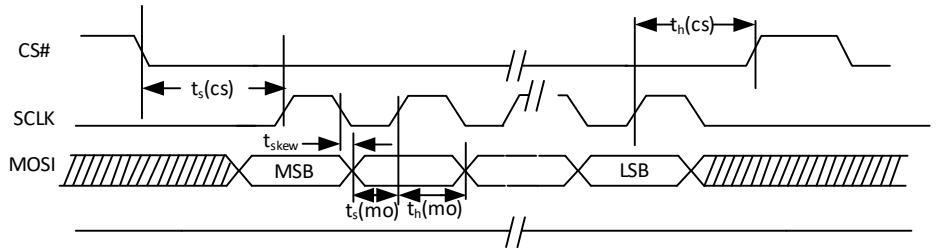


Figure 5-30 SPI Reading Timing

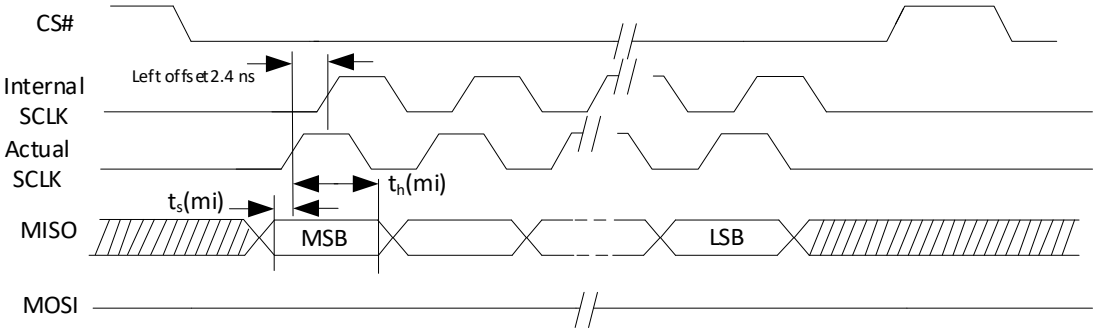


Table 5-26 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	t_s(cs)	-	2T(1)	-	ns
CS# Active Hold Time	t_h(cs)	-	2T(1)	-	ns
CLK/Data output skew time	t_{skew}(2)	-	-	1	ns
Data output Delay Time	t_v(mo)	-	T(1)/2-3	-	ns
Data output Hold Time	t_h(mo)	-	T(1)/2-3	-	ns
Data In Setup Time	t_s(mi)	0.2	-	-	ns
Data In Hold Time	t_h(mi)	0.2	-	-	ns

Note:

(1) T is the cycle of clock.

(2) t_{skew} is the output skew time between SCLK and MOSI. SCLK may be either faster or slower than MOSI.

5.9.9 SPI_DBI Interface Timing

Figure 5-31 DBI 3-line Serial Interface Timing

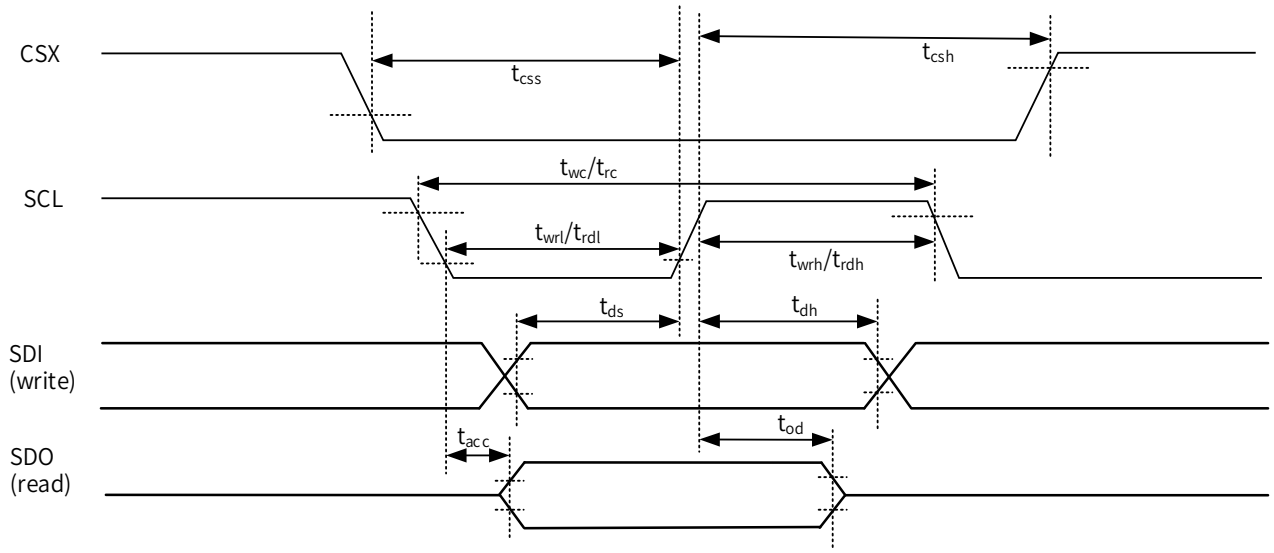


Table 5-27 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-28 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10(1)	50	ns
	Output disable time	t_{od}	15(1)	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 5-32 DBI 4-line Serial Interface Timing

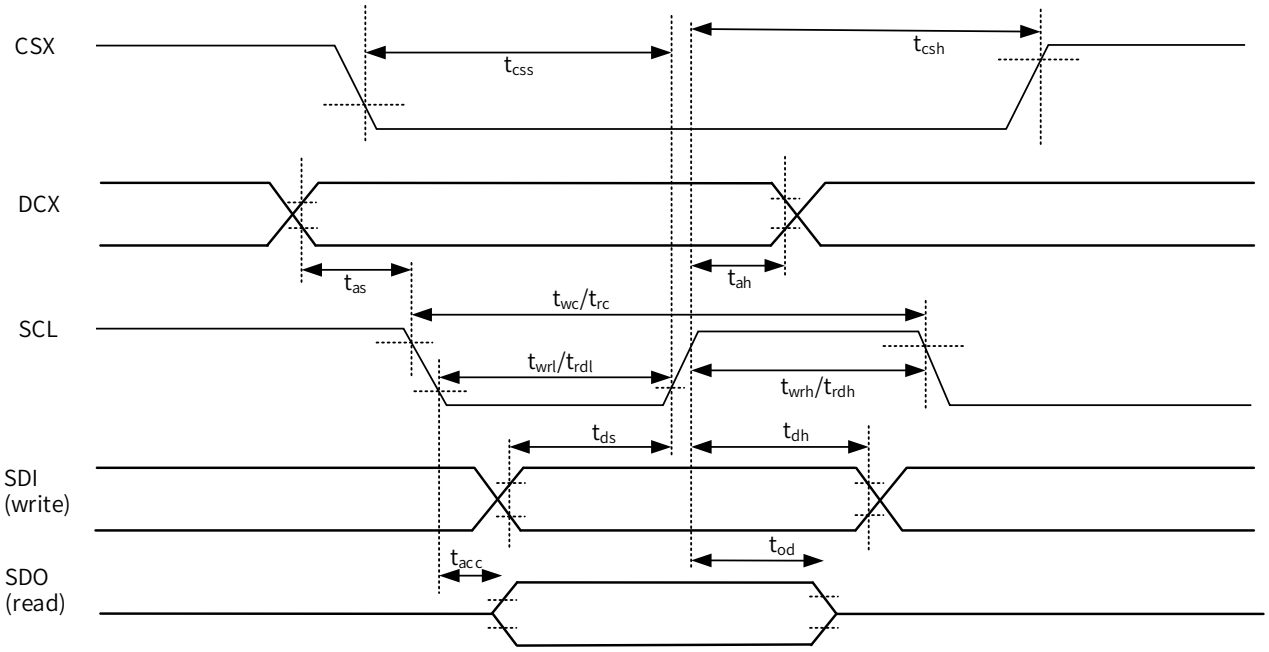


Table 5-29 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-30 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns

Signal	Parameter	Symbol	Min	Max	Unit
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

5.9.10 SPI Flash Interface Timing

5.9.10.1 Controller Output to Target Input Timing

Figure 5-33 xSPI Target Data Input Timing

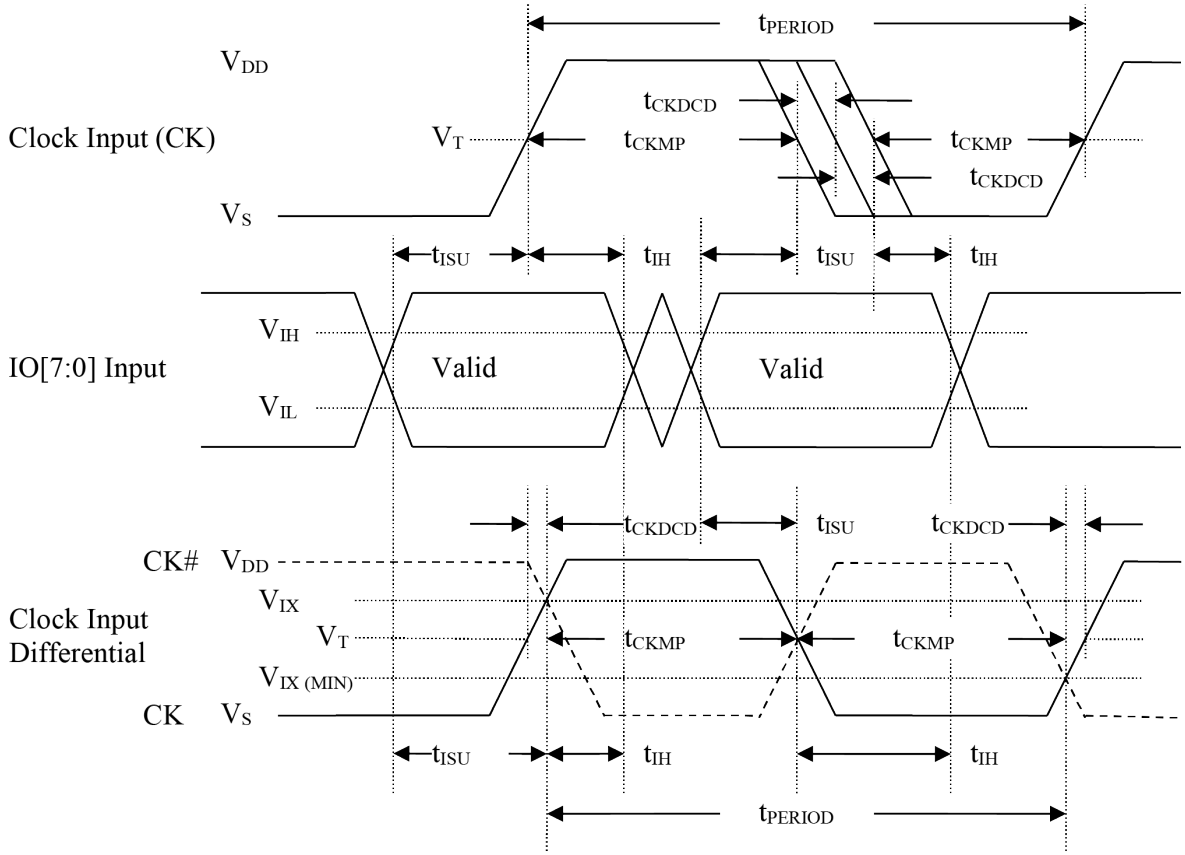


Table 5-31 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T\ (AC)}$	0.50 * V_{DD}	0.50 * V_{DD}	V
Input differential crossing (AC)	$V_{IX\ (AC)}$	0.4 * V_{DD}	0.60 * V_{DD}	V

Table 5-32 xSPI Device Input Timing

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	t_{PERIOD}	6	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to V_T.
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to VIH/VIL.
Duty Cycle Distortion	t_{CKDCD}	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.7	-	3.375	-	4.5	-	ns	With respect to V_T.
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	t_{ISUddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (DTR)	t_{IHddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Setup Time (STR)	t_{ISU}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (STR)	t_{IH}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Note: (1) xSPI-333: Up to 166 MHz; up to 333 MT/s. (2) xSPI-266: Up to 133 MHz; up to 266 MT/s. (3) xSPI-200: Up to 100 MHz; up to 200 MT/s.									

5.9.10.2 Target Output to Controller Input Timing

Figure 5-34 xSPI Target Data Output Timing

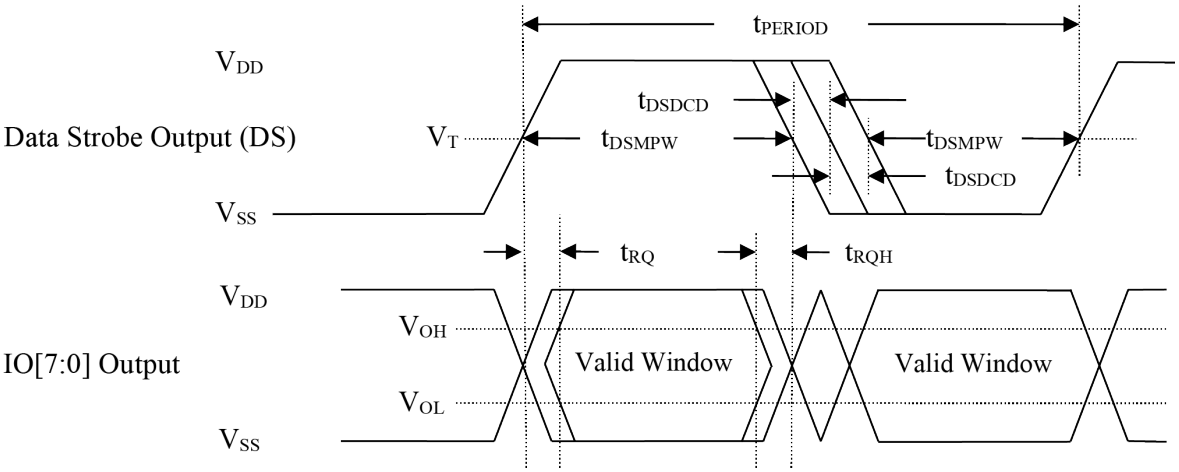


Table 5-33 xSPI Device Output Timing

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Data Strobe(2)					
Cycle Time Data Transfer Mode	t_{PERIOD}	10	-	ns	100 MHz (max) between the rising edges with respect to V_T.
Duty Cycle Distortion	t_{DSDCD}	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (tCKDCD) with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{DSMPW}	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to V_T.

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Output DATA (Referenced to DS)					
Output skew	t_{RQ}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Output hold skew	t_{RQH}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Note: (1) xSPI-200: Up to 100 MHz; up to 200 MT/s. (2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.					

5.9.11 UART Interface Timing

Figure 5-35 UART RX Timing

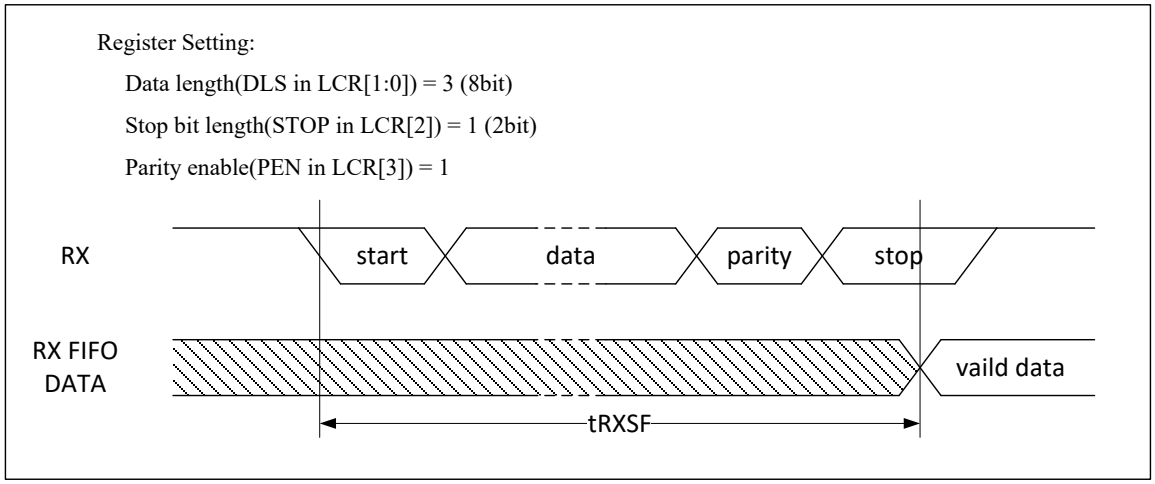


Figure 5-36 UART nCTS Timing

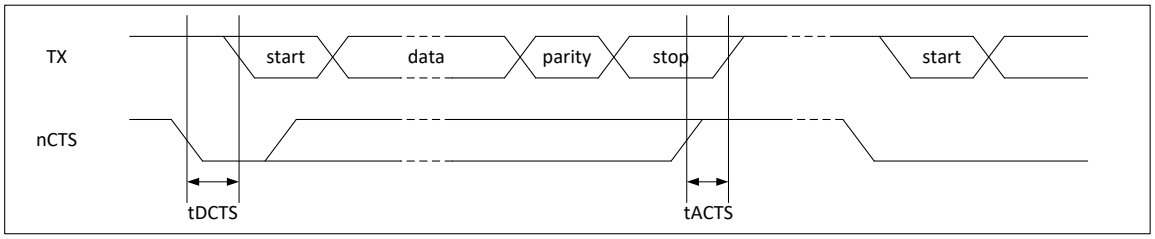


Figure 5-37 UART nRTS Timing

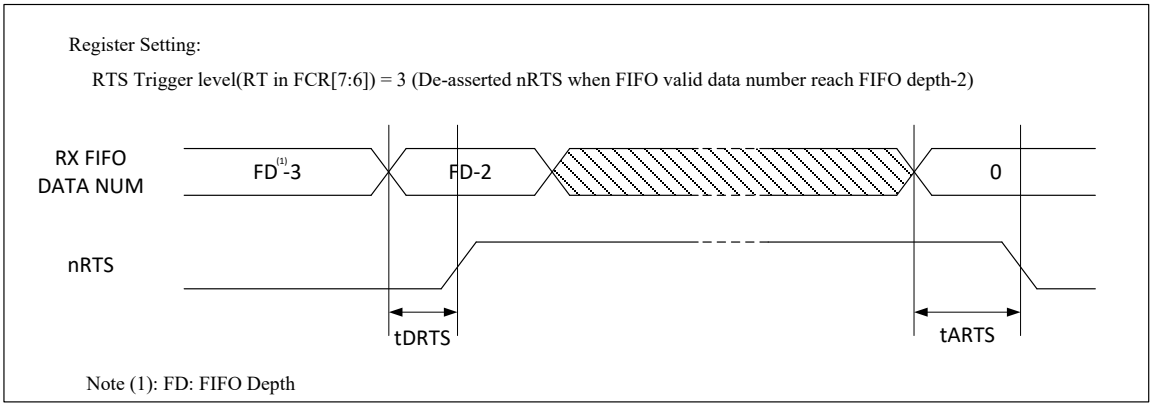


Table 5-34 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP(1)	-	11*BRP(1)	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1) BRP: Baud-Rate Period.					

5.9.12 TWI Interface Timing

Figure 5-38 TWI Timing

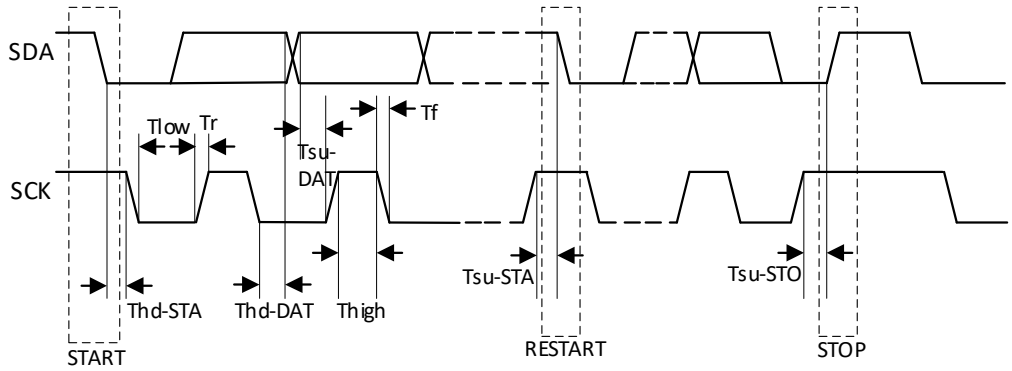


Table 5-35 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz

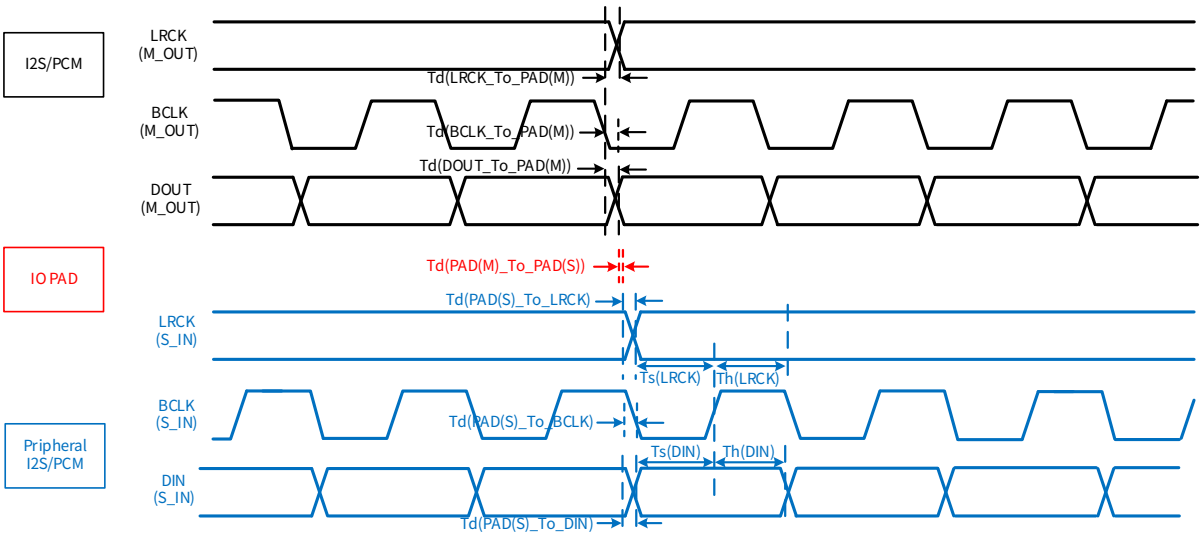
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	0	-	0	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.9.13 I2S Interface Timing

5.9.13.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 5-39.

Figure 5-39 Data Output Timing of I2S/PCM in Master Mode



The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in Table 5-36.

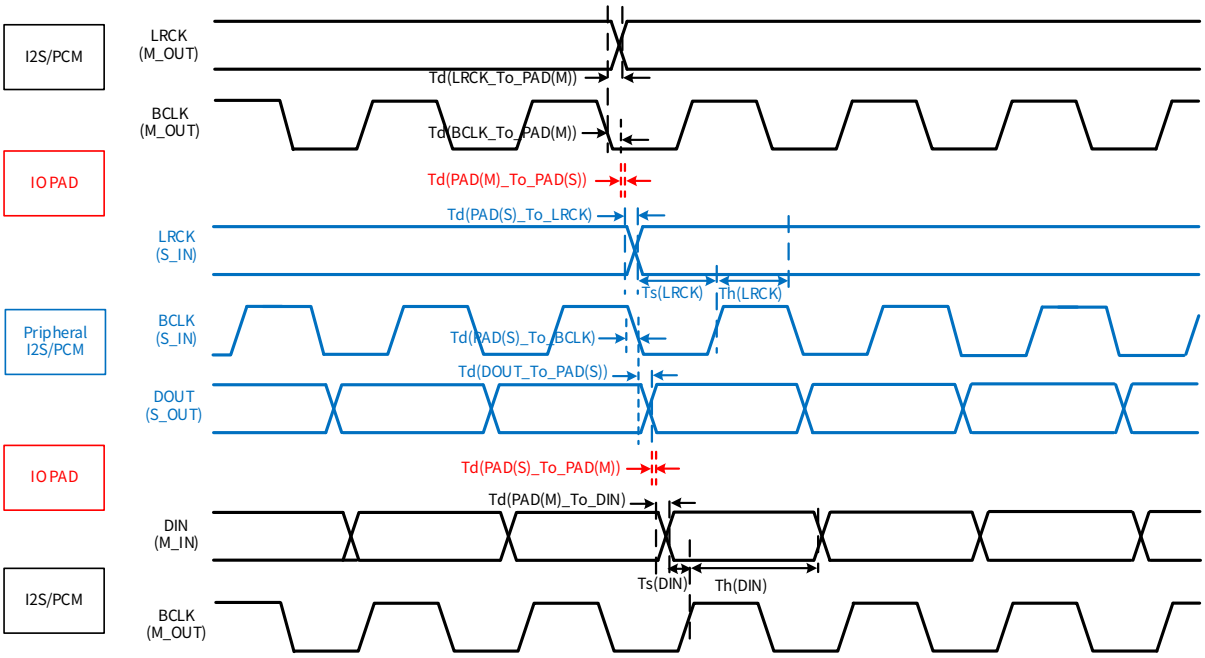
Table 5-36 Data Output Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T_d(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T_w1<2.5(requirement)	ns
T_d(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(restriction)		
T_d(DOUT_To_PAD(M))	DOUT to PAD(M) Delay	/	T3<6.5(restriction)		
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T_d(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimation)	T_w2*<1.0(requirement)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimation)		
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimation)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T_d(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assumption)	T_w3*<2.5(requirement)	ns
T_d(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assumption)		
T_d(PAD(S)_To_DIN)	PAD(S) to DIN Delay	/	T9*<6.5(assumption)		
T_s(LRCK)	LRCK Setup Slack	T10*(analysis)	/	/	ns
T_h(LRCK)	LRCK Hold Slack	T11*(analysis)	/	/	ns
T_s(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
T_h(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

5.9.13.2 Data Input timing of I2S/PCM in Master mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 5-40.

Figure 5-40 Data Input Timing of I2S/PCM in Master Mode



The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in Table 5-37.

Table 5-37 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5 (estimation)	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)		ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0 (estimation)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)		

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T5*<6.5(requirement)	Tw3*<2.5 (estimation)	ns
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T6*<6.5(requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	T7*<6.5(requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	T8*(analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	T9*(analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	T10*<7.0(requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	T11<6.5(requirement)	/	ns
Ts(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

5.9.14 DMIC Interface Timing

Figure 5-41 DMIC Timing

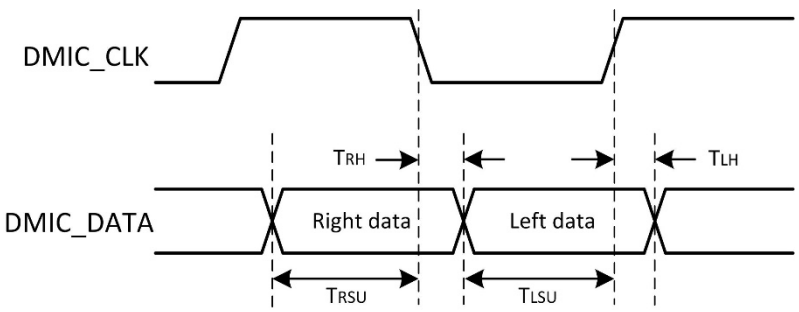


Table 5-38 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Setup Time to Falling Edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) Hold Time from Falling Edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) Setup Time to Rising Edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) Hold Time From Rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.9.15 OWA Interface Timing

Figure 5-42 OWA Timing

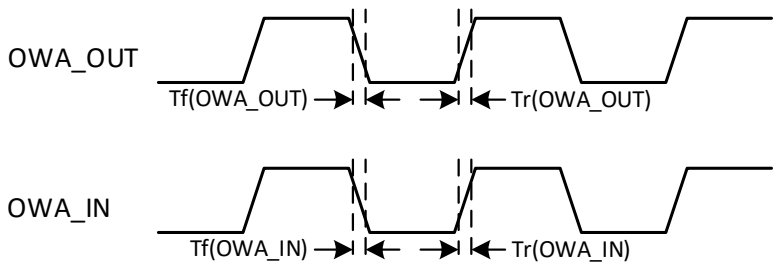


Table 5-39 OWA Timing Constants

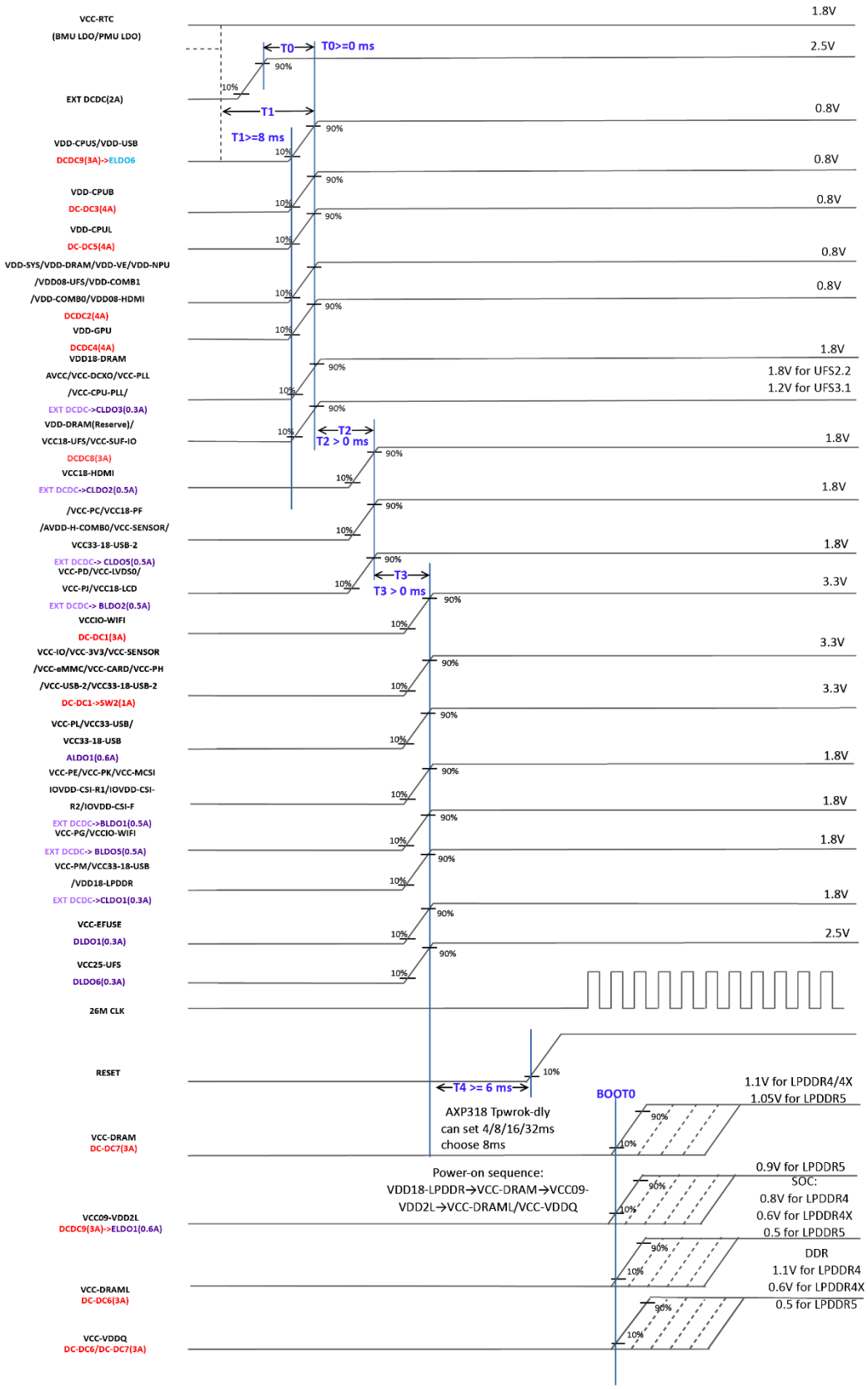
Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT Fall Time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN Rise Time	Tr(OWA_IN)	-	-	4	ns
OWA_IN Fall Time	Tf(OWA_IN)	-	-	4	ns

5.10 Power-up and Power-down Sequence

5.10.1 Power-up Sequence

Figure 5-43 shows an example of the power-up sequence. The description of the power-up sequence is as follows.

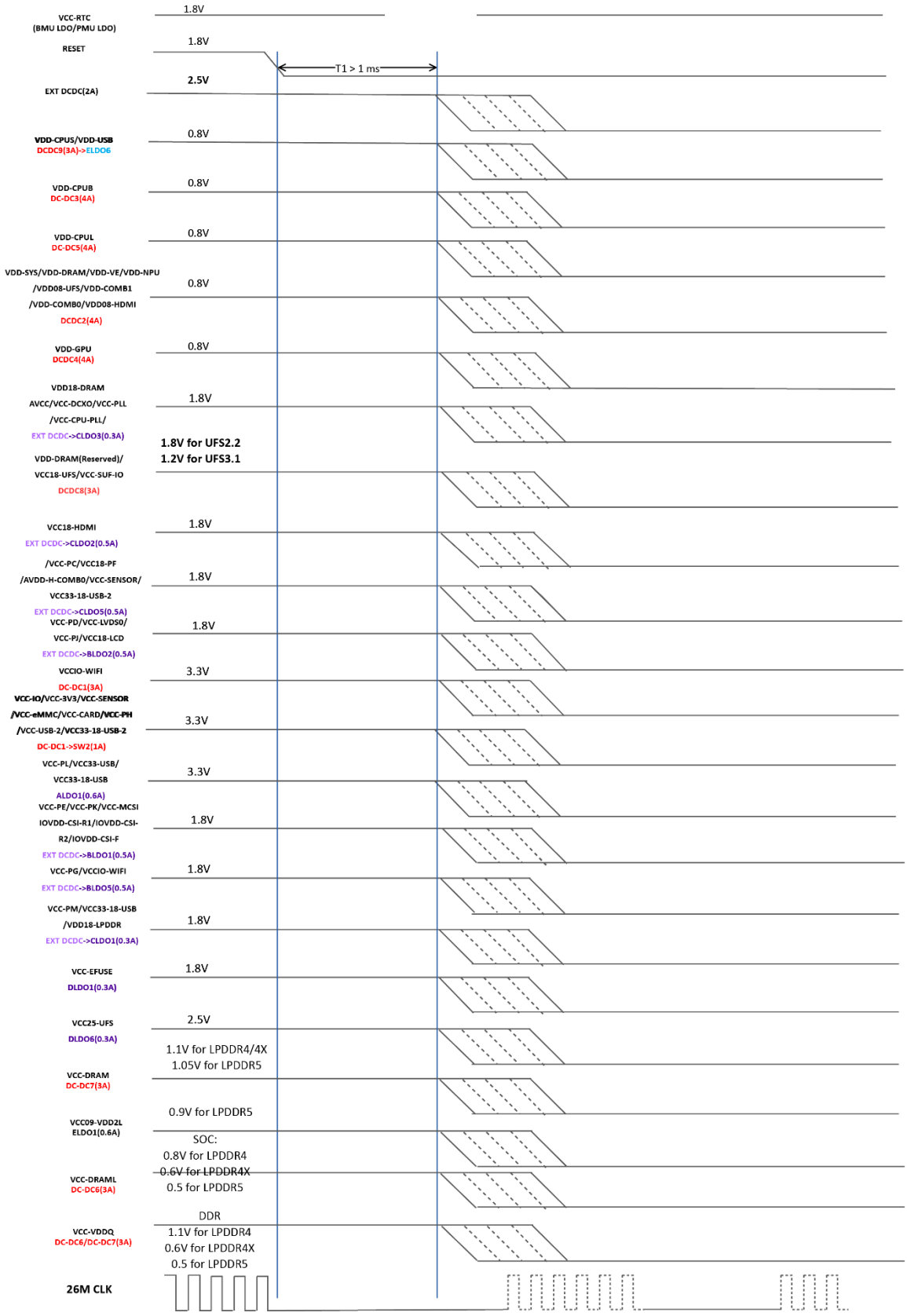
Figure 5-43 Power-up Sequence



5.10.2 Power-down Sequence

Figure 5-44 shows an example of the power-down sequence. The description of the power-down sequence is as follows.

Figure 5-44 Power-down Sequence



6 Temperature and Thermal Characteristics

6.1.1 Temperature

The following tables describe the temperature of the device

Table 6-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T_a	Ambient Operating Temperature	-25	75	°C
T_{STG}(1)	Storage Temperature	-40	150	°C

(1) The MIN and MAX values of T_{STG} are calculated in accordance with the *High Temperature Storage Life JESD22-A103E*.

Table 6-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
A733	-25	115	125	°C

6.1.2 Package Thermal Characteristics

The maximum chip junction temperature ($T_{J\ max}$) must never exceed the values given in Table 6-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-3 A733MX-HN3, A733MX-N3X, and A733MX-1XX Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	25.265	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	10.33	-	°C/W

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JC}	Junction-to-Case Thermal Resistance	-	-	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

(2) The testing PCB is 2 layers, 114.3 mm x 76.2 mm body, and 0.216 mm thickness. Ambient temperature is 25.2°C.

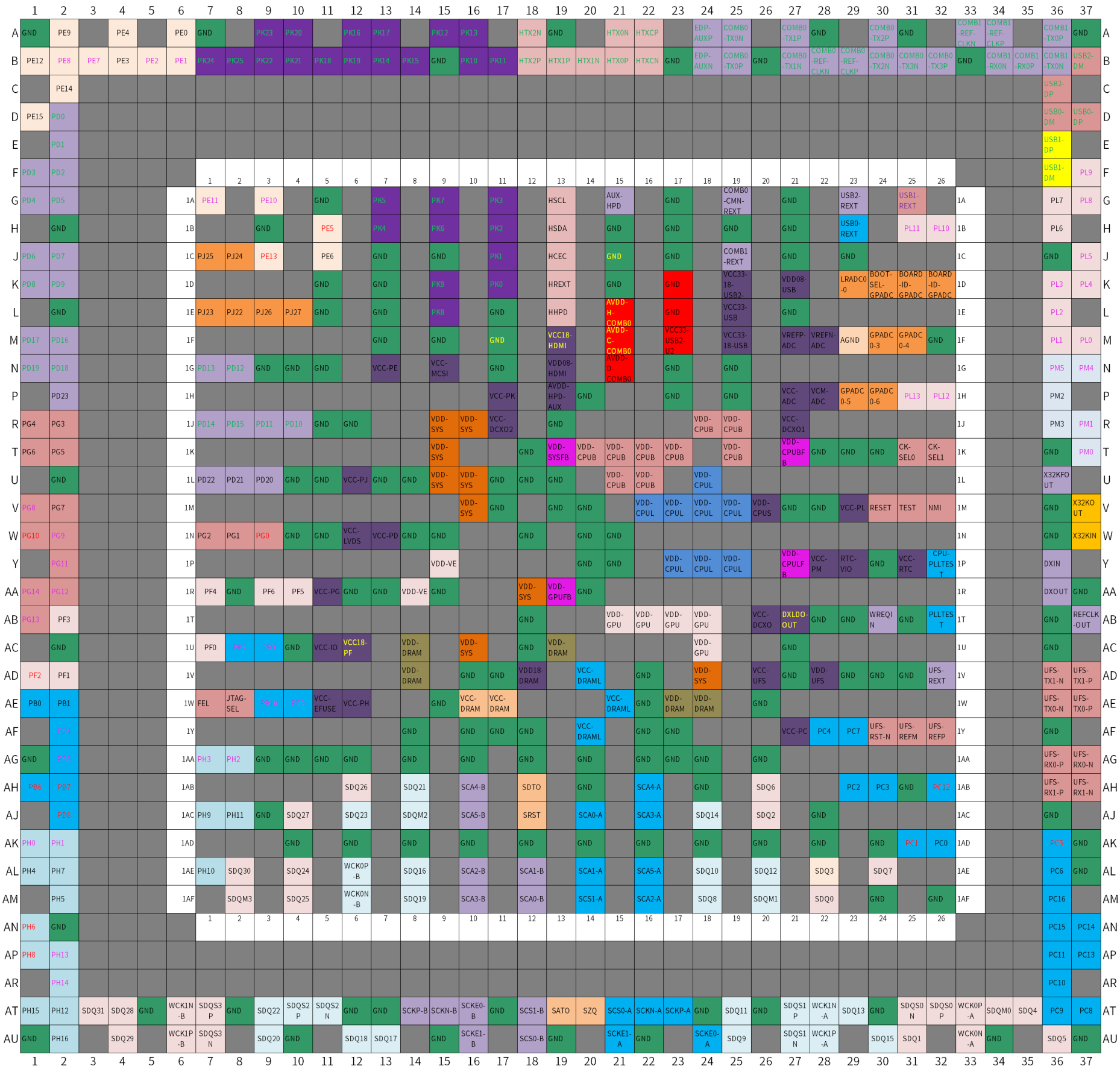
(3) Due to the value of θ_{JC} approaching zero, it is unable to provide accurate test data for ED-FCCSP package.

7 Pin Assignment

7.1.1 Pin Map

The following shows the A733 pin map with ED-FCCSP 570 balls, 15 mm x 15 mm body size, 0.5 mm & 0.4 mm mixed ball pitch, and 0.25 mm ball size.

Figure 7-1 Pin Map



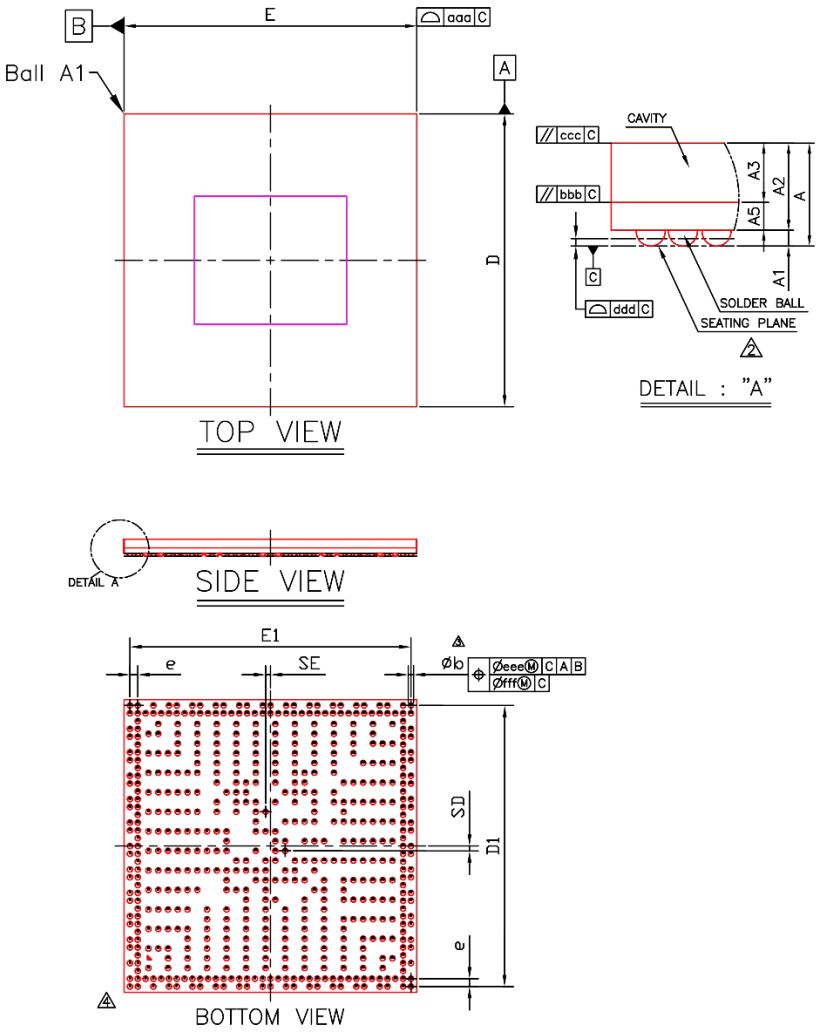
NOTE

The ball pitch of outer two circles on the pin map is 0.4 mm, while the rest is 0.5 mm.

7.1.2 Package Dimension

The following figure shows the top, bottom, and side views of the A733 package.

Figure 7-2 A733MX-HN3, A733MX-N3X, and A733MX-1XX Package Dimension



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.809	0.880	0.951	0.032	0.035	0.037
A1	0.110	0.160	0.210	0.004	0.006	0.008
A2	0.670	0.720	0.770	0.026	0.028	0.030
A3	0.420	0.450	0.480	0.017	0.018	0.019
A5	0.230	0.270	0.310	0.009	0.011	0.012
E	14.900	15.000	15.100	0.587	0.591	0.594
D	14.900	15.000	15.100	0.587	0.591	0.594
E1	---	14.400	---	---	0.567	---
D1	---	14.400	---	---	0.567	---
e	---	0.400	---	---	0.016	---
b	0.220	0.270	0.320	0.009	0.011	0.013
aaa		0.100			0.004	
bbb		0.100			0.004	
ccc		0.150			0.006	
ddd		0.130			0.005	
eee		0.150			0.006	
fff		0.050			0.002	
MD/ME		37/37				
SE		0.250			0.010	
SD		0.250			0.010	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.250 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.250 mm.

8 Carrier, Storage and Backing Information

8.1 Carrier

The following table shows matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 135.9 mm x 7.62 mm	119 Pieces/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

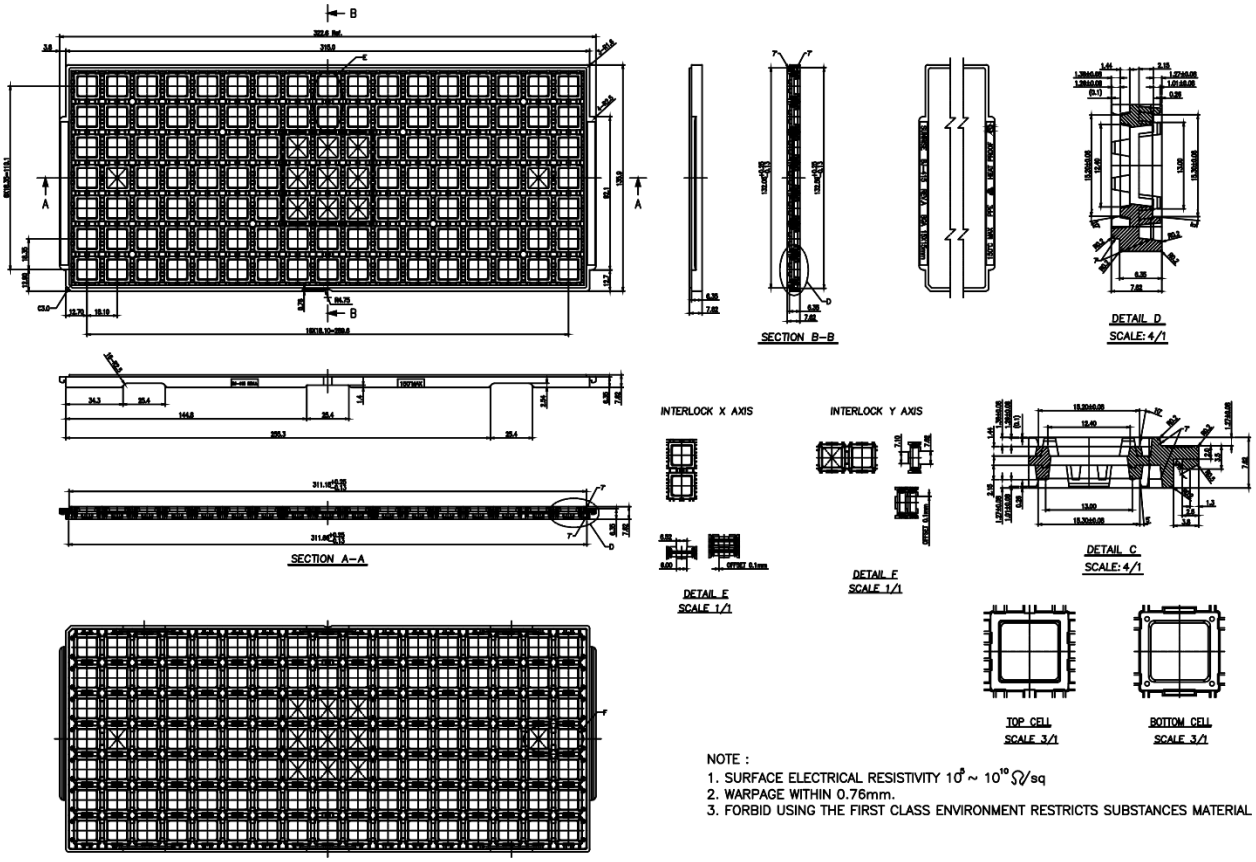
The following table shows Packing quantity.

Table 8-2 Packing Quantity Information

Sample	Size (mm)	Pieces/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
A733	15 x15	119	10	1190	6	7140

The following figure shows tray dimension drawing.

Figure 8-1 Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	⩽30°C / 85%RH
2	1 year	⩽30°C / 60%RH
2a	4 weeks	⩽30°C / 60%RH
3	168 hours	⩽30°C / 60%RH
4	72 hours	⩽30°C / 60%RH

MSL	Out-of-bag floor life	Comments
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The A733 device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 8-4 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Shelf Life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 8-5 Out-of-bag Duration

Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake chips if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

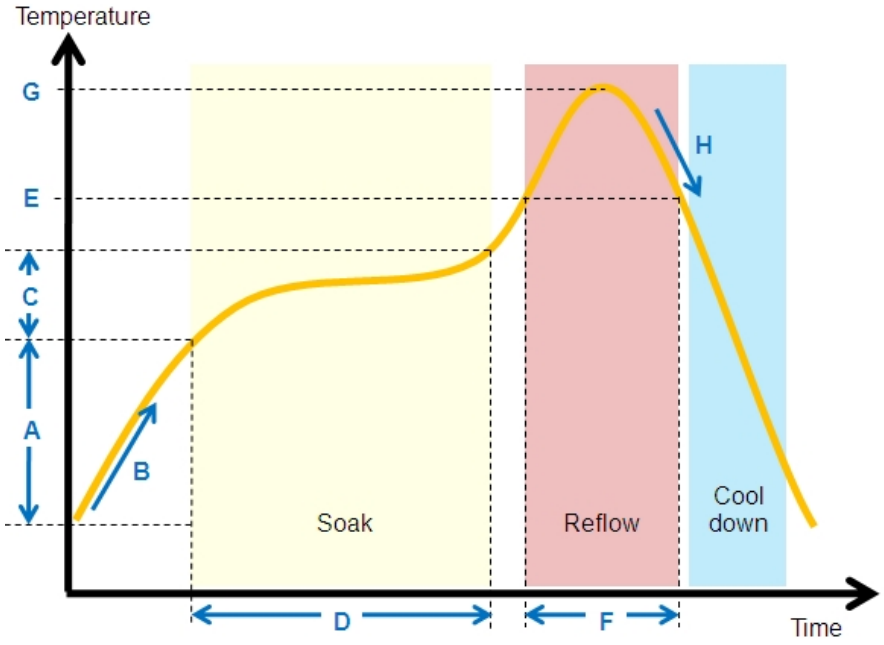


Table 9-1 Lead-free Reflow Profile Conditions

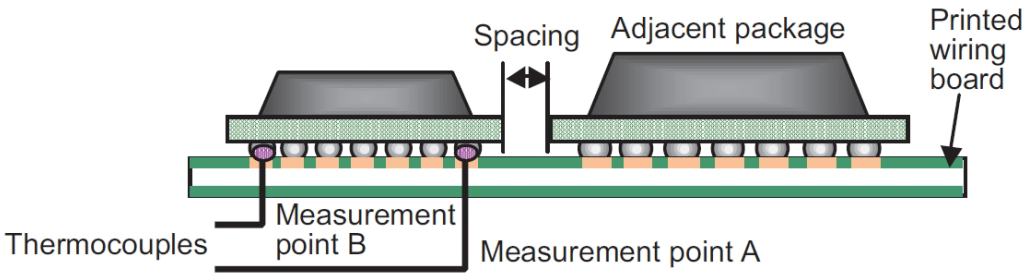
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s
G	Peak temperature	240–250 °C
H	Cool down temperature rate	⩽4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder

wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the Reflow Soldering Process



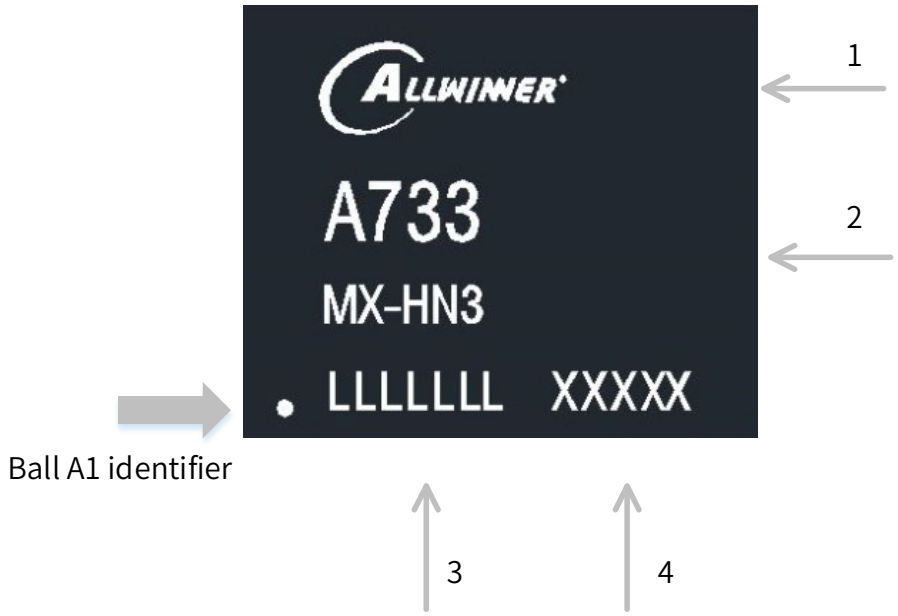
If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 Part Marking

10.1 A733MX-HN3

The following figure shows the A733MX-HN3 marking.

Figure 10-1 A733MX-HN3 Marking



The following table describes the A733MX-HN3 marking definitions.

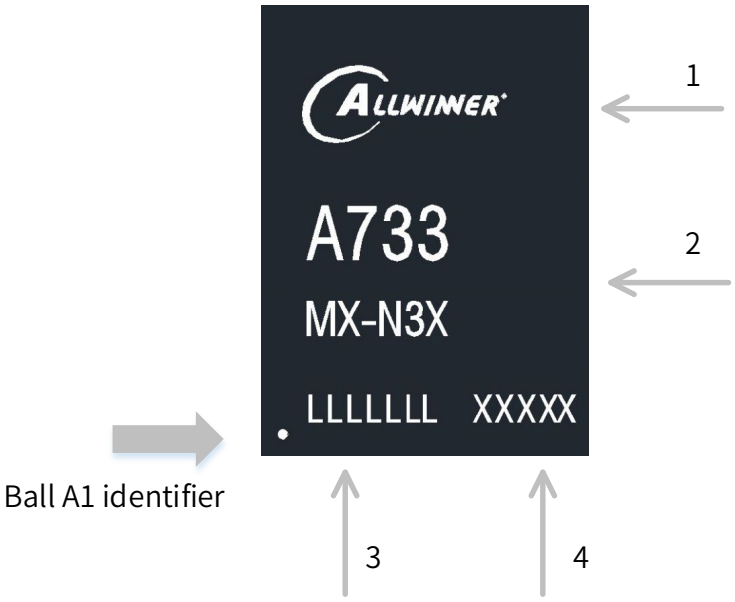
Table 10-1 A733MX-HN3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	A733MX-HN3	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.2 A733MX-N3X

The following figure shows the A733MX-N3X marking.

Figure 10-2 A733MX-N3X Marking



The following table describes the A733MX-N3X marking definitions.

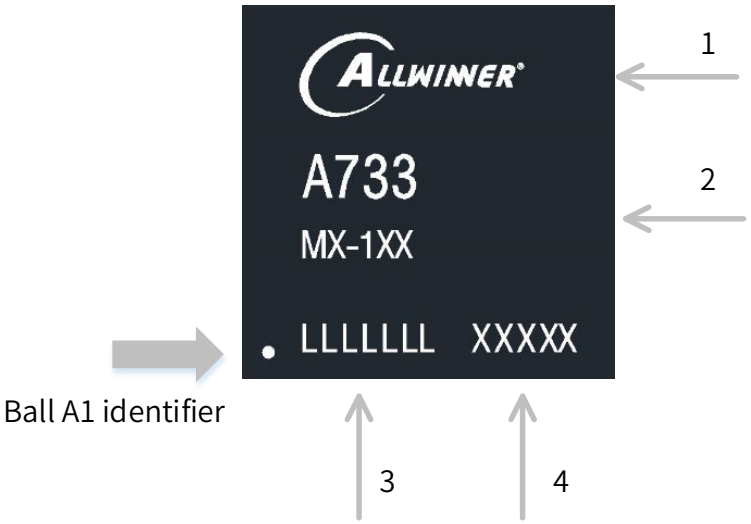
Table 10-2 A733MX-N3X Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	A733MX-N3X	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.3 A733MX-1XX

The following figure shows the A733MX-1XX marking.

Figure 10-3 A733MX-1XX Marking



The following table describes the A733MX-1XX marking definitions.

Table 10-3 A733MX-1XX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	A733MX-1XX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

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