Qualcomm Technologies, Inc.

QCS6490 and QCS5430 Data Sheet

Data Sheet
80-23889-1 Rev. AW
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Device description

QCS6490 and QCS5430 are chipsets that deliver premium features with advanced camera, AI, and compute for high performance at low-power. These chipsets are built for industrial and commercial IoT applications such as ruggedized handhelds and tablets, kiosks, industrial scanners, point of sale systems, human machine interface systems, robotics, drone and controllers, cameras, and edge AI boxes.

QCS6490 and QCS5430 are pin-to-pin compatible and share a similar package dimension of 14.0 × 12.0 × 0.91 mm.

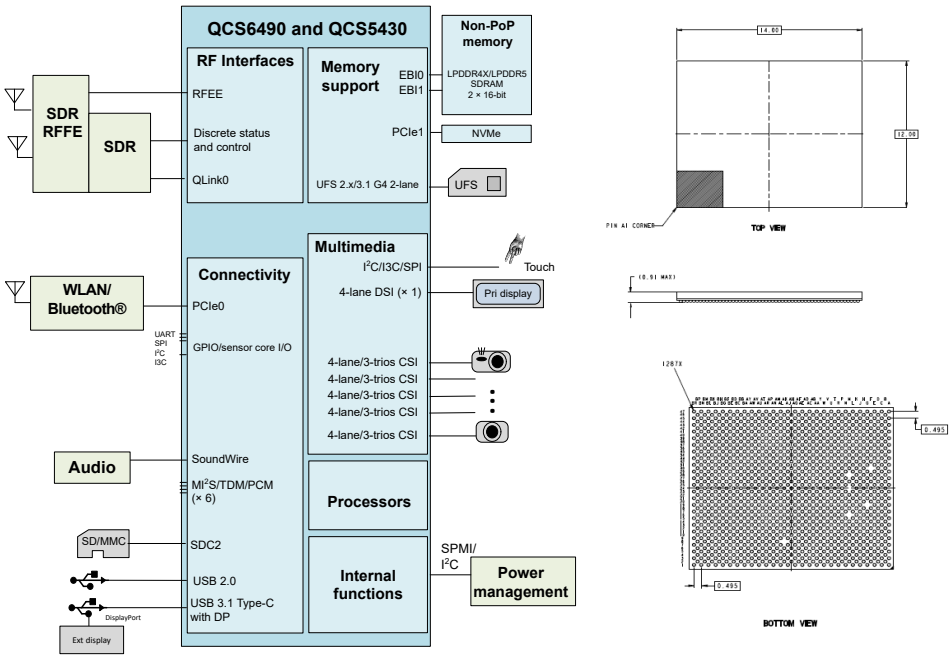
QCS6490 and QCS5430 functional block diagram
Device physical dimensions
Device ordering information

Key features

- Qualcomm® Kryo™ CPU built on Arm® v8 Cortex® technology.
- Qualcomm® Adreno™ GPU for better graphics performance and power efficiency.
- Qualcomm® Hexagon™ compute DSP with Hexagon Vector eXtensions (HVX) and Hexagon Tensor Accelerator.
- Qualcomm Spectra™ ISP image-processing engine for the ultimate photography and videography experiences.
- Qualcomm® Adreno™ VPU for high-quality, ultra HD video encode and decode.
- Qualcomm® Adreno™ DPU for on-device and external ultra HD display support.

QCS6490 and QCS5430 features

High-level block diagram and package outline



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1 Overview

This topic provides the chipset component information, high-level functional block diagram, and the device features.

1.1 QCS6490 and QCS5430 chipset components

For details regarding the QCS6490 and QCS5430 chipset components see, *QCS6490 and QCS5430 chipset components* (80-23889-10A) and *QCS6490/QCS5430 Technical Reference Manual* (80-20659-5).

1.2 QCS6490 and QCS5430 functional block diagram

The following functional block diagram shows the overall representation of the subsystems on these chipsets.

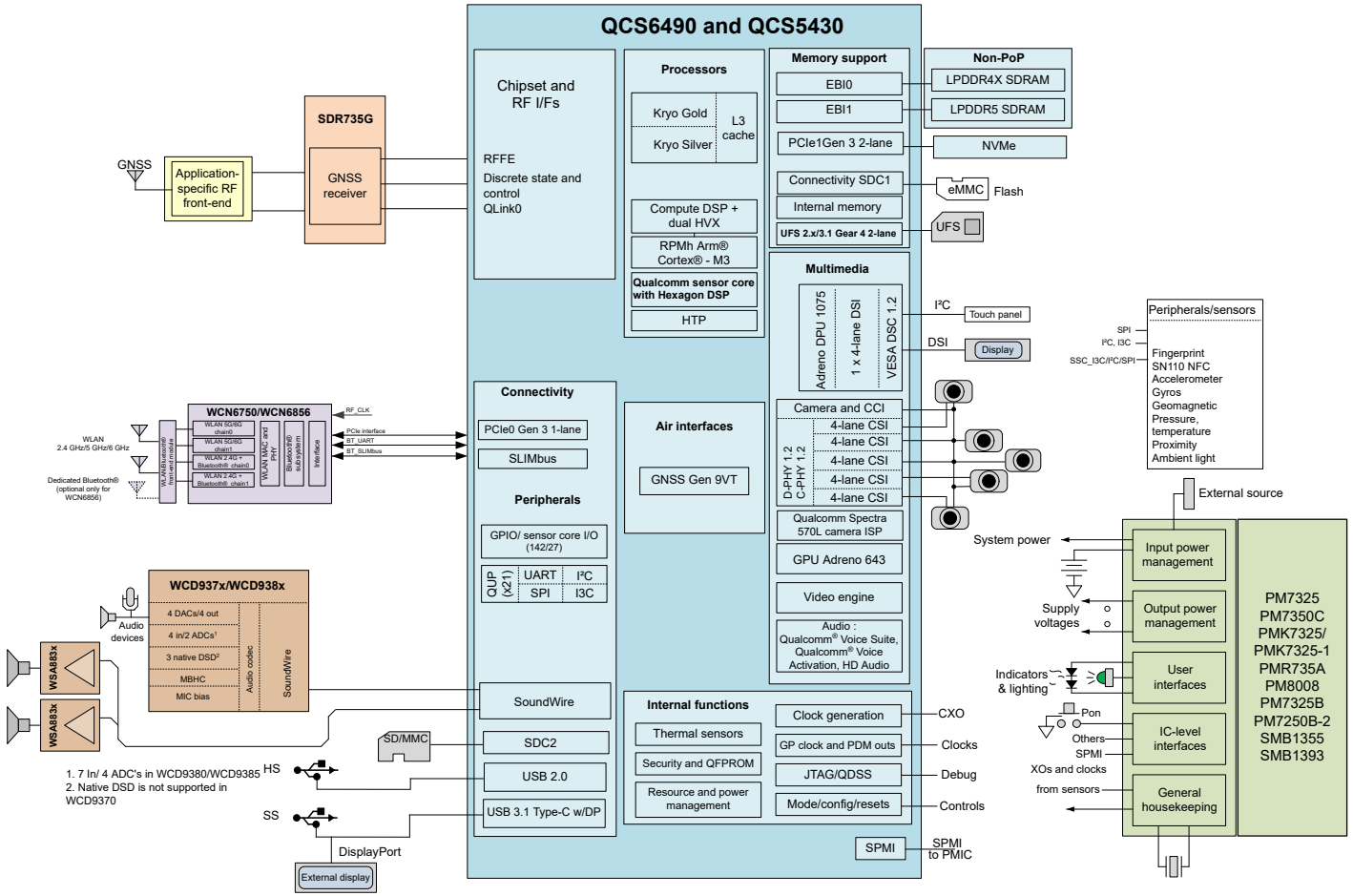


Figure 1-1 QCS6490 and QCS5430 functional block diagram

1.3 QCS6490 and QCS5430 features

The following table lists the comprehensive features of the QCS6490 and QCS5430 chipsets and its capabilities.

NOTE The QCS5430 chipset is available in four different configurations enabled through feature packs.

Some hardware features on the QCS6490 and QCS5430 are software-enabled. For details of QCS6490 and QCS5430 software-enabled features, see the latest revision of the applicable software release notes.

Processor

Feature	Description
CPU	Qualcomm® Kryo™ CPU built on Arm v8 Cortex technology **QCS6490** ■ Kryo Prime: Single high-performance core clocked up to 2.7 GHz ■ Kryo Gold: 3 high-performance cores running at 2.4 GHz ■ Kryo Silver: 4 low-power cores operating at 1.9 GHz Available in 4 configurations: ■ Feature pack 1: □ Kryo Gold: 2 high-performance Kryo Gold cores, each clocked at 2.13 GHz □ Kryo Silver: 4 low-power Kryo Silver cores running at 1.8 GHz each ■ Feature pack 2: □ Kryo Prime: Single high-performance core clocked up to 2.2 GHz □ Kryo Gold: 3 high-performance Kryo Gold cores, each clocked at 2.13 GHz □ Kryo Silver: 4 low-power Kryo Silver cores running at 1.8 GHz each ■ Feature pack 2.5: and 3 [a] □ Kryo Prime: Single high-performance core clocked up to 2.38 GHz □ Kryo Gold: 3 high-performance Kryo Gold cores, each clocked at 2.4 GHz □ Kryo Silver: 4 low-power Kryo Silver cores running at 1.8 GHz each
Digital signal processing (DSP) and artificial intelligence (AI) engine	Compute Hexagon DSP with dual Hexagon Vector eXtensions (HVX) for: ■ Video playback enhancements ■ Virtual reality ■ Computer vision ■ Camera snapshot enhancements ■ Video capture enhancement ■ Machine learning This DSP is optimized for handling signal processing tasks efficiently Hexagon coprocessor 2.0 ■ Additional coprocessor that complements the main CPU and DSP ■ Vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions Hexagon Tensor Accelerator ■ Designed to accelerate tensor-based operations ■ Commonly used in deep learning and neural networks

Feature	Description
Always-on subsystem	Always-on subsystem with always-on processor The hardware-based resource and power management (RPMh) incorporates hardware accelerators for voltage control and regulation, clock management, and resource communication
Low-power island (LPI) with Hexagon DSP	Embedded neuron processor unit (eNPU)/AI accelerator: Embedded AI accelerator for sensor core and low-power audio use cases

[a] Software enablement for feature packs 2.5 and 3 is under progress.

Memory

Feature	Description
System memory	The memory offers dual-channel non-package-on-package (non-PoP) high-speed LPDDR5/ LPDDR4X SDRAM ■ The LPDDR5 SDRAM is optimized for a clock speed of 3200 MHz using a 2 × 16-bit configuration ■ The LPDDR4X SDRAM is optimized for a clock speed of 2133 MHz using a 2 × 16-bit configuration ■ Supports multichip packages (MCP) and discrete DRAMs
External memory	UFS 2.x/3.1, two-lane high speed (HS) gear 4 SDv3.0 4 bit for SD card and eMMC 5.1 PCIe1 interface: PCIe1 two-lane, supports non-volatile memory express (NVMe)
Other internal memory	172 kB internal memory (IMEM) 512 kB graphics memory (GMEM)

Wireless connectivity

Feature	Description
Wi-Fi/ Bluetooth	■ Supported with WCN6750/WCN6856 ■ WLAN standards: 802.11ax, 2 × 2 multiple input, multiple output (MIMO) Wi-Fi 6E ■ Bluetooth 5.2 compliant ■ Only WCN6856 supports dual-band simultaneous (DBS)
Antenna sharing	Antenna shared between Wi-Fi and wireless area network (WAN)
Location	SDR735G: ■ Multiband GNSS - Integrated Qualcomm® Location Suite Engine ■ Global positioning system (GPS), GLONASS, NavIC, BeiDou, Galileo, quasi-zenith satellite system (QZSS) ■ Supports GNSS L1 and L5 bands ■ GNSS engine hardware version: Gen 9 v4 ■ GNSS software version: v20

Multimedia

Feature	Description
Display	Adreno display processing unit (DPU) 1075: ■ : Maximum resolution for internal panel: FHD+ 144 Hz local tone map (LTM), HDR10+, WCG, improved inline RoT, rounded corner, SPR, Demura, concurrent writeback – region of interest (CWB-ROI) ■ (for all feature packs): Maximum resolution for internal panel: FHD+ 120 Hz LTM, HDR10+, WCG, improved inline RoT, rounded corner, SPR, Demura, CWB-ROI

Feature	Description
	■ One 4-lane; DSI D-PHY 1.2 or C-PHY 1.2; VESA DSC 1.2 ■ 4K60 display support over DisplayPort (USB3 + DisplayPort concurrency)
Camera	■ Qualcomm Spectra 570 L supports 36 + 22 MP at 30 fps/3 × 22 MP 30 fps ZSL. It also supports connectivity to multiple cameras due to 5 C-PHY/D-PHY interfaces ■ Real-time sensor input resolution: 22 + 22 + 22 ■ 3 IFE + 2 IFE lite, 5 concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 configuration ■ 5x D-PHY v1.2/C-PHY v1.2 feature pack 1 and 2: ■ Qualcomm Spectra 570 L: 22 + 22 MP at 30 fps ZSL ■ Qualcomm Spectra 570 L image signal processor (ISP) supports connectivity to multiple cameras due to 4 C-PHY/D-PHY interfaces ■ Real-time sensor input resolution: 22 + 22 ■ 2 IFE (22 MP + 22 MP) + 2 IFE lite, 4 concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 configuration ■ 4x D-PHY v1.2/C-PHY v1.2 feature pack 2.5 and 3: ■ Qualcomm Spectra 570 L: 36 + 22 MP at 30 fps/3 x 22 MP 30 fps ZSL ■ Qualcomm Spectra 570 L ISP supports connectivity to multiple cameras due to 5 C-PHY/D-PHY interfaces ■ Real-time sensor input resolution: 22 + 22 + 22 ■ 3 IFE (22 MP + 22 MP + 22 MP) + 2 IFE lite, 5 concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 configuration ■ 5x D-PHY v1.2/C-PHY v1.2
Video	Adreno video processing unit (VPU) 633 – fifth-generation ultra high definition (UHD) ■ Video decode up to 4K60 for H.264/H.265/VP9 ■ Video encode: Up to 4K30 for H.264/H.265 ■ Video concurrency: 1080p60 decode and 1080p60 encode/ 4K30 decode + 1080p30 encode ■ HDR playback: Support for HDR10 and HDR10+ ■ HFR capture: 720p at 480 fps or 1080p at 240 fps
Graphics	■ : Adreno graphics processing unit (GPU) 643 ■ : Adreno GPU 642 L ■ OpenGL ES 3.2, Vulkan 1.x ■ OpenCL 2.0, DX FL12
Audio	Hexagon digital signal processor (DSP) V66M: LPI, improved voice UI concurrencies, ML hardware accelerator, LPI shared with sensor subsystem ■ Qualcomm Voice Activation and keyword detection ■ Echo cancellation and noise suppression (ECNS) ■ DSP offload for audio playback, including universal serial bus (USB) digital audio and Bluetooth audio Codec: WCD9370/WCD9375/WCD9380/WCD9385 high fidelity audio codec Speaker amplifier: WSA8830/WSA8835 class-H, low-noise smart amplifier

Physical interfaces

Interface	Description
Qualcomm universal peripheral (QUP) ports	21: multiplexed serial interface functions
USB	One USB 3.1 port: Gen 1, 5 Gbps (DisplayPort + data), supports Type-C with DisplayPort v1.4 and one USB 2.0 HS port

Interface	Description
PCIe	■ PCIe0 Gen 3 1-lane for WCN6750/WCN6856 ■ PCIe1 interface: PCIe1 two-lane supports NVMe
Secure digital card (SDC) interfaces	■ 2 ports (SDC1 and SDC2); SD 3.0 ■ SDC2 is dual-voltage ■ SD/MM card ■ Universal Flash Storage (UFS)
Audio interfaces	■ SLIMbus for WCN6750/WCN6856 ■ SoundWire interface (2 Tx and 2 Rx data for codec) ■ SoundWire microphone support ■ Dedicated SoundWire interface for smart speaker amplifier ■ 3 digital microphone (DMIC) ports in LPI ■ 5 MI2S with 2x data lanes to support full duplex stereo, or up to 4 channel Tx/Rx application ■ One MI2S supports 4 data lanes for up to 8 channels Tx/Rx application ■ Audio over USB Type-C ■ 4 MIS ports ■ 2 I²S ports SoundWire interface **WCN6750** ■ SLIMbus interface for Bluetooth audio ■ 4-wire BT_UART to interface with host **WCN6856** ■ Flexible interface SLIMbus/PCM/I²S for Bluetooth audio ■ 4-wire BT_UART or 2-wire BT_USB to interface with the host
Touchscreen support	Capacitive panels via external IC (I²C, I3C, SPI, and interrupts)

Chipset interfaces

Interface	Description
QLink	QLink port for GNSS application
Power management	2-line SPMI; plus other lines as needed, via GPIOs, I²C PM7325, PM7350C, PMK7325/PMK7325-1, PMR735A, PM8008, PM7325B, PM7250B-2, SMB1355, SMB1393 **NOTE** ■ PM7250B-2 can only be paired with PMK7325-1 ■ PM7325B can only be paired with PMK7325 QTI recommends using PM7250B-2 + PMK7325-1 combination in the customer design. For more information, see *QCM6490/QCS6490+ PM7325 + PM7350C + PM7250B-2 Reference Schematic* (80-20659-44).
Wireless connectivity	WLAN: PCIe interface SLIMbus Bluetooth: universal asynchronous receiver-transmitter (UART) interface
GPIO	■ 169 GPIO ports ■ Input configurations: pull-up, pull-down, keeper, or no pull ■ Output configurations: programmable drive current ■ Top-level mode multiplexer: provides a convenient way to program groups of GPIOs ■ Wake-up capable

Internal functions

Function	Description
Security	■ Crypto: advance encryption standard (AES)-GCM, hardware elliptic-curve cryptography (ECC) and RSA, ICE crypto engine v5 (CE5), FIPS/CAVP certifiable ■ QFPROM: fuse bits are available for original equipment manufacturer (OEM) use ■ Access control: programmable security domain protection and sand-boxing ■ Secure boot and tools: secure boot with Sectools 2.0; easy to use tool set ■ User data encryption: file-based encryption (FBE) ■ Storage security: secure file system (SFS); fast trusted storage TrustZone: Qualcomm® Trusted Execution Environment (TEE) v5.3 ■ DRM: Widevine V16 L1, HDCP v2.3 ■ QTEE services: ISDB-T, IP protection, camera security, trusted UI, DSP security, device attestation, connection security, trusted location, and RTIC
Boot sources	■ Supports the following boot sources: □ Universal serial bus (USB) □ Universal flash storage (UFS) □ Embedded multimedia card (eMMC) ■ Supports force boot from USB with dedicated GPIO to trigger
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz clock crystal oscillator (CXO) ■ General-purpose outputs: MN counter and PDM

2 Pin definitions

This topic explains the pin assignments of the QCS6490 and QCS5430 chipsets. The figure and table within this topic provide details on pinouts, pad attributes, and their corresponding definitions.

2.1 I/O parameter definitions

The following table lists pad attributes and their descriptions, pad pull details, and the pad voltage groupings used throughout this topic.

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Internal weak keeper device (keepers cannot drive external buses)
NP	Internal pull
PU	Internal pull-up device
PD	Internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
PX0	Power for pad group 0
PX1	Power for pad group 1
PX2	Pad group 2 (SDC2); 1.8 V or 2.95 V
PX3	Pad group 3 (most peripherals); 1.8 V
PX5	Pad group 5 (UIM1); 1.8 V or 2.95 V
PX6	Pad group 6 (UIM2); 1.8 V or 2.95 V
PX7	Pad group 7 (eMMC); tied to VDD_P7 pins (1.8 V only)

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
PX10	Pad group 10 (UFS_REF_CLK and UFS_RESET); 1.2 V
PX11	Pad group 11 (CXO); 1.2 V
CSI	Supply voltage for MIPI-CSI circuits and I/Os; tied to VDD_A_CSI_X_1P2 (1.2 V)
DSI	Supply voltage for MIPI-DSI circuits and I/Os; tied to VDD_A_DSI_1P2 (1.2 V)

2.2 Pin map

The QCS6490 and QCS5430 chipsets are available in the pico scale package (1287 PSP). A high-level view of the pin assignments is shown in the following figure. For more information on package details and to create printed circuit board (PCB) footprint, see Mechanical information.

QCS6490 and QCS5430 *Pin Assignment and GPIO Configuration Spreadsheet* (80-23889-1A) lists all QCS6490 and QCS5430 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

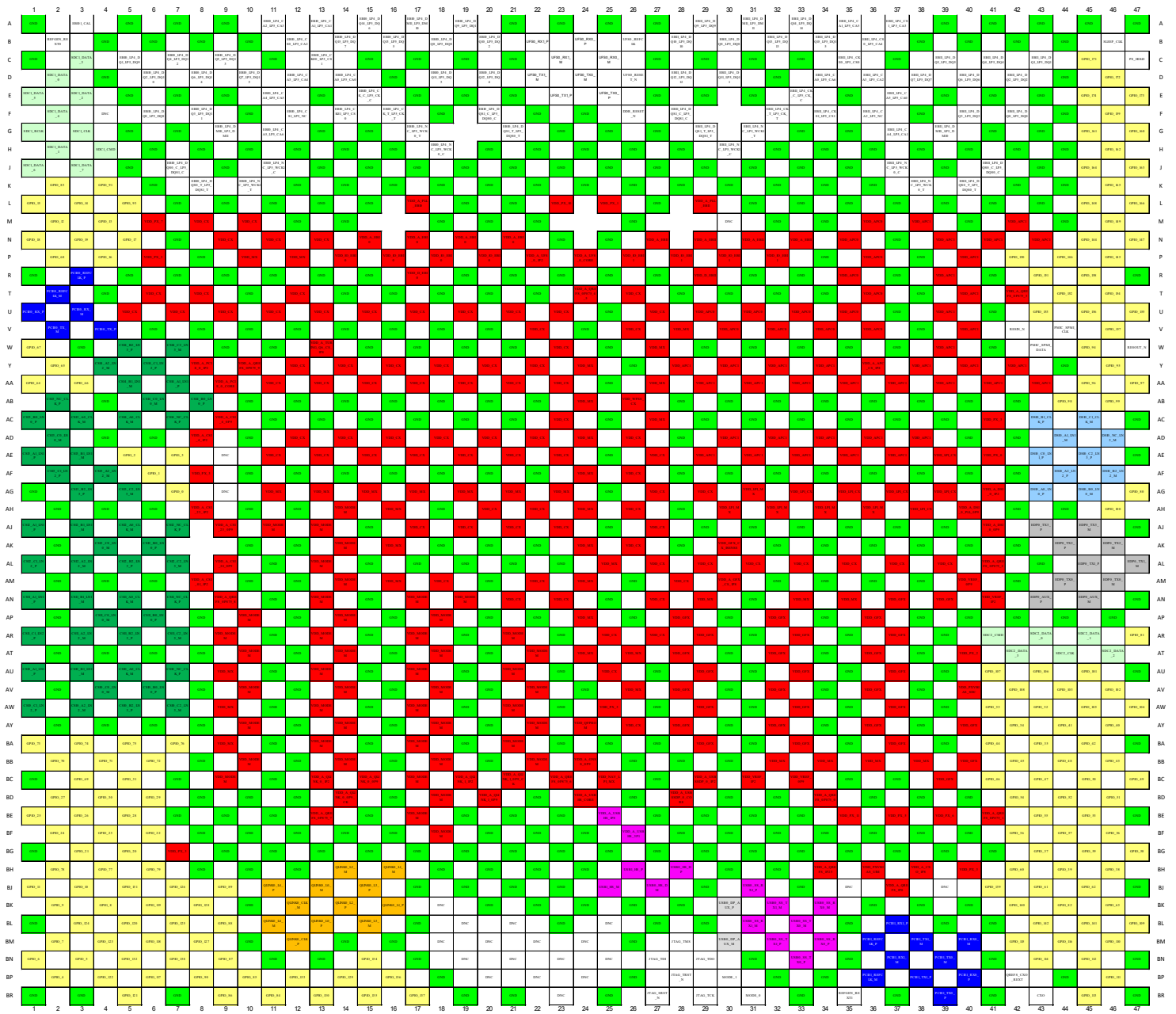


Figure 2-1 QCS6490 and QCS5430 pin assignments

2.3 Pin descriptions

The following table describes the pin functions, pin pull types, and pin voltages. It also provides a mapping of pin numbers and pin names for all the pins on the device. These include general pins, GPIO pins, and power pins.

Table 2-2 Pin descriptions – general pins

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AU5	CSI0_A0_CLK_M	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential clock – negative MIPI-CSI 0 (C-PHY), trio lane 0 – A
AU1	CSI0_A1_LN1_P	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 1 – positive MIPI-CSI 0 (C-PHY), trio lane 1 – A
AW3	CSI0_A2_LN2_M	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 2 – negative MIPI-CSI 0 (C-PHY), trio lane 2 – A
AV6	CSI0_B0_LN0_P	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 0 – positive MIPI-CSI 0 (C-PHY), trio lane 0 – B
AU3	CSI0_B1_LN1_M	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 1 – negative MIPI-CSI 0 (C-PHY), trio lane 1 – B
AW5	CSI0_B2_LN3_P	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 3 – positive MIPI-CSI 0 (C-PHY), trio lane 2 – B
AV4	CSI0_C0_LN0_M	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 0 – negative MIPI-CSI 0 (C-PHY), trio lane 0 – C
AW1	CSI0_C1_LN2_P	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 2 – positive MIPI-CSI 0 (C-PHY), trio lane 1 – C
AW7	CSI0_C2_LN3_M	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential lane 3 – negative MIPI-CSI 0 (C-PHY), trio lane 2 – C
AU7	CSI0_NC_CLK_P	CSI	AI AI, AO	MIPI-CSI 0 (D-PHY), differential clock – positive MIPI-CSI 0 (C-PHY), no connect
AN5	CSI1_A0_CLK_M	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential clock – negative MIPI-CSI 1 (C-PHY), trio lane 0 – A
AN1	CSI1_A1_LN1_P	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 1 – positive MIPI-CSI 1 (C-PHY), trio lane 1 – A
AR3	CSI1_A2_LN2_M	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 2 – negative MIPI-CSI 1 (C-PHY), trio lane 2 – A
AP6	CSI1_B0_LN0_P	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 0 – positive MIPI-CSI 1 (C-PHY), trio lane 0 – B
AN3	CSI1_B1_LN1_M	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 1 – negative MIPI-CSI 1 (C-PHY), trio lane 1 – B
AR5	CSI1_B2_LN3_P	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 3 – positive MIPI-CSI 1 (C-PHY), trio lane 2 – B
AP4	CSI1_C0_LN0_M	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 0 – negative MIPI-CSI 1 (C-PHY), trio lane 0 – C

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AR1	CSI1_C1_LN2_P	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 2 – positive MIPI-CSI 1 (C-PHY), trio lane 1 – C
AR7	CSI1_C2_LN3_M	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential lane 3 – negative MIPI-CSI 1 (C-PHY), trio lane 2 – C
AN7	CSI1_NC_CLK_P	CSI	AI AI, AO	MIPI-CSI 1 (D-PHY), differential clock – positive MIPI-CSI 1 (C-PHY), no connect
AJ5	CSI2_A0_CLK_M	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential clock – negative MIPI-CSI 2 (C-PHY), trio lane 0 – A
AJ1	CSI2_A1_LN1_P	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 1 – positive MIPI-CSI 2 (C-PHY), trio lane 1 – A
AL3	CSI2_A2_LN2_M	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 2 – negative MIPI-CSI 2 (C-PHY), trio lane 2 – A
AK6	CSI2_B0_LN0_P	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 0 – positive MIPI-CSI 2 (C-PHY), trio lane 0 – B
AJ3	CSI2_B1_LN1_M	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 1 – negative MIPI-CSI 2 (C-PHY), trio lane 1 – B
AL5	CSI2_B2_LN3_P	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 3 – positive MIPI-CSI 2 (C-PHY), trio lane 2 – B
AK4	CSI2_C0_LN0_M	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 0 – negative MIPI-CSI 2 (C-PHY), trio lane 0 – C
AL1	CSI2_C1_LN2_P	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 2 – positive MIPI-CSI 2 (C-PHY), trio lane 1 – C
AL7	CSI2_C2_LN3_M	CSI	AI AI, AO	MIPI-CSI 2 (D-PHY), differential lane 3 – negative MIPI-CSI 2 (C-PHY), trio lane 2 – C
AJ7	CSI2_NC_CLK_P	CSI	AI AI, AO	MIPI-CSI 2 (C-PHY), no connect MIPI-CSI 2 (D-PHY), differential clock – positive
AC3	CSI3_A0_CLK_M	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential clock – negative MIPI-CSI 3 (C-PHY), trio lane 0 – A
AE1	CSI3_A1_LN1_P	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 1 – positive MIPI-CSI 3 (C-PHY), trio lane 1 – A
AF4	CSI3_A2_LN2_M	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 2 – negative MIPI-CSI 3 (C-PHY), trio lane 2 – A
AC1	CSI3_B0_LN0_P	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 0 – positive MIPI-CSI 3 (C-PHY), trio lane 0 – B
AE3	CSI3_B1_LN1_M	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 1 – negative MIPI-CSI 3 (C-PHY), trio lane 1 – B
AG3	CSI3_B2_LN3_P	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 3 – positive MIPI-CSI 3 (C-PHY), trio lane 2 – B

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AD2	CSI3_C0_LN0_M	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 0 – negative MIPI-CSI 3 (C-PHY), trio lane 0 – C
AF2	CSI3_C1_LN2_P	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 2 – positive MIPI-CSI 3 (C-PHY), trio lane 1 – C
AG5	CSI3_C2_LN3_M	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential lane 3 – negative MIPI-CSI 3 (C-PHY), trio lane 2 – C
AB2	CSI3_NC_CLK_P	CSI	AI AI, AO	MIPI-CSI 3 (D-PHY), differential clock – positive MIPI-CSI 3 (C-PHY), no connect
AC5	CSI4_A0_CLK_M	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential clock – negative MIPI-CSI 4 (C-PHY), trio lane 0 – A
AA7	CSI4_A1_LN1_P	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 1 – positive MIPI-CSI 4 (C-PHY), trio lane 1 – A
Y4	CSI4_A2_LN2_M	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 2 – negative MIPI-CSI 4 (C-PHY), trio lane 2 – A
AB8	CSI4_B0_LN0_P	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 0 – positive MIPI-CSI 4 (C-PHY), trio lane 0 – B
AA5	CSI4_B1_LN1_M	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 1 – negative MIPI-CSI 4 (C-PHY), trio lane 1 – B
W5	CSI4_B2_LN3_P	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 3 – positive MIPI-CSI 4 (C-PHY), trio lane 2 – B
AB6	CSI4_C0_LN0_M	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 0 – negative MIPI-CSI 4 (C-PHY), trio lane 0 – C
Y6	CSI4_C1_LN2_P	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 2 – positive MIPI-CSI 4 (C-PHY), trio lane 1 – C
W7	CSI4_C2_LN3_M	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential lane 3 – negative MIPI-CSI 4 (C-PHY), trio lane 2 – C
AC7	CSI4_NC_CLK_P	CSI	AI AI, AO	MIPI-CSI 4 (D-PHY), differential clock – positive MIPI-CSI 4 (C-PHY), no connect
BR43	CXO	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
F26	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
BM30	USB0_DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – negative
BK30	USB0_DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – positive
AG43	DSI0_A0_LN0_P	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 0 – positive MIPI-DSI 0 (C-PHY), trio lane 0 – A
AD44	DSI0_A1_LN1_M	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 1 – negative MIPI-DSI 0 (C-PHY), trio lane 1 – A
AF44	DSI0_A2_LN2_P	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 2 – positive MIPI-DSI 0 (C-PHY), trio lane 2 – A

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
AG45	DSI0_B0_LN0_M	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 0 – negative MIPI-DSI 0 (C-PHY), trio lane 0 – B
AC43	DSI0_B1_CLK_P	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential clock – positive MIPI-DSI 0 (C-PHY), trio lane 1 – B
AF46	DSI0_B2_LN2_M	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 2 – negative MIPI-DSI 0 (C-PHY), trio lane 2 – B
AE43	DSI0_C0_LN1_P	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 1 – positive MIPI-DSI 0 (C-PHY), trio lane 0– C
AC45	DSI0_C1_CLK_M	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential clock – negative MIPI-DSI 0 (C-PHY), trio lane 1 – C
AE45	DSI0_C2_LN3_P	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 3 – positive MIPI-DSI 0 (C-PHY), trio lane 2 – C
AD46	DSI0_NC_LN3_M	DSI	AI, AO	MIPI-DSI 0 (D-PHY), differential lane 3 – negative MIPI-DSI 0 (C-PHY), no connect
A3	EBI01_CAL	EBI	AI	EBI 0/1 LPDDRx calibration resistor
D14	EBI0_LP4_CA0_LP5_CA0	EBI	DO	EBI0 LPDDR4X command/address bit 0 EBI0 LPDDR5 command/address bit 0
A13	EBI0_LP4_CA1_LP5_CA1	EBI	DO	EBI0 LPDDR4X command/address bit 1 EBI0 LPDDR5 command/address bit 1
B12	EBI0_LP4_CS0_LP5_CA2	EBI	DO	EBI0 LPDDR4X chip-select 0 EBI0 LPDDR5 command/address bit 2
A11	EBI0_LP4_CA2_LP5_CA3	EBI	DO	EBI0 LPDDR4X command/address bit 2 EBI0 LPDDR5 command/address bit 3
D12	EBI0_LP4_CA3_LP5_CA4	EBI	DO	EBI0 LPDDR4X command/address bit 3 EBI0 LPDDR5 command/address bit 4
E11	EBI0_LP4_CA4_LP5_CA5	EBI	DO	EBI0 LPDDR4X command/address bit 4 EBI0 LPDDR5 command/address bit 5
G11	EBI0_LP4_CA5_LP5_CA6	EBI	DO	EBI0 LPDDR4X command/address bit 5 EBI0 LPDDR5 command/address bit 6
F14	EBI0_LP4_CKE1_LP5_CS0	EBI	DO	EBI0 LPDDR4X clock enable 1 EBI0 LPDDR5 chip-select 0
C13	EBI0_LP4_CKE0_LP5_CS1	EBI	DO	EBI0 LPDDR4X clock enable 0 EBI0 LPDDR5 chip-select 1
F12	EBI0_LP4_CS1_LP5_NC	EBI	DO	EBI0 LPDDR4 chip-select 1
E15	EBI0_LP4_CK_C_LP5_CK_C	EBI	DO	EBI0 LPDDR4X differential clock – negative EBI0 LPDDR5 differential clock – negative
F16	EBI0_LP4_CK_T_LP5_CK_T	EBI	DO	EBI0 LPDDR4X differential clock – positive EBI0 LPDDR5 differential clock – positive

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
A17	EBI0_LP4_DMI1_LP5_DMI0	EBI	DO	EBI0 LPDDR4X data mask inversion 1 EBI0 LPDDR5 data mask inversion 0
G9	EBI0_LP4_DMI0_LP5_DMI1	EBI	DO	EBI0 LPDDR4X data mask inversion 0 EBI0 LPDDR5 data mask inversion 1
F20	EBI0_LP4_DQS1_C_LP5_DQS0_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 negative EBI0 LPDDR5 differential data strobe for byte 0 negative
J7	EBI0_LP4_DQS0_C_LP5_DQS1_C	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 negative EBI0 LPDDR5 differential data strobe for byte 1 negative
G21	EBI0_LP4_DQS1_T_LP5_DQS0_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 1 positive EBI0 LPDDR5 differential data strobe for byte 0 positive
K8	EBI0_LP4_DQS0_T_LP5_DQS1_T	EBI	B	EBI0 LPDDR4X differential data strobe for byte 0 positive EBI0 LPDDR5 differential data strobe for byte 1 positive
B18	EBI0_LP4_DQ8_LP5_DQ0	EBI	B	EBI0 LPDDR4X data bit 8 EBI0 LPDDR5 data bit 0
A19	EBI0_LP4_DQ9_LP5_DQ1	EBI	B	EBI0 LPDDR4X data bit 9 EBI0 LPDDR5 data bit 1
B20	EBI0_LP4_DQ10_LP5_DQ2	EBI	B	EBI0 LPDDR4X data bit 10 EBI0 LPDDR5 data bit 2
D18	EBI0_LP4_DQ11_LP5_DQ3	EBI	B	EBI0 LPDDR4X data bit 11 EBI0 LPDDR5 data bit 3
D20	EBI0_LP4_DQ12_LP5_DQ4	EBI	B	EBI0 LPDDR4X data bit 12 EBI0 LPDDR5 data bit 4
B16	EBI0_LP4_DQ13_LP5_DQ5	EBI	B	EBI0 LPDDR4X data bit 13 EBI0 LPDDR5 data bit 5
A15	EBI0_LP4_DQ14_LP5_DQ6	EBI	B	EBI0 LPDDR4X data bit 14 EBI0 LPDDR5 data bit 6
B14	EBI0_LP4_DQ15_LP5_DQ7	EBI	B	EBI0 LPDDR4X data bit 15 EBI0 LPDDR5 data bit 7
F6	EBI0_LP4_DQ0_LP5_DQ8	EBI	B	EBI0 LPDDR4X data bit 0 EBI0 LPDDR5 data bit 8
C5	EBI0_LP4_DQ1_LP5_DQ9	EBI	B	EBI0 LPDDR4X data bit 1 EBI0 LPDDR5 data bit 9
D6	EBI0_LP4_DQ2_LP5_DQ10	EBI	B	EBI0 LPDDR4X data bit 2 EBI0 LPDDR5 data bit 10

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
F8	EBI0_LP4_DQ3_LP5_DQ11	EBI	B	EBI0 LPDDR4X data bit 3 EBI0 LPDDR5 data bit 11
C7	EBI0_LP4_DQ4_LP5_DQ12	EBI	B	EBI0 LPDDR4X data bit 4 EBI0 LPDDR5 data bit 12
C9	EBI0_LP4_DQ5_LP5_DQ13	EBI	B	EBI0 LPDDR4X data bit 5 EBI0 LPDDR5 data bit 13
D8	EBI0_LP4_DQ6_LP5_DQ14	EBI	B	EBI0 LPDDR4X data bit 6 EBI0 LPDDR5 data bit 14
D10	EBI0_LP4_DQ7_LP5_DQ15	EBI	B	EBI0 LPDDR4X data bit 7 EBI0 LPDDR5 data bit 15
H18	EBI0_LP4_NC_LP5_WCK0_C	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 negative
J11	EBI0_LP4_NC_LP5_WCK1_C	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 negative
G17	EBI0_LP4_NC_LP5_WCK0_T	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 positive
K10	EBI0_LP4_NC_LP5_WCK1_T	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 positive
E37	EBI1_LP4_CA5_LP5_CA0	EBI	DO	EBI1 LPDDR4X command/address bit 5 EBI1 LPDDR5 command/address bit 0
G37	EBI1_LP4_CA4_LP5_CA1	EBI	DO	EBI1 LPDDR4X command/address bit 4 EBI1 LPDDR5 command/address bit 1
D36	EBI1_LP4_CA3_LP5_CA2	EBI	DO	EBI1 LPDDR4X command/address bit 3 EBI1 LPDDR5 command/address bit 2
A37	EBI1_LP4_CS1_LP5_CA3	EBI	DO	EBI1 LPDDR4X chip-select 1 EBI1 LPDDR5 command/address bit 3
B36	EBI1_LP4_CS0_LP5_CA4	EBI	DO	EBI1 LPDDR4X chip-select 0 EBI1 LPDDR5 command/address bit 4
A35	EBI1_LP4_CA1_LP5_CA5	EBI	DO	EBI1 LPDDR4X command/address bit 1 EBI1 LPDDR5 command/address bit 5
D34	EBI1_LP4_CA0_LP5_CA6	EBI	DO	EBI1 LPDDR4X command/address bit 0 EBI1 LPDDR5 command/address bit 6
C35	EBI1_LP4_CKE0_LP5_CS0	EBI	DO	EBI1 LPDDR4X clock enable 0 EBI1 LPDDR5 chip-select 0
F34	EBI1_LP4_CKE1_LP5_CS1	EBI	DO	EBI1 LPDDR4X clock enable 1 EBI1 LPDDR5 chip-select 1
F36	EBI1_LP4_CA2_LP5_NC	EBI	DO	EBI1 LPDDR4X command/address bit 2
E33	EBI1_LP4_CK_C_LP5_CK_C	EBI	DO	EBI1 LPDDR4X differential clock – negative EBI1 LPDDR5 differential clock – negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
F32	EBI1_LP4_CK_T_LP5_CK_T	EBI	DO	EBI1 LPDDR4X differential clock – positive EBI1 LPDDR5 differential clock – positive
G39	EBI1_LP4_DMI0_LP5_DMI0	EBI	DO	EBI1 LPDDR4X data mask 0 EBI1 LPDDR5 data mask 0
A31	EBI1_LP4_DMI1_LP5_DMI1	EBI	DO	EBI1 LPDDR4X data mask 1 EBI1 LPDDR5 data mask 1
J41	EBI1_LP4_DQS0_C_LP5_DQS0_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 negative EBI1 LPDDR5 differential data strobe for byte 0 negative
F28	EBI1_LP4_DQS1_C_LP5_DQS1_C	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 negative EBI1 LPDDR5 differential data strobe for byte 1 negative
K40	EBI1_LP4_DQS0_T_LP5_DQS0_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 0 positive EBI1 LPDDR5 differential data strobe for byte 0 positive
G29	EBI1_LP4_DQS1_T_LP5_DQS1_T	EBI	B	EBI1 LPDDR4X differential data strobe for byte 1 positive EBI1 LPDDR5 differential data strobe for byte 1 positive
F42	EBI1_LP4_DQ0_LP5_DQ0	EBI	B	EBI1 LPDDR4X data bit 0 EBI1 LPDDR5 data bit 0
C43	EBI1_LP4_DQ1_LP5_DQ1	EBI	B	EBI1 LPDDR4X data bit 1 EBI1 LPDDR5 data bit 1
D42	EBI1_LP4_DQ2_LP5_DQ2	EBI	B	EBI1 LPDDR4X data bit 2 EBI1 LPDDR5 data bit 2
F40	EBI1_LP4_DQ3_LP5_DQ3	EBI	B	EBI1 LPDDR4X data bit 3 EBI1 LPDDR5 data bit 3
C41	EBI1_LP4_DQ4_LP5_DQ4	EBI	B	EBI1 LPDDR4X data bit 4 EBI1 LPDDR5 data bit 4
C39	EBI1_LP4_DQ5_LP5_DQ5	EBI	B	EBI1 LPDDR4X data bit 5 EBI1 LPDDR5 data bit 5
D40	EBI1_LP4_DQ6_LP5_DQ6	EBI	B	EBI1 LPDDR4X data bit 6 EBI1 LPDDR5 data bit 6
D38	EBI1_LP4_DQ7_LP5_DQ7	EBI	B	EBI1 LPDDR4X data bit 7 EBI1 LPDDR5 data bit 7
B30	EBI1_LP4_DQ8_LP5_DQ8	EBI	B	EBI1 LPDDR4X data bit 8 EBI1 LPDDR5 data bit 8
A29	EBI1_LP4_DQ9_LP5_DQ9	EBI	B	EBI1 LPDDR4X data bit 9 EBI1 LPDDR5 data bit 9

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
B28	EBI1_LP4_DQ10_LP5_DQ10	EBI	B	EBI1 LPDDR4X data bit 10 EBI1 LPDDR5 data bit 10
D30	EBI1_LP4_DQ11_LP5_DQ11	EBI	B	EBI1 LPDDR4X data bit 11 EBI1 LPDDR5 data bit 11
D28	EBI1_LP4_DQ12_LP5_DQ12	EBI	B	EBI1 LPDDR4X data bit 12 EBI1 LPDDR5 data bit 12
B32	EBI1_LP4_DQ13_LP5_DQ13	EBI	B	EBI1 LPDDR4X data bit 13 EBI1 LPDDR5 data bit 13
A33	EBI1_LP4_DQ14_LP5_DQ14	EBI	B	EBI1 LPDDR4X data bit 14 EBI1 LPDDR5 data bit 14
B34	EBI1_LP4_DQ15_LP5_DQ15	EBI	B	EBI1 LPDDR4X data bit 15 EBI1 LPDDR5 data bit 15
J37	EBI1_LP4_NC_LP5_WCK0_C	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 negative
H30	EBI1_LP4_NC_LP5_WCK1_C	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 negative
K38	EBI1_LP4_NC_LP5_WCK0_T	EBI	DO	EBI1 LPDDR5 differential data clock for byte 0 positive
G31	EBI1_LP4_NC_LP5_WCK1_T	EBI	DO	EBI1 LPDDR5 differential data clock for byte 1 positive
AN45	EDP0_AUX_M	–	B	eDP 1.4 auxiliary channel – negative
AN43	EDP0_AUX_P	–	B	eDP 1.4 auxiliary channel – positive
AM46	EDP0_TX0_M	–	AO	eDP 1.4 transmit channel 0 – negative
AM44	EDP0_TX0_P	–	AO	eDP 1.4 transmit channel 0 – positive
AL47	EDP0_TX1_M	–	AO	eDP 1.4 transmit channel 1 – negative
AL45	EDP0_TX1_P	–	AO	eDP 1.4 transmit channel 1 – positive
AK46	EDP0_TX2_M	–	AO	eDP 1.4 transmit channel 2 – negative
AK44	EDP0_TX2_P	–	AO	eDP 1.4 transmit channel 2 – positive
AJ45	EDP0_TX3_M	–	AO	eDP 1.4 transmit channel 3 – negative
AJ43	EDP0_TX3_P	–	AO	eDP 1.4 transmit channel 3 – positive
BJ25	USB1_HS_M	–	B	USB1_HS – negative
BH26	USB1_HS_P	–	B	USB1_HS – positive
BR31	MODE_0	PX_3	DI	Mode control bit 0 – unconnected for native mode
BP30	MODE_1	PX_3	DI	Mode control bit 1 – unconnected for native mode
T2	PCIE0_REFCLK_M	–	AI, AO	PCIe 0 Gen 3 reference clock – negative
R3	PCIE0_REFCLK_P	–	AI, AO	PCIe 0 Gen 3 reference clock – positive
U3	PCIE0_RX_M	–	AI	PCIe 0 Gen 3 receive – negative
U1	PCIE0_RX_P	–	AI	PCIe 0 Gen 3 receive – positive
V2	PCIE0_TX_M	–	AO	PCIe 0 Gen 3 transmit – negative

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
V4	PCIE0_TX_P	–	AO	PCIe 0 Gen 3 transmit – positive
BP36	PCIE1_REFCLK_M	–	AI, AO	PCIe 1 Gen 3 reference clock – negative
BM36	PCIE1_REFCLK_P	–	AI, AO	PCIe 1 Gen 3 reference clock – positive
BM40	PCIE1_RX0_M	–	AI	PCIe 1 Gen 3 receive lane 0 – negative
BP40	PCIE1_RX0_P	–	AI	PCIe 1 Gen 3 receive lane 0 – positive
BN37	PCIE1_RX1_M	–	AI	PCIe 1 Gen 3 receive lane 1 – negative
BL37	PCIE1_RX1_P	–	AI	PCIe 1 Gen 3 receive lane 1 – positive
BN39	PCIE1_TX0_M	–	AO	PCIe 1 Gen 3 transmit lane 0 – negative
BR39	PCIE1_TX0_P	–	AO	PCIe 1 Gen 3 transmit lane 0 – positive
BM38	PCIE1_TX1_M	–	AO	PCIe 1 Gen 3 transmit lane 1 – negative
BP38	PCIE1_TX1_P	–	AO	PCIe 1 Gen 3 transmit lane 1 – positive
V44	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
W43	PMIC_SPMI_DATA	PX_0	BH-PD:nppukp	Slave and PBUS interface for PMICs – data
C47	PS_HOLD	PX_3	DO	Power-supply hold signal to PMIC
BK12	QLINK0_CLK_M	–	AI, AO	QLink0 clock – negative
BM12	QLINK0_CLK_P	–	AI, AO	QLink0 clock – positive
BH14	QLINK0_L2_M	–	AI, AO	QLink0 lane 2 – negative
BK14	QLINK0_L2_P	–	AI, AO	QLink0 lane 2 – positive
BL11	QLINK0_L4_M	–	AI, AO	QLink0 lane 4 – negative
BJ11	QLINK0_L4_P	–	AI, AO	QLink0 lane 4 – positive
BL15	QLINK0_L3_M	–	AI, AO	QLink0 lane 3 – negative
BJ15	QLINK0_L3_P	–	AI, AO	QLink0 lane 3 – positive
BJ13	QLINK0_L0_M	–	AI, AO	QLink0 lane 0 – negative
BL13	QLINK0_L0_P	–	AI, AO	QLink0 lane 0 – positive
BH16	QLINK0_L1_M	–	AI, AO	QLink0 lane 1 – negative
BK16	QLINK0_L1_P	–	AI, AO	QLink0 lane 1 – positive
BP42	QREFS_CXO_REXT	PX_11	AI, AO	External resistor for on-chip clocking
B2	REFGEN_REXT0	PX_3	AI, AO	East-side high-speed interface – external resistor
BR35	REFGEN_REXT1	PX_3	AI, AO	West-side high-speed interface – external resistor
V42	RESIN_N	PX_0	DI	Reset input
W47	RESOUT_N	PX_3	DO	Reset output
G3	SDC1_CLK	PX_7	DO-NP:pdpukp	Secure digital controller 1 clock
H4	SDC1_CMD	PX_7	B-NP:pdpukp	Secure digital controller 1 command

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
D2	SDC1_DATA0	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 0
H2	SDC1_DATA1	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 1
E3	SDC1_DATA2	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 2
C3	SDC1_DATA3	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 3
F2	SDC1_DATA4	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 4
E1	SDC1_DATA5	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 5
J1	SDC1_DATA6	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 6
J3	SDC1_DATA7	PX_7	B-NP:pdpukp	Secure digital controller 1 data bit 7
G1	SDC1_RCLK	PX_7	DI-PD:pdpukp	Secure digital controller 1 return clock
AT44	SDC2_CLK	PX_2	DO-NP:pdpukp	Secure digital controller 2 clock
AR41	SDC2_CMD	PX_2	BH-NP:pdpukp	Secure digital controller 2 command
AR43	SDC2_DATA0	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 0
AR45	SDC2_DATA1	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 1
AT46	SDC2_DATA2	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 2
AT42	SDC2_DATA3	PX_2	BH-NP:pdpukp	Secure digital controller 2 data bit 3
B46	SLEEP_CLK	PX_3	DI	Sleep clock
BR27	JTAG_SRST_N	PX_3	DI-PU:nppdkp	JTAG reset for debug

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pad name and/or function	Pad characteristics [a]		Functional description
		Voltage	Type	
BR29	JTAG_TCK	PX_3	DI-PU:nppdkp	JTAG clock input
BN27	JTAG_TDI	PX_3	DI-PU:nppdkp	JTAG data input
BN29	JTAG_TDO	PX_3	DO-Z	JTAG data output
BM28	JTAG_TMS	PX_3	DI-PU:nppdkp	JTAG mode select input
BP28	JTAG_TRST_N	PX_3	DI-PU:nppdkp	JTAG reset
C25	UFS_RX0_M	–	AI	UFS lane 0 receiver – negative
B24	UFS_RX0_P	–	AI	UFS lane 0 receiver – positive
D24	UFS_TX0_M	–	AO	UFS lane 0 transmit – negative
E25	UFS_TX0_P	–	AO	UFS lane 0 transmit – positive
C23	UFS_RX1_M	–	AI	UFS lane 1 receiver – negative
B22	UFS_RX1_P	–	AI	UFS lane 1 receiver – positive
D22	UFS_TX1_M	–	AO	UFS lane 1 transmit – negative
E23	UFS_TX1_P	–	AO	UFS lane 1 transmit – positive
B26	UFS0_REFCLK	PX_10	DO-Z:PD:nppukp	UFS reference clock
D26	UFS0_RESET_N	PX_10	DO-Z:PD:nppukp	UFS reset
BJ27	USB0_HS_DM	–	AI, AO	USB 2.0 high-speed data – negative
BH28	USB0_HS_DP	–	AI, AO	USB 2.0 high-speed data – positive
BK34	USB0_SS_RX0_M	–	AI	USB 3.0 Type-C PHY receiver 0 – negative
BM34	USB0_SS_RX0_P	–	AI	USB 3.0 Type-C PHY receiver 0 – positive
BL31	USB0_SS_RX1_M	–	AI	USB 3.0 Type-C PHY receiver 1 – negative
BJ31	USB0_SS_RX1_P	–	AI	USB 3.0 Type-C PHY receiver 1 – positive
BL33	USB0_SS_TX0_M	–	AO	USB 3.0 Type-C PHY transmit 0 – negative
BN33	USB0_SS_TX0_P	–	AO	USB 3.0 Type-C PHY transmit 0 – positive
BK32	USB0_SS_TX1_M	–	AO	USB 3.0 Type-C PHY transmit 1 – negative
BM32	USB0_SS_TX1_P	–	AO	USB 3.0 Type-C PHY transmit 1 – positive

[a] For parameter and acronym definitions, see Table 2-1.

NOTE
- GPIO pins can support multiple functions. To assign GPIOs to particular functions as in Table 2-2, identify all application requirements and map each GPIO to its function. Ensure to avoid GPIO assignment conflicts. See the following table for a list of all supported functions for each GPIO.
- Some GPIOs can wake up the SoC from sleep. For more information, see Table 2-3.

To avoid excessive current leakage, examine each GPIO external connection and programmed configuration. Ensure control of the following factors:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high impedance (tri-state) outputs
  - Unattached connections to external devices

For GPIO assignments, see QCS6490 and QCS5430 *Pin Assignment and GPIO Configuration Spreadsheet* (80-23889-1A). It lists all pad name and/or function for QCS6490 and QCS5430 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
AG7	GPIO_0		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP 0 SE0, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO	
		I3C_SDA		B	QUP 0 SE0, lane 0: I3C_SDA	
AF6	GPIO_1		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP 0 SE0, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 0 SE0, lane 1: I3C_SCL	
AE5	GPIO_2		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP 0 SE0, lane 2: UART_TX	
		SPI_SCLK		DO	QUP 0 SE0, lane 2: SPI_SCLK	
		SPI_CS_1		DO	QUP 0 SE7, lane 4: SPI_CS_1	
		QDSS_GPIO_TRACEDATA_LOCA[0]		DO	QDSS trace data bit 0 A	
AE7	GPIO_3		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE0, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE0, lane 3: SPI_CS_0	
		SPI_CS_2		DO	QUP0 SE7, lane 5: SPI_CS_2	
		QDSS_GPIO_TRACEDATA_LOCA[1]		DO	QDSS trace data bit 1 A	
BP2	GPIO_4		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE1, lane 0 UART_CTS	
		I2C_SDA		B	QUP0 SE1, lane 0 I2C_SDA	
		SPI_MISO		DI	QUP0 SE1, lane 0 SPI_MISO	
		I3C_SDA		B	QUP 0 SE1, lane 0: I3C_SDA	
BN3	GPIO_5		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE1, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE1, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE1, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 0 SE1, lane 1: I3C_SCL	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BN1	GPIO_6		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE1, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE1, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP0 SE7, lane 6: SPI_CS_3	
BM2	GPIO_7		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE1, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE1, lane 3: SPI_CS_0	
BK4	GPIO_8		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE2, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE2, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE2, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA[2]		DO	QDSS trace data bit 2 A	
BK2	GPIO_9		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE2, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE2, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE2, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA[3]		DO	QDSS trace data bit 3 A	
BJ3	GPIO_10		PX_3	PD:nppukp	Configurable I/O	N
		GNSS_L1_ELNA_EN		DO	eLNA enable for L1	
		UART_TX		DO	QUP0 SE2, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE2, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA[4]		DO	QDSS trace data bit 4 A	
BJ1	GPIO_11		PX_3	PD:nppukp	Configurable I/O	Y
		GNSS_L2_L5_ELNA_EN		DO	eLNA enable for L2_L5	
		UART_RX		DI	QUP0 SE2, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE2, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA[5]		DO	QDSS trace data bit 5 A	
M2	GPIO_12		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE3, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE3, lane 0: I2C_SDA	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		SPI_MISO		DI	QUP0 SE3, lane 0: SPI_MISO	
		QDSS_GPIO_TRACECTL_LOCA		DO	QDSS trace control A	
M4	GPIO_13		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE3, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE3, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE3, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACECLK_LOCA		DO	QDSS trace clock A	
L3	GPIO_14		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE3, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE3, lane 2: SPI_SCLK	
		BOOT_CONFIG[12]		DI	Boot configuration control bit 12	
L1	GPIO_15		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE3, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE3, lane 3: SPI_CS_0	
		QDSS_CTI_TRIG0_OUT_MIRA		DO	QDSS trigger output 0 A	
		BOOT_CONFIG[9]		DI	Boot configuration control bit 9	
P4	GPIO_16		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE4, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE4, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE4, lane 0: SPI_MISO	
		QDSS_CTI_TRIG1_OUT_MIRA		DO	QDSS trigger output 1 A	
N5	GPIO_17		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE4, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE4, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE4, lane 1: SPI_MOSI	
N1	GPIO_18		PX_3	PD:nppukp	Configurable I/O	Y
		UART_TX		DO	QUP0 SE4, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE4, lane 2: SPI_SCLK	
		QDSS_CTI_TRIG1_IN_MIRA		DI	QDSS trigger input 1 A	
N3	GPIO_19		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_RX		DI	QUP0 SE4, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE4, lane 3: SPI_CS_0	
BG5	GPIO_20		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE5, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE5, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE5, lane 0: SPI_MISO	
		CCI_TIMER0		DO	Camera control interface timer	
		QDSS_GPIO_TRACEDATA_LOCA[6]		DO	QDSS trace data 6	
BG3	GPIO_21		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP0 SE5, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE5, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP 0 SE5, lane 1: SPI_MOSI	
		CCI_TIMER1		DO	Camera control interface timer 1	
		QDSS_GPIO_TRACEDATA_LOCA[7]		DO	QDSS trace data 7	
BF6	GPIO_22		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE5, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE5, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data 8	
BF4	GPIO_23		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE5, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE5, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data 9	
BF2	GPIO_24		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE6, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE6, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE6, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA[10]		DO	QDSS trace data bit 10 A	
BE1	GPIO_25		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP0 SE6, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE6, lane 1: I2C_SCL	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		SPI_MOSI		DO	QUP0 SE6, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA[11]		DO	QDSS trace data bit 11 A	
BE3	GPIO_26		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP0 SE6, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE6, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACEDATA_LOCA[12]		DO	QDSS trace data bit 12 A	
BD2	GPIO_27		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE6, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACEDATA_LOCA[13]		DO	QDSS trace data 13	
BE5	GPIO_28		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP0 SE7, lane 0: UART_CTS	
		I2C_SDA		B	QUP0 SE7, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP0 SE7, lane 0: SPI_MISO	
		QDSS_GPIO_TRACEDATA_LOCA[14]		DO	QDSS trace data 14	
BD6	GPIO_29		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP0 SE7, lane 1: UART_RFR	
		I2C_SCL		DO	QUP0 SE7, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP0 SE7, lane 1: SPI_MOSI	
		QDSS_GPIO_TRACEDATA_LOCA[15]		DO	QDSS trace data bit 15 A	
BD4	GPIO_30		PX_3	PU:nppdkp	Configurable I/O	N
		UART_TX		DO	QUP0 SE7, lane 2: UART_TX	
		SPI_SCLK		DO	QUP0 SE7, lane 2: SPI_SCLK	
BC5	GPIO_31		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP0 SE7, lane 3: UART_RX	
		SPI_CS_0		DO	QUP0 SE7, lane 3: SPI_CS_0	
AW43	GPIO_32		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE0, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE0, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE0, lane 0: SPI_MISO	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		QUP_SPMI_DATA		B		
AW41	GPIO_33		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE0, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE0, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE0, lane 1: SPI_MOSI	
		QUP_SPMI_CLK		DO		
AY42	GPIO_34		PX_3	PD:nppukp	Configurable I/O	Y
		UART_TX		DO	QUP1 SE0, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE0, lane 2: SPI_SCLK	
BA43	GPIO_35		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE0, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE0, lane 3: SPI_CS_0	
BF42	GPIO_36		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE1, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE1, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE1, lane 0: SPI_MISO	
		I3C_SDA		B	QUP 1SE1, lane 0: I3C_SDA	
BG43	GPIO_37		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE1, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE1, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE1, lane 1: SPI_MOSI	
		I3C_SCL		DO	QUP 1SE1, lane 1: I3C_SCL	
BH46	GPIO_38		PX_3	PU:nppdkp	Configurable I/O	N
		UART_TX		DO	QUP1 SE1, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE1, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP1 SE4, lane 6: SPI_CS_3	
BH44	GPIO_39		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE1, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE1, lane 3: SPI_CS_0	
AY46	GPIO_40		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_CTS		DI	QUP1 SE2, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE2, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE2, lane 0: SPI_MISO	
AY44	GPIO_41		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE2, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE2, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE2, lane 1: SPI_MOSI	
BA45	GPIO_42		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE2, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE2, lane 2: SPI_SCLK	
BB46	GPIO_43		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE2, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE2, lane 3: SPI_CS_0	
BA41	GPIO_44		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE3, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE3, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE3, lane 0: SPI_MISO	
BB42	GPIO_45		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE3, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE3, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE3, lane 1: SPI_MOSI	
BC41	GPIO_46		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE3, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE3, lane 2: SPI_SCLK	
BC43	GPIO_47		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE3, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE3, lane 3: SPI_CS_0	
		DP_HOT_PLUG_DETECT		DI	DisplayPort hot plug detect	
BB44	GPIO_48		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE4, lane 0: UART_CTS	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		I2C_SDA		B	QUP1 SE4, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE4, lane 0: SPI_MISO	
BC47	GPIO_49		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE4, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE4, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE4, lane 1: SPI_MOSI	
BC45	GPIO_50		PX_3	PD-nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE4, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE4, lane 2: SPI_SCLK	
		SPI_CS_3		DO	QUP1 SE6, lane 6: SPI_CS_3	
BD46	GPIO_51		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE4, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE4, lane 3: SPI_CS_0	
BD44	GPIO_52		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE5, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE5, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE5, lane 0: SPI_MISO	
BE45	GPIO_53		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE5, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE5, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE5, lane 1: SPI_MOSI	
BD42	GPIO_54		PX_3	PD:nppukp	Configurable I/O	Y
		UART_TX		DO	QUP1 SE5, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE5, lane 2: SPI_SCLK	
		SPI_CS_2		DO	QUP1 SE4, lane 5: SPI_CS_2	
BE43	GPIO_55		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE5, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE5, lane 3: SPI_CS_0	
		SPI_CS_1		DO	QUP1 SE4, lane 4: SPI_CS_1	
BF46	GPIO_56		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_CTS		DI	QUP1 SE6, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE6, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE6, lane 0: SPI_MISO	
BF44	GPIO_57		PX_3	PD:nppukp	Configurable I/O	N
		UART_RFR		DO	QUP1 SE6, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE6, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE6, lane 1: SPI_MOSI	
BG47	GPIO_58		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE6, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE6, lane 2: SPI_SCLK	
		QDSS_GPIO_TRACECTL_LOCB		DO	QDSS trace control B	
BG45	GPIO_59		PX_3	PU:nppdkp	Configurable I/O	Y
		UART_RX		DI	QUP1 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE6, lane 3: SPI_CS_0	
		QDSS_GPIO_TRACECLK_LOCB		DO	QDSS trace clock B	
BH42	GPIO_60		PX_3	PD:nppukp	Configurable I/O	Y
		UART_CTS		DI	QUP1 SE7, lane 0: UART_CTS	
		I2C_SDA		B	QUP1 SE7, lane 0: I2C_SDA	
		SPI_MISO		DI	QUP1 SE7, lane 0: SPI_MISO	
		EDP_HOT_PLUG_DETECT		DI	eDP hot plug detect	
BJ43	GPIO_61		PX_3	PD:nppukp	Configurable I/O	Y
		UART_RFR		DO	QUP1 SE7, lane 1: UART_RFR	
		I2C_SCL		DO	QUP1 SE7, lane 1: I2C_SCL	
		SPI_MOSI		DO	QUP1 SE7, lane 1: SPI_MOSI	
		SD_WRITE_PROTECT		DO	Secure digital card write protection	
BJ45	GPIO_62		PX_3	PD:nppukp	Configurable I/O	N
		UART_TX		DO	QUP1 SE7, lane 2: UART_TX	
		SPI_SCLK		DO	QUP1 SE7, lane 2: SPI_SCLK	
		SPI_CS_1		DO	QUP1 SE6, lane 4: SPI_CS_1	
BK46	GPIO_63		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		UART_RX		DI	QUP1 SE6, lane 3: UART_RX	
		SPI_CS_0		DO	QUP1 SE6, lane 3: SPI_CS_0	
		SPI_CS_2		DO	QUP1 SE6, lane 5: SPI_CS_2	
		BOOT_CONFIG[11]		DI	Boot configuration control bit 11	
AA1	GPIO_64		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK0		DO	Camera master clock 0	
Y2	GPIO_65		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK1		DO	Camera master clock 1	
AA3	GPIO_66		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK2		DO	Camera master clock 2	
W1	GPIO_67		PX_3	PD:nppukp	Configurable I/O	N
		CAM_MCLK3		DO	Camera master clock 3	
P2	GPIO_68		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK4		DO	Camera master clock 4	
BC3	GPIO_69		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0		B	Dedicated camera control interface I²C serial data	
BB2	GPIO_70		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0		DO	Dedicated camera control interface I²C clock	
BB4	GPIO_71		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA1		B	Dedicated camera control interface I²C 1 serial data	
BB6	GPIO_72		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SCL1		DO	Dedicated camera control interface I²C 1 clock	
BA1	GPIO_73		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2		B	Dedicated camera control interface I²C 2 serial data	
BA3	GPIO_74		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2		DO	Dedicated camera control interface I²C 2 clock	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BA5	GPIO_75		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SDA3		B	Dedicated camera control interface I²C 3 serial data	
BA7	GPIO_76 [b]		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL3		DO	Dedicated camera control interface I²C 3 clock	
		GCC_GP1_CLK_MIRB		DO	Global general-purpose clock 1 B	
BH4	GPIO_77 [b]		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER2		DO	Camera control interface timer 2	
		GCC_GP2_CLK_MIRB		DO	General-purpose clock	
BH2	GPIO_78 [b]		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_TIMER3		DO	Camera control interface timer 3	
		CCI_ASYNC_IN1		DI	Camera control interface async 1	
		GCC_GP3_CLK_MIRB		DO	General-purpose clock	
BH6	GPIO_79		PX_3	PU:nppdkp	Configurable I/O	Y
		CCI_TIMER4		DO	Camera control interface timer 4	
		CCI_ASYNC_IN2		DI	Camera control interface async 2	
		PCIE1_CLKREQN		DI	PCIe1 clock request signal	
		MDP_VSYNC_E		DI	MDP vertical sync – external	
AG47	GPIO_80		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_P_MIRA		DI	MDP vertical sync – primary	
		MDP_VSYNC0_OUT		DO	MDP vertical sync 0 output	
		MDP_VSYNC1_OUT		DO	MDP vertical sync 1 output	
		MDP_VSYNC4_OUT		DO	MDP vertical sync 4 output	
AR47	GPIO_81		PX_3	PD:nppukp	Configurable I/O	Y
		MDP_VSYNC_S_MIRA		DI	MDP vertical sync – secondary	
		MDP_VSYNC2_OUT		DO	MDP vertical sync 2 output	
		MDP_VSYNC3_OUT		DO	MDP vertical sync 3 output	
		MDP_VSYNC5_OUT		DO	MDP vertical sync 5 output	
BK44	GPIO_82		PX_3	PD:nppukp	Configurable I/O	Y

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		FORCED_USB_BOOT		DI	Forced USB boot	
K2	GPIO_83		PX_3	PD:nppukp	Configurable I/O	Y
		BOOT_CONFIG[8]		DI	Boot configuration control bit 8	
BR11	GPIO_84		PX_3	PD:nppukp	Configurable I/O	N
		USB2PHY_AC_EN0		DO	USB AC coupling 0 control	
BP10	GPIO_85		PX_3	PD:nppukp	Configurable I/O	N
		USB2PHY_AC_EN1		DO	USB AC coupling 1 control	
BR9	GPIO_86	–	PX_3	PD:nppukp	Configurable I/O	Y
BN9	GPIO_87	–	PX_3	PD:nppukp	Configurable I/O	N
BL9	GPIO_88		PX_3	PU:nppdkp	Configurable I/O	Y
		PCIE0_CLKREQN		DI	PCIe clock request	
BJ9	GPIO_89	–	PX_3	PD:nppukp	Configurable I/O	Y
BP8	GPIO_90	–	PX_3	PD:nppukp	Configurable I/O	Y
K4	GPIO_91	–	PX_3	PD:nppukp	Configurable I/O	Y
L5	GPIO_93		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK5		DO	Camera master clock 5	
		CCI_ASYNC_IN0		DI	Camera control interface async	
		BOOT_CONFIG[13]		DI	Boot configuration control bit 13	
W45	GPIO_94		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_SLIMBUS_CLK		B	Low-power audio SLIMbus clock	
Y46	GPIO_95		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_SLIMBUS_DATA0		B	Low-power audio SLIMbus data 0	
AA45	GPIO_96		PX_3	PD:nppukp	Configurable I/O	N
		PRI_MI2S_MCLK		DO	Primary MI2S master clock	
AA47	GPIO_97		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_SCK		DO	MI2S 0 clock	
AB44	GPIO_98		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_DATA0		B	MI2S 0 serial data channel 0	
AB46	GPIO_99		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		MI2S0_DATA1		B	MI2S 0 serial data channel 1	
AH46	GPIO_100		PX_3	PD:nppukp	Configurable I/O	N
		MI2S0_WS		B	MI2S 0 serial data word select	
AU45	GPIO_101		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_SCK		B	MI2S 2 clock	
		QDSS_GPIO_TRACEDATA_LOCB[0]		DO	QDSS trace data bit 0 B	
AV46	GPIO_102		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_DATA0		B	MI2S 2 serial data channel 0	
		GP_PDM_MIRA[0]		DO	General-purpose PDM output 0 A	
		QDSS_GPIO_TRACEDATA_LOCB[1]		DO	QDSS trace data bit 1 B	
AV44	GPIO_103		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_WS		B	MI2S 2 serial data word select	
		GP_PDM_MIRA[1]		DO	General-purpose PDM output 1 A	
		QDSS_GPIO_TRACEDATA_LOCB[2]		DO	QDSS trace data bit 2 B	
AW47	GPIO_104		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S2_DATA1		B	MI2S 2 serial data channel 1	
		GP_PDM_MIRA[2]		DO	General-purpose PDM output 2 A	
		QDSS_GPIO_TRACEDATA_LOCB[3]		DO	QDSS trace data bit 3	
AW45	GPIO_105 [b]		PX_3	PD:nppukp	Configurable I/O	N
		SEC_MI2S_MCLK		DO	Secondary MI2S master clock	
		MI2S1_DATA1		B	MI2S 1 serial data channel 1	
		AUDIO_REF_CLK		DI	Audio reference clock	
		GCC_GP1_CLK_MIRA		A	General-purpose clock 1 A	
		QDSS_GPIO_TRACEDATA_LOCB[4]		DO	QDSS trace data bit 4 B	
AU43	GPIO_106 [b]		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_SCK		B	MI2S 1 clock	
		GCC_GP2_CLK_MIRA		DO	General-purpose clock 2 A	
		QDSS_GPIO_TRACEDATA_LOCB[5]		DO	QDSS trace data bit 5 B	
AU41	GPIO_107 [b]		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_DATA0		B	MI2S 1 serial data channel 0	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		GCC_GP3_CLK_MIRA		DO	General-purpose clock 3 A	
		QDSS_GPIO_TRACEDATA_LOCB[6]		DO	QDSS trace data bit 6 B	
AV42	GPIO_108		PX_3	PD:nppukp	Configurable I/O	N
		MI2S1_WS		B	MI2S 1 serial word select	
		QDSS_GPIO_TRACEDATA_LOCB[7]		DO	QDSS trace data bit 7 B	
BL47	GPIO_109		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_DATA		B	UIM1 data (dual voltage)	
BM46	GPIO_110		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_CLK		DO	UIM1 clock (dual voltage)	
BP46	GPIO_111		PX_6	PD:nppukp	Configurable I/O	N
		UIM1_RESET		DO	UIM1 reset (dual voltage)	
BN45	GPIO_112		PX_3	PD:nppukp	Configurable I/O	Y
		UIM1_PRESENT		DI	UIM1 presence detection	
BR45	GPIO_113		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_DATA		B	UIM0 data (dual voltage)	
BN43	GPIO_114		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_CLK		DO	UIM0 clock (dual voltage)	
BM42	GPIO_115		PX_5	PD:nppukp	Configurable I/O	N
		UIM0_RESET		DO	UIM0_RESET	
BM44	GPIO_116		PX_3	PD:nppukp	Configurable I/O	Y
		UIM0_PRESENT		DI	UIM0 presence detection	
BP6	GPIO_117		PX_3	PD:nppukp	Configurable I/O	Y
		RFFE0_CLK		DO	RF front-end interface clock	
BM6	GPIO_118		PX_3	PD:nppukp	Configurable I/O	N
		RFFE0_DATA		B	RF front-end 0 interface data	
		BOOT_CONFIG[0]		DI	Boot configuration control bit 0	
BK6	GPIO_119	–	PX_3	PD:nppukp	Configurable I/O	Y
BL5	GPIO_120		PX_3	PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[1]		DI	Boot configuration control bit 1	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
BR5	GPIO_121	–	PX_3	PD:nppukp	Configurable I/O	Y
BP4	GPIO_122		PX_3	>PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[2]		DI	Boot configuration control bit 2	
BM4	GPIO_123	–	PX_3	PD:nppukp	Configurable I/O	Y
BL3	GPIO_124		PX_3	PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[3]		DI	Boot configuration control bit 3	
BL7	GPIO_125	–	PX_3	PD:nppukp	Configurable I/O	Y
BJ7	GPIO_126		PX_3	PD:nppukp	Configurable I/O	N
		BOOT_CONFIG[4]		DI	Boot configuration control bit 4	
BM8	GPIO_127		PX_3	PD:nppukp	Configurable I/O	Y
		WLAN_COEX_UART1_RX		DI	Interface between WCN and QCS6490	
BK8	GPIO_128		PX_3	PD:nppukp	Configurable I/O	Y
		WLAN_COEX_UART1_TX		DO	Interface between WCN and QCS6490	
		BOOT_CONFIG[10]		DI	Boot configuration control bit 10	
BP14	GPIO_129		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_0		B	Generic input/output 0 for GNSS	
BR13	GPIO_130		PX_3	PD:nppukp	Configurable I/O	Y
		NAV_GPIO_1		B	Generic input/output 1 for GNSS	
		BOOT_CONFIG[7]		DI	Boot configuration control bit 7	
BJ5	GPIO_131		PX_3	PD:nppukp	Configurable I/O	Y
		PA_INDICATOR_1_OR_2		DO	PA transmit indicator	
		NAV_GPIO_2		B	Generic input/output 2 for GNSS	
		BOOT_CONFIG[5]		DI	Boot configuration control bit 5	
BN5	GPIO_132		PX_3	PD:nppukp	Configurable I/O	N
		GRFC0_MIRA		DO	Generic RF controller bit 0 A	
		BOOT_CONFIG[6]		DI	Boot configuration control bit 6	
BP12	GPIO_133		PX_3	PD:nppukp	Configurable I/O	Y
		QLINK0_REQUEST		DI	QLink0 request	
BN15	GPIO_134		PX_3	PD:nppukp	Configurable I/O	N

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		QLINK0_ENABLE		DO	QLink0 enable	
BR15	GPIO_135		PX_3	PD:nppukp	Configurable I/O	N
		QLINK0_WMSS_RESET_N		DO	QLINK0 SDR subsystem reset output	
		BOOT_CONFIG[14]		DI	Boot configuration control bit 14	
BP16	GPIO_136	–	PX_3	PD:nppukp	Configurable I/O	Y
BR17	GPIO_137	–	PX_3	PD:nppukp	Configurable I/O	N
BN7	GPIO_138		PX_3		Configurable I/O	N
		BOOT_CONFIG[15]		DI	Boot configuration control bit 15	
BJ41	GPIO_139		PX_3	PD:nppukp	Configurable I/O	N
		FORCED_USB_BOOT_POLARITY_ SEL		DI	Forced USB boot parity select	
BK42	GPIO_140		PX_3	PD:nppukp	Configurable I/O	Y
		USB_PHY_PS		DI	USB PHY port select	
BL45	GPIO_141	–	PX_3	PD:nppukp	Configurable I/O	Y
BL43	GPIO_142	–	PX_3	PD:nppukp	Configurable I/O	Y
N45	GPIO_144		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_0 [c]		B	LPI GPIO 0	
		SWR_TX_CLK		DO	SoundWire transmit clock	
		LPI_QUA_MI2S_SCK		B	LPI quaternary MI2S clock	
P46	GPIO_145		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_1		B	LPI GPIO 1	
		SWR_TX_DATA0		DO	SoundWire transmit data 0	
		LPI_QUA_MI2S_WS		B	LPI quaternary MI2S word select	
P44	GPIO_146		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_2		B	LPI GPIO 2	
		SWR_TX_DATA1		DO	SoundWire transmit data 1	
		LPI_QUA_MI2S_DATA0		B	LPI quaternary MI2S data 0	
N47	GPIO_147		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_3		B	LPI GPIO 3	
		SWR_RX_CLK		DI	SoundWire receive clock	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_QUA_MI2S_DATA1		B	LPI quaternary MI2S data 1	
L45	GPIO_148		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_4		B	LPI GPIO 4	
		SWR_RX_DATA0		DI	SoundWire receive data 0	
		LPI_QUA_MI2S_DATA2		B	LPI quaternary MI2S data 2	
M46	GPIO_149		PX_3	PD:nppuk	Configurable I/O	N
		LPI_GPIO_5		B	LPI GPIO 5	
		SWR_RX_DATA1		DI	SoundWire receive data 1	
		EXT_MCLK1_C		DO	External master clock 1 C	
		LPI_QUA_MI2S_DATA3		B	LPI quaternary MI2S data 3	
P42	GPIO_150		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data bit 8 A	
		LPI_GPIO_6		B	LPI GPIO 6	
		LPI_DMIC1_CLK		DO	LPI DMIC 1 Clock	
		LPI_I2S1_CLK		B	LPI I2S 1 clock	
R43	GPIO_151		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data bit 9 A	
		LPI_GPIO_7		B	LPI GPIO 7	
		LPI_DMIC1_DATA		DI	LPI DMIC 1 data	
		LPI_I2S1_WS		B	LPI I2S 1 word select	
T44	GPIO_152		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEdata_LOCA[10]		DO	QDSS trace data bit 10 A	
		LPI_GPIO_8		B	LPI GPIO 8	
		LPI_DMIC2_CLK		DO	LPI DMIC 2 clock	
		LPI_I2S1_data0		B	LPI I2S 1 data 0	
U43	GPIO_153		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEdata_LOCA[11]		DO	QDSS trace data bit 11 A	
		LPI_GPIO_9		B	LPI GPIO 9	
		LPI_DMIC2_DATA		DI	LPI DMIC 2 data	
		LPI_I2S1_DATA1		B	LPI I2S 1 data 1	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		EXT_MCLK1_B		DO	External master clock 1 B	
T46	GPIO_154		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_10		B	LPI GPIO 10	
		LPI_I2S2_CLK		B	LPI MI2S 2 clock	
		WSA_SWR_CLK		DO	SoundWire clock for WSA	
U47	GPIO_155		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_11		B	LPI GPIO 11	
		LPI_I2S2_WS		B	LPI I2S 2 Word select	
		WSA_SWR_DATA		B	SoundWire data for WSA	
U45	GPIO_156		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG0_IN_MIRB		DI	QDSS trigger input 0 B	
		LPI_GPIO_12		B	LPI GPIO 12	
		LPI_DMIC3_CLK		DO	LPI DMIC 3 clock	
		LPI_I2S2_DATA0		B	LPI I2S 2 data 0	
V46	GPIO_157		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG1_IN_MIRB		DI	QDSS trigger input 1 B	
		LPI_GPIO_13		B	LPI GPIO 13	
		LPI_DMIC3_DATA		DO	LPI DMIC 3 data	
		LPI_I2S2_DATA1		B	LPI I2S 2 data 1	
		EXT_MCLK1_A		DO	External master clock 1 A	
R45	GPIO_158		PX_3	PD:nppukp	Configurable I/O	Y
		LPI_GPIO_14		B	LPI GPIO 14	
		SWR_TX_DATA2		DO	SoundWire transmit data 2	
F46	GPIO_159		PX_3	PD:nppuk	Configurable I/O	N
		LPI_GPIO_15 [d]		B	LPI GPIO 15	
		LPI_I2C_SDA		B	LPI_QUP0 SE0, lane 0: I2C_SDA	
		LPI_I3C_SDA		B	LPI_QUP0 SE0, lane 0: I3C_SDA	
		SYNC_OUT_GPIO_0		DO	Sync out GPIO_0	
G47	GPIO_160		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_16		B	LPI GPIO 16	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_I2C_SCL		DO	LPI_QUP0 SE0, lane 1: I2C_SCL	
		LPI_I3C_SCL		DO	LPI_QUP0 SE0, lane 1: I3C_SCL	
		SYNC_OUT_GPIO_1		DO	Sync out GPIO_1	
G45	GPIO_161		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_17		B	LPI GPIO 17	
		LPI_I2C_SDA		B	LPI_QUP0 SE1, lane 0: I2C_SDA	
		LPI_I3C_SDA		B	LPI_QUP0 SE1, lane 0: I3C_SDA	
		SPI_CS_1		DO	LPI_QUP0 SE2, lane 4: SPI_CS_1	
		SYNC_OUT_GPIO_2		DO	Sync out GPIO_2	
H46	GPIO_162		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_18		B	LPI GPIO 18	
		LPI_I2C_SCL		DO	LPI_QUP0 SE1, lane 1: I2C_SCL	
		LPI_I3C_SCL		DO	LPI_QUP0 SE1, lane 1: I3C_SCL	
		SYNC_OUT_GPIO_3		DO	Sync out GPIO_3	
J47	GPIO_163		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_19		B	LPI GPIO 19	
		LPI_UART_CTS		DI	LPI_QUP0 SE2, lane 0: UART_CTS	
		LPI_I2C_SDA		B	LPI_QUP0 SE2, lane 0: I2C_SDA	
		LPI_SPI_MISO		DI	LPI_QUP0 SE2, lane 0: SPI_MISO	
		SYNC_OUT_GPIO_4		DO	Sync out GPIO_4	
J45	GPIO_164		PX_3	PD:nppukp	Configurable I/O	N
		LPI_GPIO_20		B	LPI GPIO 20	
		LPI_UART_RFR		DO	LPI_QUP0 SE2, lane 1: UART_RFR	
		LPI_I2C_SCL		DO	LPI_QUP0 SE2, lane 1: I2C_SCL	
		LPI_SPI_MOSI		DO	LPI_QUP0 SE2, lane 1: SPI_MOSI	
		SYNC_OUT_GPIO_5		DO	Sync out GPIO_5	
K46	GPIO_165		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_CTI_TRIG0_OUT_MIRB		DO	QDSS trigger output 0 B	
		LPI_GPIO_21		B	LPI GPIO 21	
		LPI_UART_TX		DO	LPI_QUP0 SE2, lane 2: UART_TX	

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Configurable function	Pad characteristics [a]		Functional description	Wake-up function
			Voltage	Type		
		LPI_SPI_SCLK		DO	LPI_QUP0 SE2, lane 2: SPI_SCLK	
		SYNC_OUT_GPIO_6		DO	Sync out GPIO_6	
L47	GPIO_166		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_CTI_TRIG1_OUT_MIRB		DO	QDSS trigger output 1 B	
		LPI_GPIO_22		B	LPI GPIO 22	
		LPI_UART_RX		DI	LPI_QUP0 SE2, lane 3: UART_RX	
		LPI_SPI_CS_0		DO	LPI_QUP0 SE2, lane 3: SPI_CS_0	
		SYNC_OUT_GPIO_7		DO	Sync out GPIO_7	
C45	GPIO_171		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCB[12]		DO	QDSS trace data bit 12 B	
		LPI_GPIO_23		B	LPI GPIO 23	
		LPI_I2C_SDA		B	LPI_QUP0 SE5, lane 0: I2C_SDA	
		LPI_UART_TX		DO	LPI_QUP0 SE5, lane 2: UART_TX	
		SYNC_OUT_GPIO_12		DO	Sync out GPIO_12	
D46	GPIO_172		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[13]		DO	QDSS trace data bit 13 B	
		LPI_GPIO_24		B	LPI GPIO 24	
		LPI_I2C_SCL		DO	LPI_QUP0 SE5, lane 1: I2C_SCL	
		LPI_UART_RX		DI	LPI_QUP0 SE5, lane 3: UART_RX	
		SYNC_OUT_GPIO_13		DO	Sync out GPIO_13	
E47	GPIO_173		PX_3	PD:nppukp	Configurable I/O	N
		QDSS_GPIO_TRACEDATA_LOCB[14]		DO	QDSS trace data bit 14 B	
		LPI_GPIO_25		B	LPI GPIO 25	
		LPI_UART_TX		DO	LPI_QUP0 SE6, lane 2: UART_TX	
		SYNC_OUT_GPIO_14		DO	Sync out GPIO_14	
E45	GPIO_174		PX_3	PD:nppukp	Configurable I/O	Y
		QDSS_GPIO_TRACEDATA_LOCB[15]		DO	QDSS trace data bit 15 B	
		LPI_GPIO_26		B	LPI GPIO 26	
		LPI_UART_RX		DI	LPI_QUP0 SE6, lane 3: UART_RX	
		SYNC_OUT_GPIO_15		DO	Sync out GPIO_15	

[a] For parameter and acronym definitions, see Table 2-1.
[b] GP_CLK GPIO function can be configured to output clock/PWM.
[c] LPI_GPIO_144 to LPI_GPIO_158 supports LPASS application (15 LPI GPIOs).
[d] LPI_GPIO_159 to LPI_GPIO_174 supports SSC application (12 LPI GPIOs).

Table 2-4 Pin descriptions – Do not connect (DNC), ground, and power-supply pins

Pad number	Pad name	Functional description
AG9, AE9, M30, BJ39, F4, BJ35, BM20, BP20, BP22, BM22, BL19, BN19, BK18, BM18, BN23, BR23, BN21, BL21, BP24, BM24, BL25, BN25	DNC	Do not connect. **NOTE** Pad internally connected, do not connect externally.
A1, A5, A7, A9, A21, A23, A25, A27, A39, A41, A43, A45, A47, AA25, AB4, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB28, AB30, AB32, AB34, AB36, AB38, AB40, AB42, AC11, AC13, AC15, AC17, AC19, AC21, AC25, AC29, AC31, AC33, AC35, AC37, AC39, AC47, AD4, AD6, AD10, AD28, AD40, AD42, AE25, AE47, AF10, AF12, AF14, AF16, AF18, AF20, AF22, AF28, AF30,AF32, AF34, AF36, AF38, AF40, AF42, AG1, AG25, AH2, AH4, AH6, AH10, AH12, AH18, AH28, AH42, AH44, AJ15, AJ25, AJ29, AJ31, AJ33, AJ35, AJ37, AJ39, AJ47, AK2, AK10, AK12, AK18, AK20, AK22, AK28, AK32, AK34, AK36, AK38, AK40, AK42, AL11, AL15, AL17, AL19, AL21, AL23, AL43, AM2, AM4, AM6, AM10, AM12, AM20, AM26, AM32, AM34, AM36, AM38, AM42, AN11, AN15, AN25, AN31, AN47, AP2, AP8, AP12, AP16, AP20, AP22, AP26, AP30, AP34, AP38, AP40, AP42, AP44, AP46, AR11, AR15, AR19, AR23, AR31, AR35, AR39, AT2, AT4, AT6, AT8, AT12, AT16, AT20, AT30, AT34, AT38, AU11, AU15, AU19, AU23, AU27, AU31, AU35, AU39, AU47, AV2, AV8, AV12, AV16, AV20, AV24, AV30, AV34, AV38, AW11, AW15, AW19, AW23, AW27, AW31, AW35, AW39, AY2, AY4, AY6, AY8, AY12, AY16, AY20, AY30, AY34, AY38, B4, B6, B8, B10, B38, B40, B42, B44, BA11, BA15, BA19, BA23, BA25, BA27, BA31, BA35, BA39, BA47, BB8, BB12, BB16, BB20, BB26, BB28, BB30, BC1, BC7, BC11, BC27, BC35, BC37, BD8, BD10, BD12, BD16, BD22, BD26, BD30, BD32, BD36, BD38, BD40, BE7, BE9, BE11, BE15, BE19, BE21, BE23, BE27, BE29, BE31, BE33, BE47, BF8, BF10, BF12, BF14, BF16, BF20, BF22, BF24, BF28, BF30, BF32, BF34, BF36, BF38, BF40, BG1, BG9, BG11, BG13, BG15, BG17, BG19, BG21, BG23, BG25, BG27, BG29, BG31, BG33, BG35, BG37, BG39, BG41, BH8, BH10, BH12, BH18, BH20, BH22, BH24, BH30, BH32, BJ17, BJ19, BJ21, BJ23, BJ29, BJ33, BJ47, BK10, BK20, BK22, BK24, BK26, BK28, BK36, BK38, BK40, BL1, BL17, BL23, BL27, BL29, BL35, BL39, BL41, BM10, BM14, BM16, BM26, BN11, BN13, BN17, BN31, BN35, BN41, BN47, BP18, BP26, BP32, BP34, BP44, BR1, BR3, BR7, BR19, BR21, BR25, BR33, BR37, BR41, BR47, C1, C11, C15, C17, C19, C21, C27, C29, C31, C33, C37, D4, D16, D32, D44, E5, E7, E9, E13, E17, E19, E21, E27, E29, E31, E35, E39, E41, E43, F10, F18, F22,	GND	Ground

Table 2-4 Pin descriptions – Do not connect (DNC), ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
F24, F38, F44, G5, G7, G13, G15, G23, G25, G27, G33, G35, G41, G43, H6, H8, H10, H12, H14, H16, H20, H22, H24, H26, H28, H32, H34, H36, H38, H40, H42, H44, J5, J9, J13, J15, J17, J19, J21, J23, J25, J27, J29, J31, J33, J35, J39, J43, K6, K12, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K34, K36, K42, K44, L7, L9, L11, L13, L15, L19, L21, L27, L31, L33, L35, L37, L39, L41, L43, M12, M14, M18, M20, M22, M26, M32, M34, M40, M44, N7, N23, N25, N37, P8, P34, P38, R1, R5, R7, R9, R11, R13, R15, R19, R21, R23, R25, R27, R31, R33, R37, R41, R47, T4, T10, T14, T16, T18, T20, T22, T28, T30, T32, T34, T38, U25, U37, U41, V6, V8, V10, V12, V14, V16, V18, V20, V24, V38, W3, W9, W11, W15, W17, W19, W21, W25, W29, W31, W33, W35, W37, W41, Y26, Y44		
Y36	VDD_A_APC_CS_1P8	Power for application processor current sensor; 1.8 V circuits
AL9	VDD_A_CSI_01_0P9	Power for CSI 0, 1: 0.9 V circuits
AM8	VDD_A_CSI_01_1P2	Power for CSI 0, 1: 1.2 V circuits
AJ9	VDD_A_CSI_23_0P9	Power for CSI 2, 3: 0.9 V circuits
AH8	VDD_A_CSI_23_1P2	Power for CSI 2, 3: 1.2 V circuits
AC9	VDD_A_CSI_4_0P9	Power for CSI 4: 0.9 V circuits
AD8	VDD_A_CSI_4_1P2	Power for CSI 4: 1.2 V circuits
BH38	VDD_A_CXO_1P8	Power for 1.8 V clock circuits
N15, N17, N19, N21	VDD_A_EBI0	Power for EBI PHY circuits
N27, N29, N31, N33	VDD_A_EBI1	Power for EBI PHY circuits
AM30	VDD_A_GFX_CS_1P8	Power for graphics current sensor circuits
L17	VDD_A_PLL_EBI0	Power for EBI0 PLL circuits
L29	VDD_A_PLL_EBI1	Power for EBI1 PLL circuits
W13	VDD_A_TURING_Q6_CS_1P8	Power for Q6 current sensor1.8 V circuits
W23, Y14, Y16, V26, V22, Y18, Y20, Y22, Y12, AA11, AA13, AA15, AA17, AA19, AA21, AA23, AC23, AD12, AD14, AD16, AD18, AD20, AD22, AD26, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE27, AF26, AG27, AG29, AH20, AH22, AH26, AJ17, AJ19, AJ21, AJ23, AJ27, AK26, AL27, AL29, AL31, AL33, AL35, AL37, AL39, AM18, AM22, AM28, AN21, AN23, AN27, AR25, AR27, AU25, AY26, M8, M10, N9, N11, N13, T6, T8, T12, T26, U5, U7, U9, U11, U13, U15, U17, U19, U21, U23, U27	VDD_CX	Power for digital core circuits
R17	VDD_D_EBI0	Power for EBI0 digital circuits
R29	VDD_D_EBI1	Power for EBI1 digital circuits
P14, P16, P18, P20	VDD_IO_EBI0	Power for EBI0 I/O circuits
P26, P28, P30, P32	VDD_IO_EBI1	Power for EBI1 I/O circuits

Table 2-4 Pin descriptions – Do not connect (DNC), ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
AA27, AB24, AC27, AD24, AF24, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AH16, AH24, AK16, AK24, AL25, AM16, AM24, AN29, AN33, AN35, AP24, AT24, AT26, AU9, AV26, AW9, BA9, BB32, BB34, BB36, BB38, P10, P12, V28, Y24, W27	VDD_MX	Power for on-chip memory
AE41	VDD_PX0	Power for pad group 0 – control signals
L25	VDD_PX1	Power for pad group 1
L23	VDD_PX10	Power for pad group 10 – UFS
BE35	VDD_PX11	Power for pad group 11 – CXO pad
AT40	VDD_PX2	Power for pad group 2 – SDC2 pads
AC41, AF8, AW25, BG7, BH40, P6	VDD_PX3	Power for pad group 3 – most I/O pads
BE37	VDD_PX5	Power for pad group 5 – UIM1 pads
BE39	VDD_PX6	Power for pad group 6 – UIM2 pads
M6	VDD_PX7	Power for pad group 7
AV40	VDDPX_VBIAS_SDC	Reference voltage for SDC
BH36	VDDPX_VBIAS_UIM	Reference voltage for UIM
M36, N35, P36, R35, T36, U29, U31, U33, U35, V30, V32, V34, V36	VDD_APC0	Power for the Kryo Silver application processor
Y40, Y32, Y34, Y38, Y30, Y28, Y42, W39, V40, U39, AA29, AA31, AA33, AA35, AA37, AA39, AA41, AA43, AD30, AD32, AD34, AD36, AD38, AE29, AE31, AE33, AE35, AE37, M38, M42, N39, N41, N43, P40, R39, T40	VDD_APC1	Power for the Kryo Gold application processor
AJ41	VDD_A_DSI_0_0P9	Power for the DSI0 0.9 V circuits
AG41	VDD_A_DSI_0_1P2	Power for the DSI0 1.2 V circuits
AH40	VDD_A_DSI_0_PLL_0P9	Power for the DSI0 0.9 V PLL circuits
AM40	VDD_VREF_0P9	Power for eDP 0.9 V circuits
AN41	VDD_VREF_1P2	Power for eDP 1.2 V circuits
BB24	VDD_A_GNSS_0P9	Power for 0.9 V GNSS circuits
Y8	VDD_A_PCIE_0_1P2	Power for the PCIe0 PLL
AA9	VDD_A_PCIE_0_CORE	Power for PCIe0 core circuits
BC31	VDD_A_PCIE_1_1P2	Power for the PCIe1 PLL
BC33	VDD_A_PCIE_1_CORE	Power for PCIe1 core circuits
BC15	VDD_A_QLINK_0_0P9	Power for the QLink0 0.9 V circuits
BD14	VDD_A_QLINK_0_0P9_CK	Power for the QLink0 0.9 V clock circuits
BC13	VDD_A_QLINK_0_1P2_CK	Power for the QLink0 1.2 V clock circuits
BD20	VDD_A_QLINK_1_0P9	Power for the QLink1 0.9 V circuits
BC21	VDD_A_QLINK_1_0P9_CK	Power for the QLink1 0.9 V clock circuits
BC19	VDD_A_QLINK_1_1P2	Power for the QLink1 1.2 V clock circuits

Table 2-4 Pin descriptions – Do not connect (DNC), ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
AL41, AN9, BD34, BE41, BC23, BE13, T42, T24, Y10	VDD_A_QREFS_0P875	Reference voltage for the QREFS 0.875 V circuits
BH34	VDD_A_QREFS_1P25	Reference voltage for the QREFS 1.25 V circuits
BJ37	VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits
P22	VDD_A_UFS_0_1P2	Power for the UFS 1.2 V circuits
P24	VDD_A_UFS_0_CORE	Power for the UFS core circuits
BE25	VDD_A_USBHS_1P8	Power for the USB high speed1.8 V circuits
BF26	VDD_A_USBHS_3P1	Power for the USB high speed3.1 V circuits
BD24	VDD_A_USBHS_CORE	Power for the USB HS core
BC29	VDD_A_USBSSDP_0_1P2	Power for USB SS and DisplayPort 1.2 V circuits
BD28	VDD_A_USBSSDP_0_CORE	Power for the USB SS and DisplayPort core circuits
AN37, AN39, AP28, AP32, AP36, AR29, AR33, AR37, AT28, AT32, AT36, AU29, AU33, AU37, AV28, AV32, AV36, AW29, AW33, AW37, AY28, AY32, AY36, AY40, BA29, BA33, BA37, BB40, BC39	VDD_GFX	Power for graphics
AK30	VDD_GFX_CX_ISENSE	Power for the GFX current sensor circuits
AE39, AG33, AG35, AG37, AG39, AH38	VDD_LPI_CX	Power for LPI digital core circuits
AG31, AH30, AH32, AH34, AH36	VDD_LPI_MX	Power for low-power island memory circuits
AH14, AJ11, AJ13, AK14, AL13, AM14, AN13, AN17, AN19, AP10, AP14, AP18, AR9, AR13, AR17, AR21, AT10, AT14, AT18, AT22, AU13, AU17, AU21, AV10, AV14, AV18, AV22, AW13, AW17, AW21, AY10, AY14, AY18, AY22, BA13, BA17, BA21, BB10, BB14, BB18, BB22, BC9, BC17, BD18, BE17, BF18	VDD_Modem	Power for modem circuits
BC25	VDD_LPI_NAV_MX	Power for LPI on chip memory– NAV
AY24	VDD_QFPROM	Power for programming the QFPROM
AB26	VDD_WPSS_CX	Power for WLAN digital core circuits

3 Electrical specifications

This topic defines the device electrical performance specifications, including absolute maximum ratings, operating conditions, and subsystem (such as memory and connectivity) parameters, which are useful in deploying the device with optimal processing capabilities and high efficiency.

3.1 Absolute maximum ratings

Do not exceed the absolute maximum ratings mentioned in Table 3-1.

WARNING: If ratings are exceeded, this may cause permanent damage to the device.

Functionality and reliability are guaranteed only within the conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
Power supply voltages				
VDD_APC0	Kryo Silver application processor	-0.3	1.0472	V
VDD_APC1	Kryo Gold application processor	-0.3	1.2485	V
VDD_MODEM	Modem circuits	-0.3	1.0472	V
VDD_GFX	Graphics processor	-0.3	1.1299	V
VDD_PX1	Pad group 1 - DDR pads	-0.3	1.287	V
VDD_PX2	Pad group 2 - SDC2 pads	-0.3	3.8984	V
VDD_PX5	Pad group 5 - UIM1 pads	-0.3	3.63	V
VDD_PX6	Pad group 6 - UIM2 pads	-0.3	3.63	V
VDD_PX10	Pad groups 10 - UFS pads	-0.3	1.4344	V
VDD_PX11	Pad groups 11 - CXO pads	-0.3	1.4344	V
VDD_MX	On-chip memory	-0.3	1.0472	V
VDD_LPI_CX	LPI core	-0.3	1.0428	V
VDD_A_USBSSDP_0_CORE	USB SS 0.9 V circuit	-0.3	1.0175	V
VDD_IO_EBIx	EBI I/O circuit	-0.3	0.715	V
VDD_A_QREFS_1P25	Reference voltage for QREFS 1.25 V circuit	-0.3	1.512	V
VDD_A_USBHS_3P1	USB HS 3.1 V circuit	-0.3	3.8984	V
VDD_A_CXO_1P8	1.8 V for clock circuits	-0.3	2.178	V
VDDPX_VBIAS_SDC	Bias voltage for SDC and UIM circuits	-0.3	1.512	V
VDDPX_VBIAS_UIM		-0.3	1.512	
VDD_PX0	Pad group 3 - control signal pads	-0.3	2.2	V
VDD_PX3	Pad group 3 - I/O pads			
VDD_PX7	Pad group 7 - SDC1 pads			
VDD_CX	Digital core circuits	-0.3	1.129	V
VDD_WPSS_CX	WPSS circuit			
VDD_D_EBIx	EBI digital circuits			
VDD_A_PCIE_0_1P2	PCIe circuit	-0.3	1.386	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter	Description	Min	Max	Unit
VDD_A_PCIE_1_1P2	PCIe circuit			
VDD_A_EDP_1P2	eDP circuits			
VDD_VREF_1P2	PCIe circuit QLink1 circuit			
VDD_A_CSI_x_1P2	CSI 1.2 V circuits			
VDD_A_UFS_0_1P2	UFS 1.2 V circuits			
VDD_A_USBSSDP_0_1P2	USB SS 1.2 V circuits			
VDD_A_QLINK_0_1P2_CK	QLink 0 clock circuit			
VDD_A_QLINK_1_1P2	QLink 1 clock circuit			
VDD_A_DSI_0_1P2	DSI 1.2 V circuit			
VDD_A_PCIE_0_CORE	PCIe circuit	-0.3	1.155	V
VDD_A_PCIE_1_CORE	PCIe circuit			
VDD_A_EDP_0P9	eDP circuits			
VDD_VREF_0P9	PCIe reference voltage			
VDD_A_CSI_x_0P9	CSIX 0.9 V circuits			
VDD_A_QLINK_x_0P9	QLink 0.9 V circuits			
VDD_A_QLINK_x_0P9_CK	QLink clock circuits			
VDD_A_UFS_0_CORE	UFS 0.9 V circuits			
VDD_A_USBHS_CORE	USB HS 0.9 V circuits			
VDD_A_GNSS_0P9	GNSS circuits			
VDD_A_DSI_0_0P9	DSI 0.9 V circuits			
VDD_A_DSI_0_PLL_0P9	DSI PLL 0.9 V circuits			
VDD_A_QREFS_0P875	Reference voltage for QREFS 0.875 V circuit			
VDD_A_EBIx	EBI PHY voltage circuits	-0.3	1.115	V
VDD_A_PLL_EBIx	EBI PLL circuit			
VDD_A_USBHS_1P8	USB HS 1.8 V circuits	-0.3	2.178	V
VDD_QFPROM	Programming the QFPROM			
VDD_A_GFX_CS_1P8	GFX 1.8 V circuits			
VDD_A_TURNING_Q6_CS_1P8	Power for Q6 current sensor 1.8 V circuits			
VDD_A_QREFS_1P8	Reference voltage for the QREFS 1.8 V circuits			
VDD_A_APC_CS_1P8	Power for application processor current sensor; 1.8 V circuits			
VDD_LPI_NAV_MX	LPI on chip memory – NAV	-0.3	1.0043	V
VDD_LPI_MX	Low-power island memory circuits			
T_s	Storage temperature [a], [b]	-55	150	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~+35°C] and < 90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include parameters such as power supply voltage, power distribution impedances, and thermal conditions. The QCS6490 and QCS5430 chipsets meet all performance specifications listed in the following table when used within the operating conditions.

NOTE Keep the thermal mitigation algorithm enabled with default limits to ensure that the operating temperature range is kept within the specification.

Table 3-2 Operating conditions

Parameter			Min	Type [a]	Max	Unit
Power supply voltages						
VDD_APC0 [b]	–	Kryo Silver application processor	0.47	–	0.952	V
VDD_APC1 [b]	–	Kryo Gold application processor	0.484	–	1.135	V
VDD_MODEM	–	Modem circuits	0.47	–	0.952	V
VDD_GFX [b]	–	Graphics processor	0.47	–	1.027	V
VDD_PX1 (LPDDR5)	–	Pad group 1 - DDR pads	1.01	1.05	1.12	V
VDD_PX1 (LPDDR4X)	–	Pad group 1 - DDR pads	1.06	1.1	1.17	V
VDD_PX2	Low voltage	Pad group 2 - SDC2 pads	1.65	1.8	1.9	V
	High voltage		2.72	2.95	3.544	
VDD_PX5 [c]	Low voltage	Pad group 5 - UIM1 pads	1.62	1.8	1.9	V
	High voltage		2.85	2.96	3.3	
VDD_PX6	Low voltage	Pad group 6 - UIM2 pads	1.62	1.8	1.9	V
	High voltage		2.85	2.96	3.3	
VDD_PX10	–	Pad groups 10-UFS pads	1.1	1.2	1.304	V
VDD_PX11	–	Pad groups 11-CXO pads	1.1	1.2	1.304	V
VDD_MX [b]	Active	On-chip memory	0.695	–	0.952	V
VDD_MX [b]	Retention	On-chip memory	0.512	–	0.668	V
VDD_LPI_CX	–	LPI core	0.47	–	0.948	V
VDD_A_USBSSDP_0_CORE	–	USB SS 0.9 V circuit	0.825	0.875	0.925	V
VDD_IO_EBIx (LPDDR5)	> 1.5 GHz	EBI I/O circuit	0.47	0.5	0.57	V
VDD_IO_EBIx (LPDDR5)	< 1.5 GHz	EBI I/O circuit	0.27	0.3	0.37	V
VDD_IO_EBIx (LPDDR4X)	–	EBI I/O circuit	0.57	0.6	0.65	V
VDD_A_QREFS_1P25	–	Reference voltage for QREFS 1.25 V circuit	1.125	1.25	1.375	V
VDD_A_USBHS_3P1 [d]	–	USB HS 3.1 V circuit	2.7	3.072	3.544	V
VDD_A_CXO_1P8	–	1.8 V for clock circuits	1.68	1.8	1.98	V
VDDPX_VBIAS_SDC	–	Bias voltage for SDC and UIM circuits	1.125	1.25	1.375	V
VDDPX_VBIAS_UIM	–					
VDD_PX0	–	Pad group 3 - control signal pads	1.68	1.8	2	V
VDD_PX3	–	Pad group 3 - I/O pads				
VDD_PX7	–	Pad group 7- SDC1 pads				

Table 3-2 Operating conditions (cont.)

Parameter			Min	Type [a]	Max	Unit
VDD_CX	Active	Digital core circuits	0.47	–	1.027	V
VDD_CX	Retention	Digital core circuits	0.352		0.48	
VDD_WPSS_CX	–	WPSS circuit	0.47		1.027	
VDD_D_EBIx	–	EBI digital circuits	0.47		1.027	
VDD_A_PCIE_0_1P2	–	PCIe circuit	1.11	1.2	1.26	V
VDD_VREF_1P2	–	PCIe circuit QLink1 circuit				
VDD_A_CSI_x_1P2	–	CSI 1.2 V circuits				
VDD_A_UFS_0_1P2	–	UFS 1.2 V circuits				
VDD_A_USBSSDP_0_1P2	–	USB SS 1.2 V circuits				
VDD_A_QLINK_0_1P2_CK	–	QLink0 clock circuit				
VDD_A_QLINK_1_1P2	–	QLink1 clock circuit				
VDD_A_DSI_0_1P2	–	DSI 1.2 V circuit				
VDD_A_PCIE_0_CORE	–	PCIe circuit	0.86	0.875	1.05	V
VDD_VREF_0P9	–	PCIe reference voltage				
VDD_A_CSI_x_0P9	–	CSIX 0.9 V circuits				
VDD_A_QLINK_x_0P9	–	QLink 0.9 V circuits				
VDD_A_QLINK_x_0P9_CK	–	QLink clock circuits				
VDD_A_UFS_0_CORE	–	UFS 0.9 V circuits				
VDD_A_USBHS_CORE	–	USB HS 0.9 V circuits				
VDD_A_GNSS_0P9	–	GNSS circuits				
VDD_A_DSI_0_0P9	–	DSI 0.9 V circuits				
VDD_A_DSI_0_PLL_0P9	–	DSI PLL 0.9 V circuits				
VDD_A_QREFS_0P875	–	Reference voltage for QREFS 0.875 V circuit				
VDD_A_EBIx	–	EBI PHY voltage circuits	0.64	–	1.014	V
VDD_A_PLL_EBIx	–	EBI PLL circuit				
VDD_A_USBHS_1P8	–	USB HS 1.8 V circuits	1.68	1.8	1.98	V
VDD_QFPROM	–	Programming the QFPROM				
VDD_A_GFX_CS_1P8	–	GFX 1.8 V circuits				
VDD_A_TURNING_Q6_CS_1P8	–	Power for Q6 current sensor 1.8 V circuits				
VDD_A_QREFS_1P8	–	Reference voltage for the QREFS 1.8 V circuits				
VDD_A_APC_CS_1P8	–	Power for application processor current sensor; 1.8 V circuits				
VDD_LPI_NAV_MX	–	LPI on chip memory – NAV	0.695	–	0.913	V
VDD_LPI_MX	–	Low-power island memory circuits				
Thermal conditions						

Table 3-2 Operating conditions (cont.)

Parameter			Min	Type [a]	Max	Unit
T	–	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = 95	°C
T [e]	–	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = 105	°C

[a] Typical voltages represent the recommended output settings of the companion PMIC device.
[b] All voltage rails are optimized and dynamically controlled by software based on system requirements and margins. During boot-up stage, some power rails, for example, VDD_GFX, VDD_APC, VDD_MX might margin close to operation but within absolution maximum. Internal validation has been performed under these conditions.
[c] Universal Identity Module (UIM) is not supported on the QCS6490 and QCS5430 chipsets. For more information on supported pins, see *QCM6490/QCS6490+ PM7325 + PM7350C + PM7250B-2 Reference Schematic* (80-20659-44) and *QCS6490/QCS5430 Technical Reference Manual* (80-20659-5).
[d] Software configures L2B VDD_A_USBHS_3P1 to vote 2.704 V. At boot/power-on L7B starts at 2.952 V. Once UFS is enumerated at XBL, software changes this voltage to 2.5 V (for UFS3.1).
[e] This thermal condition is applicable only for the 300-AA variant of QCS6490 and QCS5430.

NOTE Unless otherwise specified, the specifications apply across the device's operating temperature range.

3.3 Power delivery network specification

For power delivery network specification, see *QCS6490/QCS5430 Chipset Power Delivery Network Specification* (80-20659-1P).

3.4 Average operating current

For current consumption information and details on operating modes tested, see *QCM6490/QCS6490 Linux Android Current Consumption Data Application Note* (80-20659-7).

3.5 Dhrystone maximum power

The Dhrystone maximum power (tested at 1× Kryo Prime at 2.4 GHz, 3 × Kryo Gold at 2.4 GHz, and 4 × Kryo Silver at 1.8 GHz) at 95°C (Tj) is 6.9 W. QTI recommends measuring the Dhrystone power on the VDD_APC1 rail, right before PDN capacitors with a small serial sampling resistor inserted, if necessary. The measurement sampling rate is > 1.25 Msps (or < 0.8 µs), and the average window is > 1 ms (or > 1250 samples).

NOTE The Dhrystone specification applies to QCS6490 and QCS5430 commercial sample (CS) devices only.

3.6 Power sequencing

The PMIC includes power-on circuits that provide the correct power sequencing for the QCS6490 and QCS5430 chipsets. The supplies are turned on as groups of regulators controlled by the hardware configuration of certain PMIC pins. For more information, see *PM7325 Data Sheet* (80-19730-1) and *PM7350C Data Sheet* (80-PW237-1).

A high-level summary of the required default power-on sequence is as follows:

Sequence	Power domain
1	VDD_PX5 (UICC1), VDD_PX6 (UICC2),
2	VDD_MX (on-chip memory)
3	VDD_LPI_MX (LPI core memory), VDD_NAV_LPI_MX
4	VDD_A_EBI_0P9 (EBI 0.9 V), VDD_A_PLL_EBI_0P9
5	VDD_CX (digital core), VDD_D_EBI, VDD_WPSS_CX (WPSS core supply)

Sequence	Power domain
6	VDD_LPI_CX (LPI core)
7	VDD_PX0 (pad group0), VDD_PX3 (peripheral), VDD_PX7 (eMMC pads)
8	VDD_PX1 (pad group1)
9	VDD_A_DSI_1P2 (DSI 1.2 V), VDD_A_PCIe_0_PLL_1P2, VDD_A_USB_SS_DP_1P2, VDD_A_UFS_0_1P, VDD_A_QLINK_1P2_CK (QLINK 1.2 V), VDD_A_CSI_X_1P2 (CSI 1.2 V)
10	VDD_A_QREFS_1P25 (reference voltage for the QREFS 1.25 V circuit), VDDPX_VBIAS_SDC (reference voltage for SDC), VDDPX_VBIAS_UIM (reference voltage for UIM)
11	VDD_A_DSI_PLL_0P9 (DSI 0.9 V PLL), VDD_A_UFS_0_CORE (UFS), VDD_A_CSI_X_0P9 (CSI 0.9 V), VDD_A_DSI_0P9 (DSI 0.9 V), VDD_USBHS_CORE (USB HS), VDD_A_QREFS_0P875 (reference voltage for the QREFS 0.875 V), VDD_A_QLINK0_0P9 (QLink0), VDD_A_QLINK1_0P9 (QLink1), VDD_A_GNSS_0P9, VDD_A_PCIe0_CORE, VDD_A_QLINK0_CK_0P9 (QLink0 clock), VDD_A_QLINK1_CK_0P9 (QLink1 clock),
12	VDD_A_USB_SS_DP_CORE (USB Core)
13	VDD_PX11 (CXO pad group)
14	VDD_A_QREFS_VREF_1P8, VDD_A_APC_CS_1P8, VDD_A_USB_HS_1P8, VDD_A_GFX_CS_1P8, VDD_A_QFPROM, VDD_A_TURNING_CS_1P8, VDD_A_CXO_1P8
15	VDD_IO_EBI (EBI I/O supply)
16	VDD_A_USB_HS_3P1 (USB HS 3.1 V)
17	VDD_PX10 (UFS reference clock, UFS reset)
18	VDD_PX2 (SDC2 pads)
19	VDD_APC0 (Silver application processor)

This sequence includes:

- After completing the sequence, the software can power-on other appropriate power supply.
- Before the next domain starts increasing, each domain must achieve its 90% value.

3.7 Digital-logic characteristics

The digital I/O performance specification depends on pad type, usage, supply voltage, or a combination of pad type, usage, and supply voltage.

- Some of the I/Os are dedicated for interconnections between the SoC device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some of the I/Os conform to existing standards, such as I²C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

NOTE Unless otherwise specified, all device characterizations are carried out across the specified operating temperature and voltage ranges.

Table 3-3 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDD_PX3	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PX3	VDD_PX3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDD_PX3	V

Table 3-3 DC specification of 1.8 V GPIOs and WCSS WSI I/Os (cont.)

Parameter	Description	Min	Max	Unit
V_{HYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	100	—	mV
V_{HYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	—	mV
I_{IH}	Input high leakage current	—	1.0	µA
I_{IL}	Input low leakage current	-1.0	—	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
V_{OH}	High-level output voltage, CMOS [a]	VDD_PX3 - 0.45	VDD_PX3	V
V_{OL}	Low-level output voltage, CMOS [a]	0.0	0.45	V

[a] VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures. For more information regarding possible drive strength settings, see Table 3-4

Table 3-4 Possible drive strength

BIT configuration	Drive strength (mA)
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Table 3-5 SDC 3 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	0.625 × VDD_PX2	–	VDD_PX2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDD_PX2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [a]	0.75 × VDD_PX2	–	VDD_PX2	V
V_{OL}	Low-level output voltage [a]	0.0	–	0.125 × VDD_PX2	V

[a] VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures. For more information regarding possible drive strength settings, see Table 3-6

Table 3-6 Possible drive strength

BIT configuration	Drive strength (mA)
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Table 3-7 SDC 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [a]	1.4	–	–	V
V_{OL}	Low-level output voltage [a]	–	–	0.45	V

[a] VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures. For more information regarding possible drive strength settings, see Table 3-8

Table 3-8 Possible drive strength

BIT configuration	Drive strength (mA)
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Table 3-9 UICC 3 V mode DC specifications for (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
VDDPX	Supply voltage	2.7	2.95	3.05	V
V_{IH}	High-level input voltage [a]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage [b]	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [c]	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage [d]	0.0	–	0.4	V

[a] V_{IH} and V_{IL} are only applicable for the I/O signal. V_{HYS} is not a required specification for UICC.
[b] V_{HYS} is not a required specification for UICC.
[c] UICC specifies V_{OH} = 0.8 × VDDPX (RST) and 0.7 × VDDPX (clock, I/O). The worse-case V_{OH} is used in this table. VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures.
[d] UICC specifies V_{OL} = 0.2 × VDDPX (RST, clock) and 0.4 V (I/O). The worse-case V_{OL} is used in this table. VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures. For more information regarding possible drive strength settings, see Table 3-10

Table 3-10 Possible drive strength

BIT configuration	Drive strength (mA)
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Table 3-11 UICC 1.8 V mode DC specifications for (VDD_PX5 and VDD_PX6)

Parameter	Description	Min	Typ	Max	Unit
VDDPX	Supply voltage [a]	1.65	1.8	1.95	V
V_{IH}	High-level input voltage [b]	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ

Table 3-11 UICC 1.8 V mode DC specifications for (VDD_PX5 and VDD_PX6) (cont.)

Parameter	Description	Min	Typ	Max	Unit
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage [c]	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage [c]	0.0	–	0.4	V

[a] The UICC supply range for class C is 1.62 V 1.98 V.
[b] V_{IH}, V_{IL}, are only applicable for I/O signal. V_{HYS} is not a required specification for UICC.
[c] VOL and VOH are measured at IOL and IOH respectively, with 16 mA current across min and max voltages and operating temperatures. For more information regarding possible drive strength settings, see Table 3-12

Table 3-12 Possible drive strength

BIT configuration	Drive strength (mA)
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Table 3-13 Digital I/O characteristics for VDD_PX10 nominal (UFS)

Parameter	Description	Min	Max	Unit
V_{OL}	Output low-level voltage	0	0.25 × VDD_PX10	V
V_{OH}	Output high-level voltage	0.75 × VDD_PX10	VDD_PX10	V
$R_{PULL-UP}$	Pull-up resistance	20	–	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	–	kΩ

3.8 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE QCS6490 and QCS5430 devices are characterized with actively terminated loads, so all baseband timing parameters assume no bus loading. For more information, see Rise and fall time specifications.

3.8.1 Timing diagram conventions

The following figure shows the conventions used within timing diagrams throughout this document.

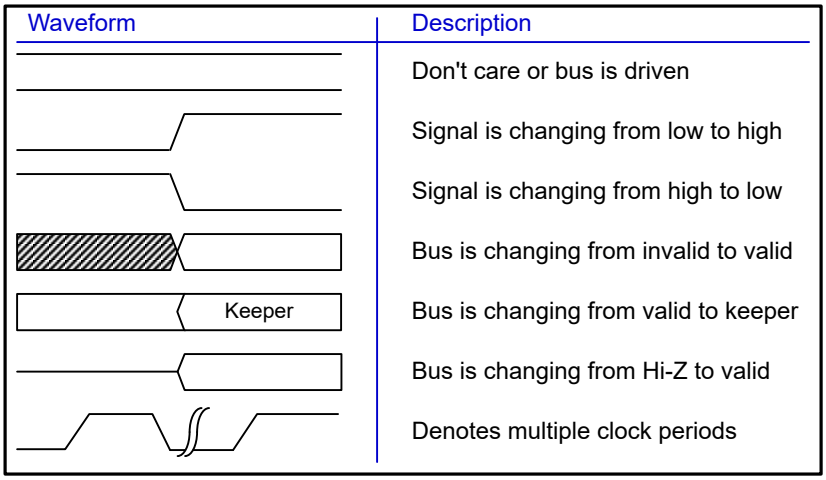


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, it indicates *don't care*.

3.8.2 Rise and fall time specifications

QCS6490 and QCS5430 chipsets characterization testing uses actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact of different external load conditions on rise and fall times is shown in the following figure.

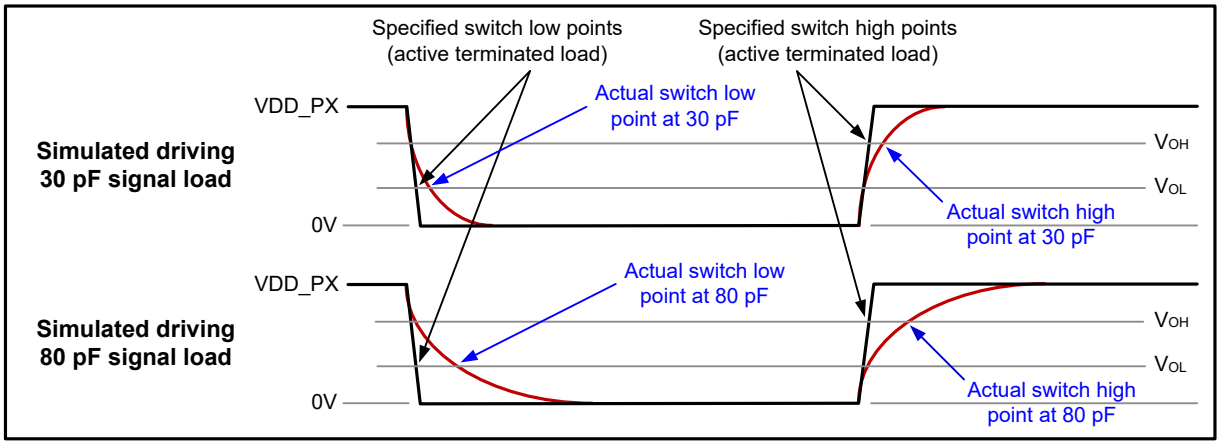


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, add the rise or fall times to the parameters that start timing at the QCS6490 and QCS5430 chipsets and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.8.3 Pad design methodology

The QCS6490 and QCS5430 chipsets use a generic CMOS pad driver design. The pad design creates a pin response and behavior that is symmetric, regarding the associated $V_{DD\_PXDD\_PX}$/2% or 50% of Vsupply. The input switchpoint for pure input-only pads is a V_{DD_PX} supply. The documented switchpoints (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_{IL} and 65% of V_{DD_PX} for V_{IH}.

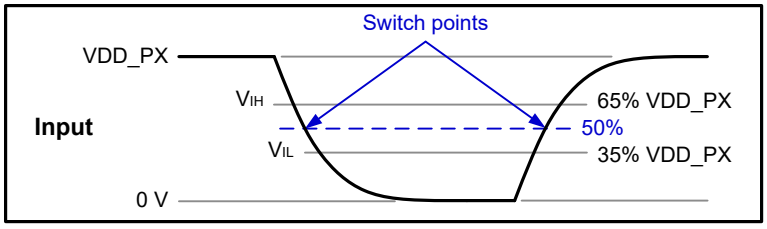


Figure 3-3 Digital input-signal switchpoints

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented VOH (min) and VOL(max) levels over worst-case process/voltage/

temperature. The pad output structures are essentially CMOS drivers. They may have a small amount of IR loss (estimated at <50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- V_{OH}~ V_{DDPX}- 50 mV or more
- V_{OL}~ 50 mV or less

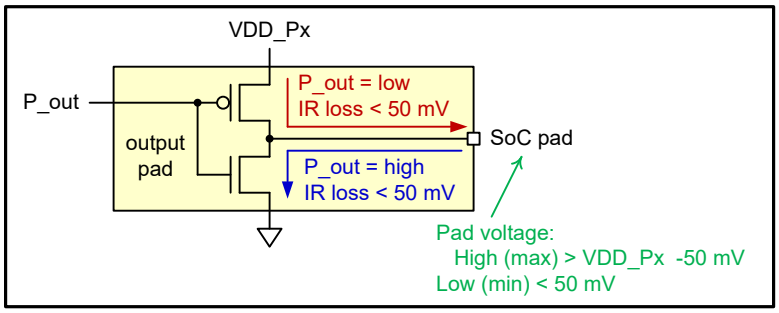


Figure 3-4 Output pad equivalent circuit

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DDPX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) provides approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) provides approximately 1.25 mA or more at ½ × [V_{DDPX} - 50 mV + V_{OH} (min)].

The target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

3.9 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must factor into the numbers in this document. For example, setup time numbers get worse, and hold time numbers may improve.

3.9.1 EBI0 and EBI1 memory support

The EBI0 and EBI1 ports are dedicated to the non-PoP LPDDR4X/LPDDR5 SDRAM memory that is attached to the QCS6490 and QCS5430 chipsets.

3.9.1.1 eMMC on SDC1

eMMC NAND flash supports the SDC1 port. For more information, see Secured digital interfaces.

3.10 Multimedia

This topic addresses the performance specification of multimedia parameters.

3.10.1 Camera interfaces

The QCS6490 and QCS5430 chipsets support five 4-lane MIPI-CSI: CSI0, CSI1, CSI2, CSI3, and CSI4.

Table 3-14 Supported MIPI-CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for D-PHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for C-PHY v1.0	None

3.10.2 Audio support

A dedicated audio codec, such as the WCD9370/WCD9375/WCD9380/WCD9385, uses the industry standard SoundWire interface.

Other audio-related interface options include:

- Digital microphone: Section 3.11.6 *Digital microphone PDM interface*
- SWR: Section 3.11.7 *SoundWire (SWR) interface*
- SLIMbus: Section 3.11.8 *SLIMbus interface*
- I²S: Section 3.11.9 *I²S interfaces*
- I²C/I3C: Section 3.11.11 *I²C/I3C interface*
- SPI: Section 3.11.12 *Serial peripheral interface*

For more information on performance characteristics, see *Qualcomm Aqstic™ WCD9370 Device Specification* (80-PG244-1), *Qualcomm Aqstic WCD9375 Device Specification* (80-PG245-1), and *Qualcomm Aqstic WCD9380/WCD9385 Device Specification* (80-PL335-1).

3.10.3 Display support

The QCS6490 and QCS5430 chipsets support one D-PHY display.

Table 3-15 Supported MIPI-DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.0	None

3.10.4 Digital media broadcast (DMB) support

The QCS6490 and QCS5430 chipsets support an external DMB solution using the following interface options:

- SPI: Section 3.11.12 *Serial peripheral interface*
- SD: Section 3.11.1 *Secured digital interfaces*

3.11 Connectivity

The connectivity functions that require electrical specifications for this chipset are as follows:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Universal integrated circuit card (UICC) interface
- DisplayPort support over USB Type-C
- Serial low-power interchip media bus (SLIMbus) interface for Bluetooth, FM
- Inter-IC sound (I²S) interfaces
- Touchscreen connections
- Dedicated I²C interfaces for camera (CCI I²C)
- Through proper configuration of QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I²C) interfaces
  - Serial peripheral interface (SPI) ports

The pertinent specifications for these functions are detailed in the following topics.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

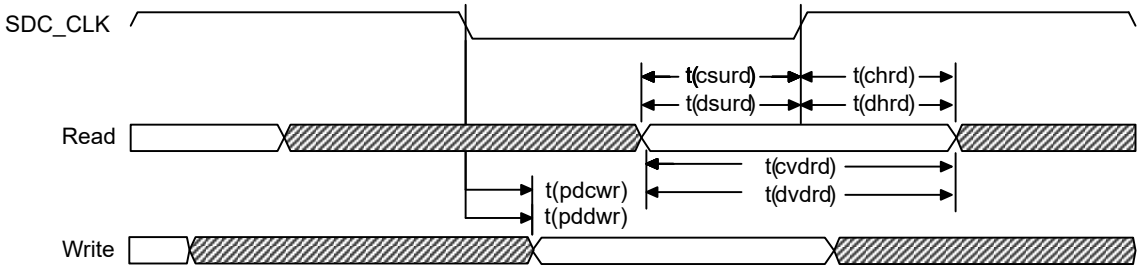
3.11.1 Secured digital interfaces

The supported secure digital (SD) interface standards and their exceptions are listed here.

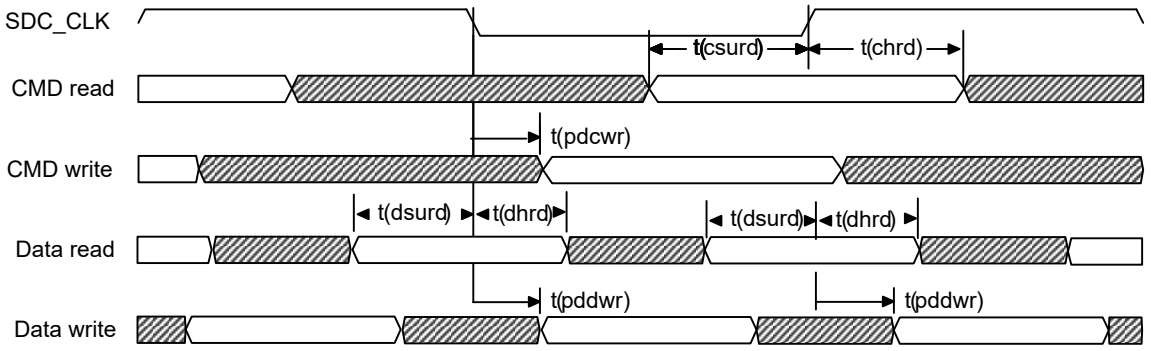
Table 3-16 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

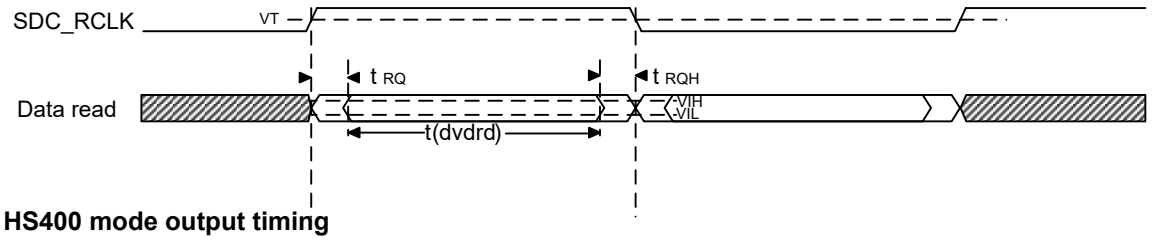
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

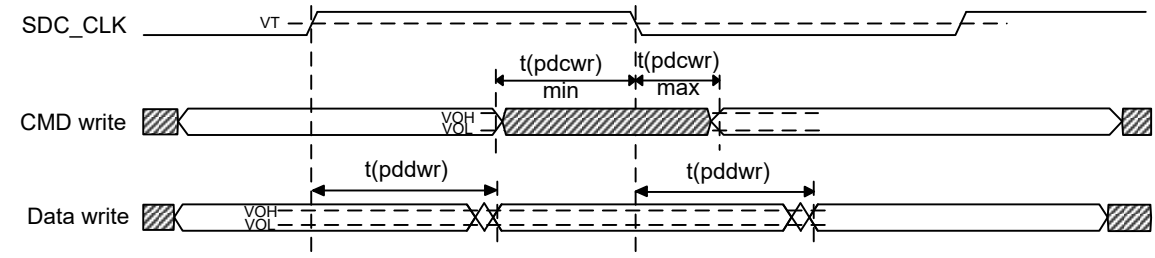


Figure 3-5 Secured digital interface timing

Table 3-17 SDCC timing specification with respect to controller – regular mode

SDCC modes	Frequency	Parameter	Description	Min (ns)	Max (ns)
HS400 (DDR 200 MHz) [a]	200 MHz	TclkH	Clock high time	2.25	2.75
		Tcidv	Command input valid window	N/A	2.4

Table 3-17 SDCC timing specification with respect to controller – regular mode (cont.)

SDCC modes	Frequency	Parameter	Description	Min (ns)	Max (ns)
		Tcodly	Command output delay	-1.45	0.85
		tRQ	DQS to DQ valid setup	0.4	N/A
		tRQH	DQS to DQ valid hold	N/A	-0.4
		Tdodly	Data output delay	0.4	1.85
HS200(SDR 200 MHz)	200 MHz	TclkH	Clock high time	2.25	2.75
		Tcidv	Command input valid window	N/A	2.4
		Tcodly	Command output delay	-1.45	0.85
		Tidv	Data input valid window	N/A	2.4
		Tdodly	Data output delay	-1.45	0.85
DDR52	52 MHz	TclkH	Clock high time	8.65	10.57
		Tcisu	Command input setup	N/A	5.53
		Tcih	Command input hold	N/A	1.50
		Tcodly	Command output delay	-7.85	2.65
		Tisu	Data input setup	N/A	1.65
		Tih	Data input hold	N/A	1.50
		Tdodly	Data output delay	2.50	6.15
SDR 104	202 MHz	TclkH	Clock high time	1.5	3.5
		Tcidv	Command input valid window	N/A	2.4
		Tcodly	Command output delay	-1.45	0.85
		Tidv	Data input valid window	N/A	2.4
		Tdodly	Data output delay	-1.45	0.85
DDR 50	50 MHz	TclkH	Clock high time	9	11
		Tcisu	Command input setup	N/A	6.3
		Tcih	Command input hold	N/A	1.5
		Tcodly	Command output delay	-8.2	3
		Tisu	Data input setup	N/A	2
		Tih	Data input hold	N/A	1.5
		Tdodly	Data output delay	0.8	6
SDR 50	100 MHz	TclkH	Clock high time	3	7
		Tcisu	Command input setup	N/A	2.5
		Tcih	Command input hold	N/A	1.5
		Tcodly	Command output delay	-3.7	1.5
		Tisu	Data input setup	N/A	2.5
		Tih	Data input hold	N/A	1.5
		Tdodly	Data output delay	-3.7	1.5
SDR 25	50 MHz	TclkH	Clock high time	9	11
		Tcisu	Command input setup	N/A	6
		Tcih	Command input hold	N/A	1.5
		Tcodly	Command output delay	-7	3

Table 3-17 SDCC timing specification with respect to controller – regular mode (cont.)

SDCC modes	Frequency	Parameter	Description	Min (ns)	Max (ns)
		Tisu	Data input setup	N/A	6
		Tih	Data input hold	N/A	2.5
		Tdodly	Data output delay	-7	3

[a] For DDR200, DDR52 and SD DDR50, command input/output is only in single data rate (with respect to controller CLK falling edge). Only data input/ output is running at DDR.

3.11.2 USB interfaces

The supported USB standards and their exceptions are listed here.

Table 3-18 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 1
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.11.3 DisplayPort

The supported DisplayPort standards and their exceptions are listed here.

Table 3-19 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.11.4 PCIe interface

The supported PCIe standards and their exceptions are listed here.

Table 3-20 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Base Specification Revision 3.0	Link configure capability

3.11.5 UFS interface

The supported UFS standards and their exceptions are listed here.

Table 3-21 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	None
Universal Flash Storage (UFS), Version 2.1	None

3.11.6 Digital microphone PDM interface

The following figure shows the digital microphone PDM interface timing.

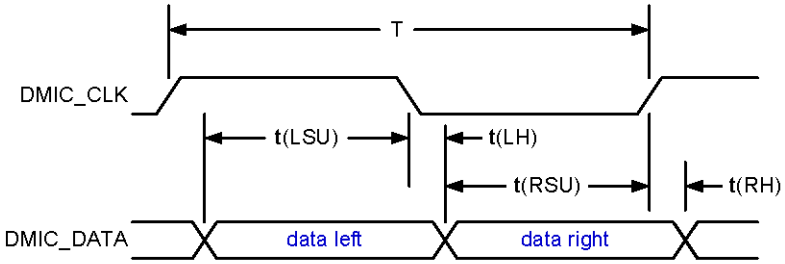


Figure 3-6 Digital microphone PDM interface timing

The supported Digital microphone timings are listed here.

Table 3-22 Digital microphone timing

Parameter		Min	Typ	Max	Unit
1/T	DMIC clock frequency	0.6	–	6.144	ns
	DMIC clock duty cycle	45	–	55	–
t(LSU)	Data left setup time to clock falling edge	–	–	–	ns
t(LH)	Data left hold time to clock falling edge	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	10	–	–	ns
t(RH)	Data right hold time to clock rising edge	0	–	–	–

3.11.7 SoundWire (SWR) interface

The QCS6490 and QCS5430 chipsets SoundWire PHY timing parameters comply with clock and data specifications, as specified in the *MIPI Alliance Specification for SoundWire Version 0.8, Revision 04.*

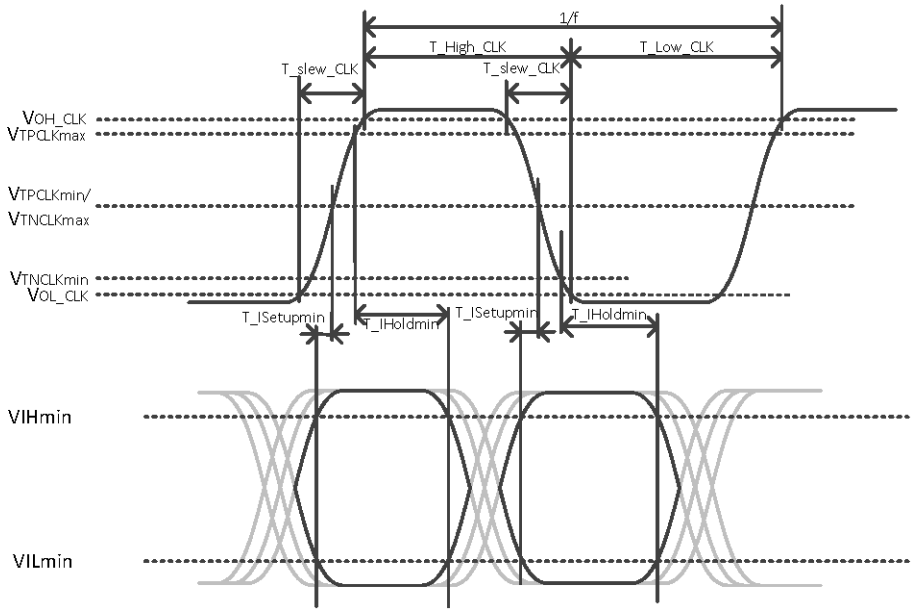


Figure 3-7 PHY timing – clock output/input and data input

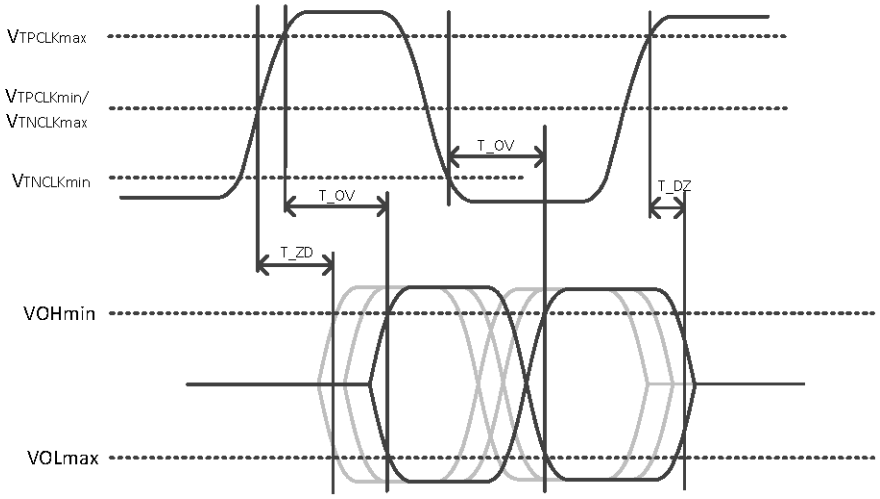


Figure 3-8 PHY timing – clock output and data output

The supported PHY timing parameters for 1.8 V systems are listed here.

Table 3-23 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Unit
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	MHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of Low half-period on Clock output signal in small systems	35.3	–	ns

Table 3-23 PHY timing parameters (1.8 V systems) (cont.)

Name	Description	Min	Max	Unit
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	ns
t_OH_Data_1V8	Time for the data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	4	–	ns
t_IHold_min_Data_1V8	Input hold time	–	5	ns
DC_Out_Clock	Duty cycle generated at clock output signal. Calculated from t_Low_Clock/(t_Low_Clock + t_High_Clock)	46% of the SWR clock	54% of the SWR clock	ns

3.11.8 SLIMbus interface

The supported SLIMbus standards and their exceptions are listed here.

Table 3-24 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.11.9 I²S interfaces

There are two supported I²S interface types:

- Legacy I²S interfaces for primary and secondary microphones and speakers
- The multiple I²S (MI2S) interface for microphone and speaker functions

The following information applies to both interface types. The supported I²S standards and their exceptions are listed here.

Table 3-25 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

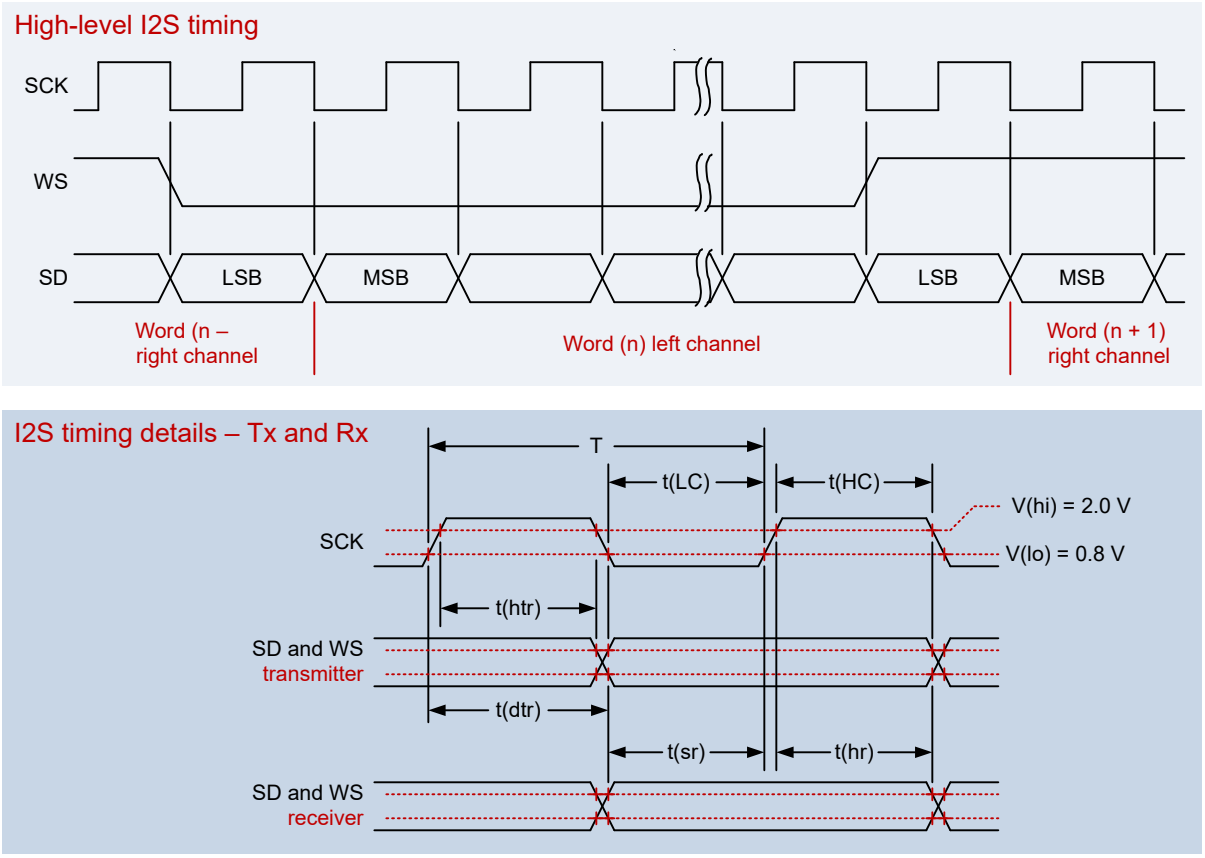


Figure 3-9 I²S timing diagram

The supported I²S interface timings are listed here.

Table 3-26 I²S interface timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency [a]		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	1.5	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.1	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.40 × T	–	0.60 × T	ns
t(LC)	Clock low	–	0.40 × T	–	0.60 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns

Table 3-26 I²S interface timing (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(hr)	SD and WS input hold time	–	1.5	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.1	ns

[a] Load capacitance is between 10 pF and 40 pF.

3.11.10 Touchscreen connections

Touchscreen panels are supported using I²C buses (I²C/I3C interface) and GPIOs configured as discrete digital inputs (Digital-logic characteristics). Additional specifications are not required.

3.11.11 I²C/I3C interface

The supported I²C standards and their exceptions are listed here.

Table 3-27 Supported I²C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C Specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.11.12 Serial peripheral interface

The QCS6490 and QCS5430 chipsets support SPI as a master only.

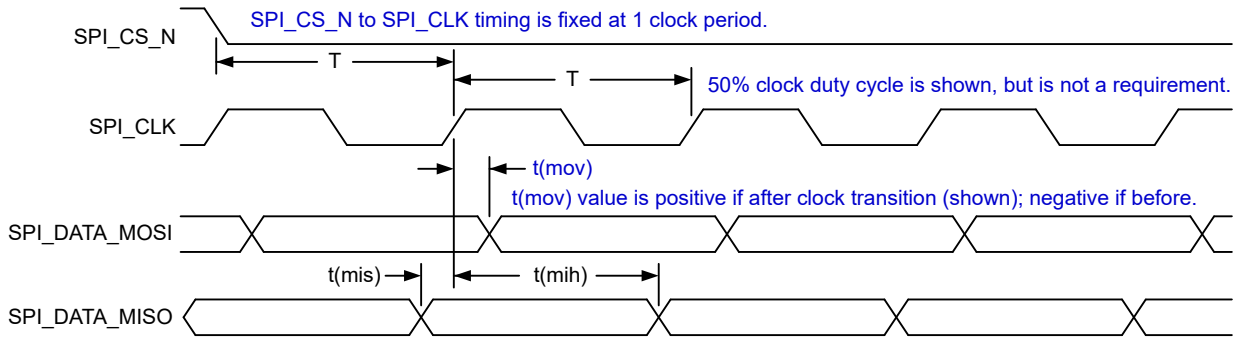


Figure 3-10 SPI master timing diagram

The supported SPI master timing characteristics are listed here.

Table 3-28 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns

Table 3-28 SPI master timing characteristics (cont.)

Parameter	Comments	Min	Typ	Max	Unit
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

3.12 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.12.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding topics of this document. Others are specified here.

3.12.1.1 19.2 MHz CXO input

The following figure shows the XO timing parameters.

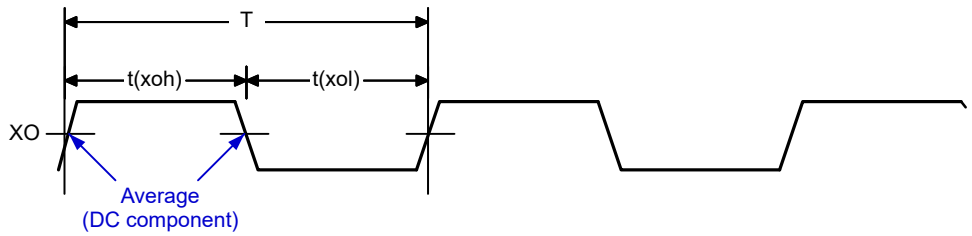


Figure 3-11 XO timing parameters

The supported XO timing parameters are listed here.

Table 3-29 XO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	–	–	ns
1/T	Frequency	19.2 MHz must be used.	–	–	–	MHz

[a] For more information, see the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* (80-V9690-24).

3.12.1.2 Sleep clock

The following figure shows the sleep-clock timing parameters.

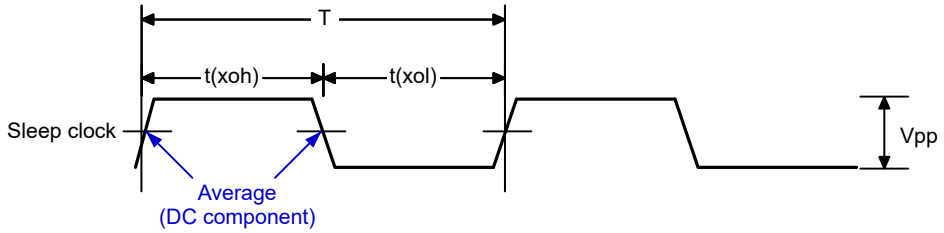


Figure 3-12 Sleep-clock timing parameters

The supported sleep-clock timing parameters are listed here.

Table 3-30 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs
F	Sleep-clock frequency	F= 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.12.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications in Digital-logic characteristics.

3.12.3 JTAG

The following figure shows the JTAG interface timing diagram.

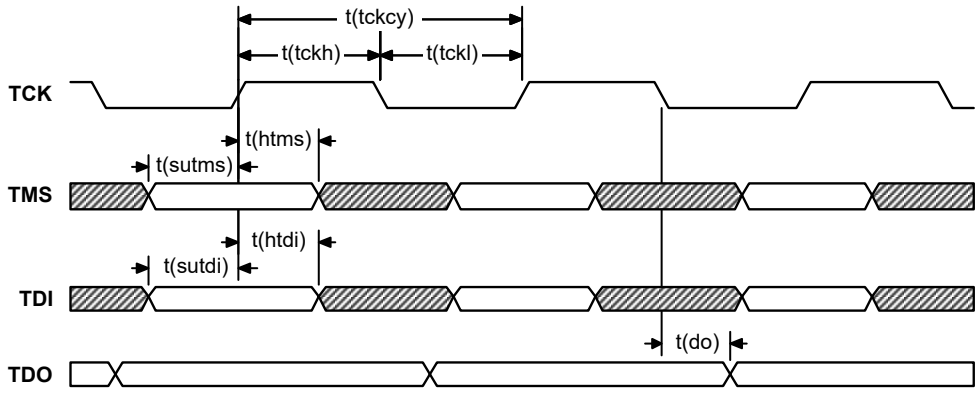


Figure 3-13 JTAG interface timing diagram

The supported JTAG interface timing characteristics are listed here.

Table 3-31 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.12.4 SWD

The following figure shows the SWD write and read AC timing diagram.

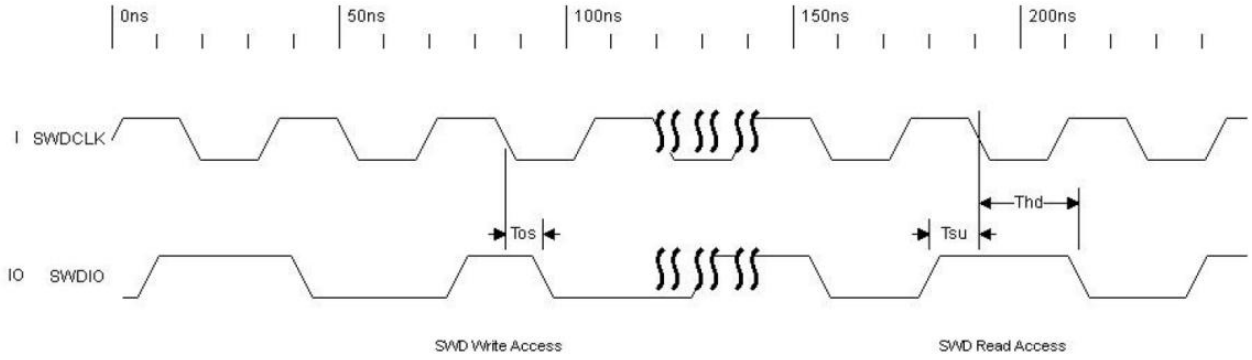


Figure 3-14 SWD write and read AC timing diagram

The supported AC timing parameters are listed here.

Table 3-32 AC timing parameters

Parameter [a]		Min	Max	Unit
T_{os}	SWDIO output skew to the falling edge of SWDCLK	-1	T - 7.5	ns
T_{su}	Input setup time between SWDIO and the rising edge of SWDCLK	6.5	s	ns
T_{hd}	Input hold the time between SWDIO and the rising edge of SWDCLK	6.5	–	ns

[a] SWDCLK runs at 20 MHz or lower.

3.13 RF front end (RFFE)

The supported RFFE standards and their exceptions are listed here.

Table 3-33 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for RF Front-End Control Interface version 2.0	None

3.14 System power management interface (SPMI)

The supported SPMI standards and their exceptions are listed here.

Table 3-34 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

This topic provides IC mechanical information including dimensions, markings, ordering information, and thermal characteristics.

4.1 Device physical dimensions

The QCS6490 and QCS5430 chipsets are available in the 1287 PSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. It has 1287 pins, with a pitch of 0.35 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. The following figure shows a simplified version of the package outline drawing.

Click the *Package Outline Drawing PSP1287, 14.0 × 12.0 × 0.91 mm, M530, S164* (NT90-18083-1) to download the drawing.

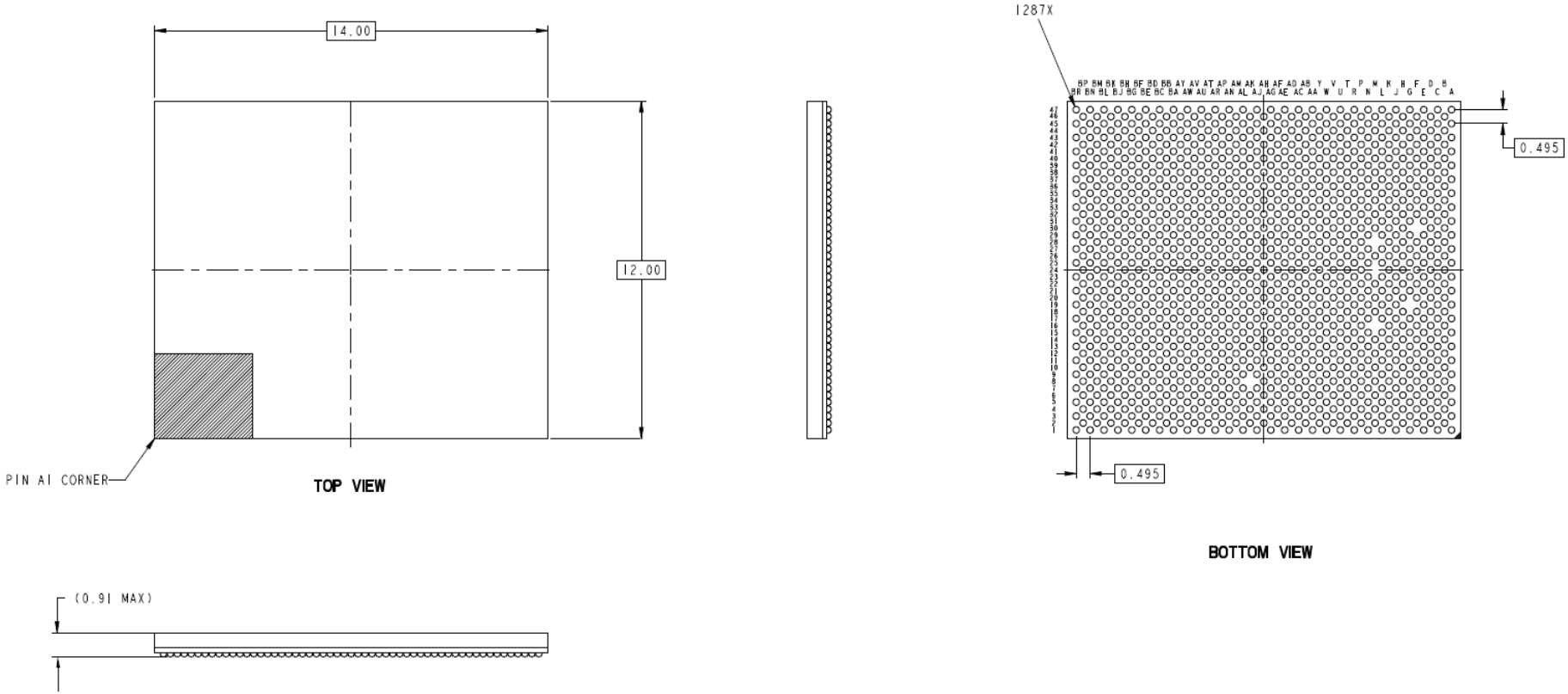


Figure 4-1 1287 PSP outline drawing

4.2 Part marking

The markings located on the top side of the chip are presented here.

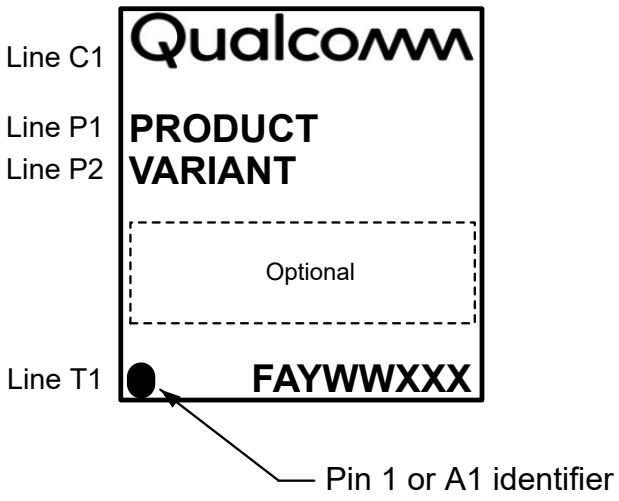


Figure 4-2 QCS6490 device marking (top view, not to scale)

Table 4-1 QCS6490 device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ QCS6490 ▪ QCS5430
P2	VARIANT	Device variant information ▪ For the assigned values, see Table 4-3.
	Blank or random	Optional information
T1	•	Pin 1 or pin A1 indicator
	FAYWWXXX	F = supply source code ▪ F = F (TSMC) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = H (JCET STATS ChipPAC, Korea) ▪ A = K (SPIL, Taiwan) Y = single/last digit of the year WW = two-digit work week of year specified by Y XXX = traceability number

4.3 Device ordering information

The short description is used to order QTI products, and is present on both the customer label and in this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code as shown in the following table:

Table 4-2 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	QCS-6490	-1	-PSP	1287			-TR	-00	-0	-AA
	QCS-5430	-1	-PSP	1287			-TR	-00	-0	-AA

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the short description ends after the source configuration code (S).

For example:

- QCS-6490-1-PSP1287-TR-00-0-AA
- QCS-5430-1-PSP1287-TR-00-0-AA

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

For availability and information to order QTI products, contact the Qualcomm sales team.

The following table summarizes the device identification details for all samples:

Table 4-3 Device identification details

Device	Sample type	Variant (PRR-BB) [a]	Hardware revision number [b]	FEATURE_ID [c]	Hardware version	Source configuration code (S) [d]	Comments	Sample date
QCS6490	ES	100-AA	0x0 0198 0E1	0x0	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; with GPS support; Tj = 95°C	4/7/2021
QCS6490	CS The CS date code is: ■ SPIL: 129	100-AA	0x0 0198 0E1	0x0	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; with GPS support; Tj = 95°C	7/30/2021
QCS6490	ES	200-AA	0x0 0198 0E1	0x0	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; without GPS support; Tj = 95°C	10/21/2022
QCS6490	CS The CS date code is: ■ SPIL: 211	200-AA	0x0 0198 0E1	0x3	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; without GPS support; Tj = 95°C	12/08/2022
QCS6490	ES	300-AA	0x0 0198 0E1	0x4	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; with GPS support; Tj = 105°C	10/30/2023
QCS6490	CS The CS date code is: ■ SPIL: 351	300-AA	0x0 0198 0E1	0x4	v1.0	0	CPU 1 × 2.7 GHz, 3 × 2.4 GHz, 4 × 1.9 GHz; with GPS support; Tj = 105°C	12/15/2023
QCS5430	ES	100-AA	0x0 020 F 0E1	0x0	v1.0	0	■ Feature pack 1: CPU 2 × 2.1 GHz, 4 × 1.8 GHz; with GPS support; Tj = 95°C ■ Feature pack 2: CPU 4 × 2.1 GHz, 4 × 1.8 GHz; with GPS support; Tj = 95°C	5/31/2022
QCS5430	CS The CS date code is: ■ SPIL: 212	100-AA	0x0 020 F 0E1	0x0	v1.0	0	■ Feature pack 1: CPU 2 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 95°C ■ Feature pack 2: CPU 1 × 2.2 GHz, CPU 3 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 95°C ■ Feature pack 2.5 and 3 [e]: CPU 1 × 2.38 GHz, CPU 3 × 2.4 GHz, 4 × 1.8 GHz; with GPS support; Tj = 95°C	7/27/2022

Table 4-3 Device identification details (cont.)

Device	Sample type	Variant (PRR-BB) [a]	Hardware revision number [b]	FEATURE_ID [c]	Hardware version	Source configuration code (S) [d]	Comments	Sample date
QCS5430	ES	300-AA	0x0 020 F 0E1	0x2	v1.0	0	■ Feature pack 1: CPU 2 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 105°C ■ Feature pack 2: CPU 4 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 105°C	10/30/2023
QCS5430	CS The CS date code is: ■ SPIL: 351	300-AA	0x0 020 F 0E1	0x2	v1.0	0	■ Feature pack 1: CPU 2 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 105°C ■ Feature pack 2: CPU 1 × 2.2 GHz, CPU 3 × 2.13 GHz, 4 × 1.8 GHz; with GPS support; Tj = 105°C ■ Feature pack 2.5 and 3 [e]: CPU 1 × 2.38 GHz, CPU 3 × 2.4 GHz, 4 × 1.8 GHz; with GPS support; Tj = 105°C	12/15/2023

[a] P = product configuration code; RR = product revision code; BB = feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
[b] For more information on JTAG_ID, see Table 4-5.
[c] For more information on FEATURE_ID, see Table 4-5. The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[d] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-4.
[e] Software enablement for feature packs 2.5 and 3 is under progress.

Table 4-4 Source configuration code

S value	Die	F value = F
0	Digital	TSMC
Other columns and rows will be added in future revisions of this document, if needed.		

Table 4-5 QFPROM_CORR_PTE_ROW0_LSB

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

The device identification register allows the user to determine the device's manufacturer, part number, and version via the test access port (TAP). The 32-bit device identification register is read through the JTAG interface and is summarized in the following table.

Table 4-6 Device identification register

Bit location	Description	Value [a]
bits [31:28]	Version data (may change with a sample type)	0x0
bits [27:12]	Part number (changes with a sample type)	01CC
bits [11:1]	Manufacturer identity code (administered by JEDEC)	070 (QTI code)
bit [0]	Device identification register start bit	Always = 1

[a] The hardware revision numbers for all sample types are provided in Table 4-3.

4.4 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the Qualcomm.com website. Designers can extract thermal resistance values by conducting their own thermal simulations.

Click *QCM6490 Package Thermal Model Icepak* (HS11-20659-5HW) and the *QCM6490 Package Thermal Model FloTHERM* (HS11-20659-6HW) to download the package thermal models.

NOTE The same Icepak and FloTHERM package thermal models are applicable to QCS6490 and QCS5430 chipsets.

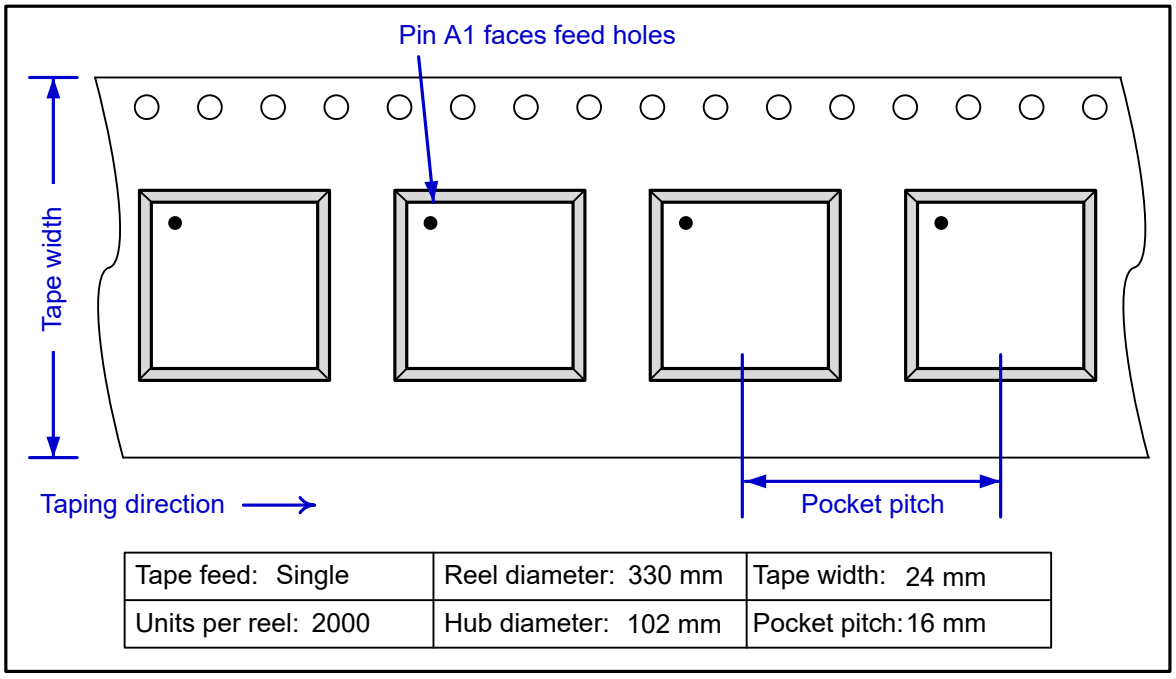
5 Carrier, storage, and handling information

This topic discusses shipping, storage, and handling of this chipset.

5.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

The following figure shows the simplified sketch of the QCS6490 and QCS5430 chipsets tape carrier including the part orientation, maximum number of devices per reel, and key dimensions.



Tape feed: Single	Reel diameter: 330 mm	Tape width: 24 mm
Units per reel: 2000	Hub diameter: 102 mm	Pocket pitch: 16 mm

Figure 5-1 Carrier tape drawing with part orientation

The following figure shows the tape-handling recommendation.

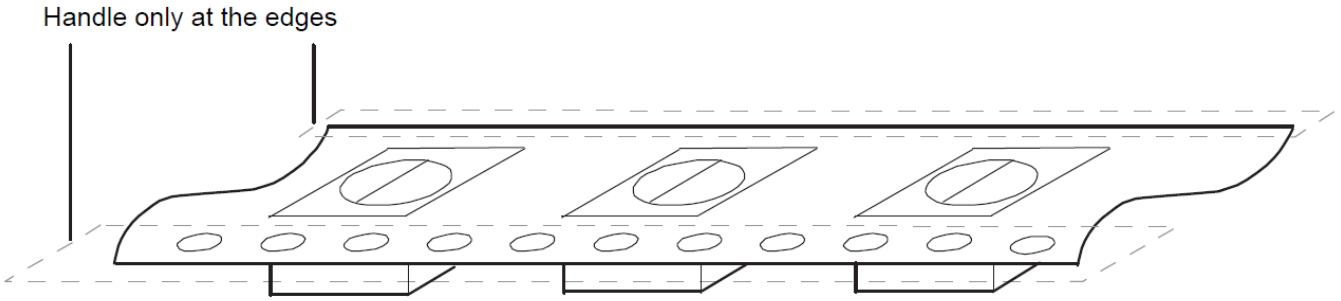


Figure 5-2 Tape handling

5.2 Matrix tray information

All matrix tray media is available for sampling only. All QTI matrix tray carriers conform to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray. The following table lists the key dimensions:

Table 5-1 Matrix tray key dimensions

Array	Key dimensions
M	15.45
M1	15.10
M2	17.80
M3	15.00
Units per tray	8 × 17 (136)

The following figure shows the matrix tray orientation.

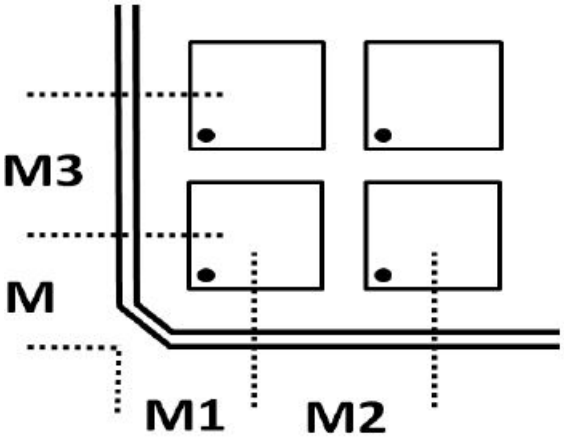


Figure 5-3 Matrix tray orientation

5.3 Device moisture sensitivity level

Plastic-encapsulated surface-mount packages are susceptible to damage induced by absorbed moisture and high temperature. A moisture sensitivity level (MSL) indicates the ability for a package to withstand exposure after it is removed from its shipment bag before PCB installation. A low MSL rating is better than a high rating; a low MSL device is exposed longer than a high MSL device. The following table summarizes all pertinent MSL ratings:

Table 5-2 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **QCS6490 and QCS5430 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH

Table 5-2 MSL ratings summary (cont.)

MSL	Out-of-bag floor life	Comments
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After baking, it must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The QCS6490 and QCS5430 devices are classified as MSL3; the qualification temperature was 255ºC.*** Do not confuse this qualification temperature (255°C) with the peak temperature within the recommended solder reflow profile.

5.4 Bagged storage conditions

QCS6490 and QCS5430 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. For the expected shelf life, see *IC Products Packing Method* (80-VK055-1).

5.5 Out-of-bag duration

The out-of-bag duration is the time that a device can be exposed before being installed onto a PCB.

5.6 Handling

Tape handling is described in Tape and reel information. For other (IC-specific) handling guidelines, see the following topics.

5.6.1 Baking

It is not necessary to bake the QCS6490 and QCS5430 chipsets if the conditions specified in Bagged storage conditions and Out-of-bag duration have not **been exceeded**.

It is necessary to bake the QCS6490 and QCS5430 chipsets if any condition specified in Bagged storage conditions or Out-of-bag duration has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag. For more details, see *IC Products Packing Method* (80-VK055-1).

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Do not bake devices in tape and reel carriers at any temperature.

5.6.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.7 Bar code label and packing for shipment

For all packing-related information, including bar code label details, see the *IC Products Packing Method* (80-VK055-1) document.

6 PCB mounting guidelines

This topic provides specifications for mounting the QCS6490 and QCS5430 onto PCBs.

6.1 RoHS compliance

This device meets the substance restriction requirements of the EU RoHS directive. For solder ball composition, see Table 7-3.

For more information, see *Product Material Declaration - QCS6490* (80-VG591-393C) and *Product Material Declaration - QCS5430* (80-VG591-433C) that provides RoHS and other product environmental governance details.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see *SMT Assembly Guidelines* (SM80-P0982-1).

7 Part reliability

This topic provides the reliability data, including a definition of the qualification samples and a summary of qualification test results.

7.1 Reliability qualification summary

The following table provides the reliability evaluation report for QCS6490 and QCS5430 for the foundry source TSMC-F15.

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from 3 different wafer lots)	333	Pass
HTOL in FIT (I) failure in billion device hours HTOL: JESD22-A108-A (Total samples from 3 different wafer lots)	333	Pass
Mean time to failure (MTTF) t = 1/I in million hours (Total samples from 3 different wafer lots)	333	> 20
ESD – human-body model (HBM) rating JS001-2017 (Total samples from 1 wafer lot)	21	Pass ±1 kV
ESD – charged-device model (CDM) rating JS-002-2014 (Total samples from 1 wafer lot)	6	Pass ± 250 V
Latch-up (I-test): EIA/JESD78E Trigger current: ±100 mA; temperature: 85°C (Total samples from 1 wafer lot)	6	Pass Class II, Level A
Latch-up (Vsupply overvoltage): EIA/JESD78E Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 85°C (Total samples from 1 wafer lot)	6	Pass Class II, Level a

The following table provides the package reliability results for QCS6490 and QCS5430.

Table 7-2 Package reliability results

Tests, standards, and conditions	ASE sample size	SPIL sample size	SCK sample size	Results
Moisture resistance test (MRT): J-STD-020C MSL3, reflow at 260 +0/-5°C (Total samples from 3 different assembly lots)	2205	2205	2250	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes	765	765	765	Pass

Table 7-2 Package reliability results (cont.)

Tests, standards, and conditions	ASE sample size	SPIL sample size	SCK sample size	Results
Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C (Total samples from 3 different assembly lots)				
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C (Total samples from 3 different assembly lots)	715	715	715	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-H MSL3, reflow temperature: 260 +0/-5°C (Total samples from 3 different assembly lots)	360 Pass	360	351	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 500, 1000 hours (Total samples from 3 different assembly lots)	765	765	765	Pass
Flammability Note: Flammability test – not required UL-STD-94	–	–	–	Note [a]
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document (Total samples from 3 different assembly lots at each SAT)	30	30	30	Pass
Die shear MIL-STD-883E, Method 2019 (Total samples from 3 different assembly lots at each SAT)	30	30	30	Pass [b]
Solder bump shear (Total samples from 3 different assembly lots at each SAT)	30	30	30	Pass [b]
Solder ball shear: JESD22-B117 (Total samples from 3 different assembly lots at each SAT)	30	30	30	Pass [b]
Internal/external visual (Total samples from 3 different assembly lots at each SAT)	30	30	30	Pass

[a] Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted, are rated V-0 (better than V-1).

[b] Data is based on other previously qualified PSP packages that are similar to this configuration.

7.2 Qualification sample description

The following table provides details of the category and definition of the device.

Table 7-3 Device characteristics

Category	Definition
Device name	QCS6490 and QCS5430
Package type	1287 PSP
Package body size	14.0 × 12.0 × 0.91 mm
Ball count	1287
Ball composition	SAC125/Ni
Fab process	6 nm
Supply sources (fab sites)	TSMC
Assembly sites	ASE, Taiwan; JCET STATS ChipPAC, Korea; SPIL, Taiwan
Solder ball pitch	0.35 mm

8 Samples and known issues

This topic discusses the issues, regardless of the sample type (or types) on which they occur.

8.1 Sample testing

For device identification details, see Table 4-3.

8.1.1 Engineering samples (ES)

These devices undergo limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Do not use engineering samples for product-level qualification.

8.1.2 Commercial samples (CS)

These devices undergo full production-level testing, and meet the specifications and features described in the data sheet, except as otherwise noted in this document. They have passed device level qualification. Commercial samples are suitable for performance testing, and also for product level production and qualification.

8.2 Known issues

There are no known issues in the QCS6490 and QCS5430 chipsets.

9 Revision history

The following table lists the technical content changes for all revisions.

Revision	Date	Description
AW	September 2025	■ Table 3-1 *Absolute maximum ratings*: Updated maximum value of VDD_GFX ■ Operating conditions: ▫ Updated maximum value of VDD_GFX ▫ Added footnote to VDD_APC0, VDD_APC1, VDD_GFX, VDD_MX, and VDD_A_USBHS_3P1
AV	August 2025	■ *Camera interfaces*: Corrected the camera interfaces support for QCS6490 and QCS5430. ■ *Operating conditions*: Added a note regarding the operating condition specifications. ■ *Digital-logic characteristics*: ▫ Added a note regarding the digital logic characteristics specification. ▫ Added possible drive strength for all V_{OL} and V_{OH} parameters.
AU	October 2024	■ *Wireless conectivity*: Removed satellite-based augmentation system (SBAS) for QCS6490 and QCS5430. ■ *Internal functions*: Removed Secure digital (SD) card for QCS6490 and QCS5430.
AT	July 2024	This revision includes the following changes: ■ Global change: ▫ Optimized figures for dark mode. ▫ Added note for feature pack 2.5 and 3. ▫ Removed the note on PCIe1 support. ■ Table 4-3 *Device identification details*: Added CS related information for QCS6490 and QCS5430 feature pack 2.5 and 3 for 300-AA variant.
Revision AS was omitted in accordance with QTI document conventions.		
AR	April 2024	The document has undergone editorial changes. The technical content remains unchanged.
Revision AQ was omitted in accordance with QTI document conventions.		
AP	March 27, 2024	Global: Restructured the document to adhere to HTML standards. Review the document in entirety. This revision includes the following changes: ■ Processor: Added CPU performance of QCS5430 for feature pack 2.5 and for feature pack 3. ■ Multimedia: Added camera description for QCS5430 feature pack 2.5 and for feature pack 3. ■ Table: Device identification details: Added CS related information for feature pack 2.5 and for feature pack 3.
Revision AO was omitted in accordance with QTI document conventions.		
AN	March 2024	■ Section 1.3 *QCS6490 and QCS5430 features*: Updated the features table. ■ Table 4-6 *Device identification register:* Added this table. ■ Chapter 8 *Samples and known issues*: Added this section.
AM	October 2023	■ Table 3-2 *Operating conditions*: Added thermal condition information for 300-AA variant. ■ Table 4-3 *Device identification details*: Added Information in this table.
AL	April 2023	Section 3.4.1 *Average operating current*:: Updated the current consumption document details.
AK	December 2022	Table 4-4 *Device identification details:* Added QCS6490 CS sample information.

Revision	Date	Description
AJ	October 2022	■ Table 2-3 *Pin descriptions – general-purpose input/output ports*: Added a note for GPIO_76, GPIO_77, GPIO_78, GPIO_79, GPIO_105, GPIO_106, and GPIO_107 regarding GP_CLK information ■ Table 4-4 *Device identification details*: Added QCS6490 ES sample information
Revision AI was omitted in accordance with QTI document conventions		
AH	August 2022	■ Table 1-1 *QCS6490 and QCS5430 features*: Updated the table with display support and VPU support ■ Table 4-4 *Device identification details*: Added QCS5430 CS sample information
AG	May 2022	■ Global: Added QCS5430 Feature Pack 1 and Feature Pack 2 details throughout the document ■ Cover: □ Added the Adreno GPU value for QCS5430 □ Added the camera support and NVMe support for QCS5430 ■ Figure 1-2 *QCS5430 functional block diagram*: Added QCS5430 functional block diagram ■ Table 1-1 *QCS6490 and QCS5430 features*: Added FP1 and FP2 details, camera support, NVMe support, and Adreno GPU support for QCS5430 ■ Table 4-4 *Device identification details*: Added QCS5430 ES sample information
AF	April 2022	■ Global: Updated the Adreno GPU 642 L to 643
AE	December 2021	■ Figure 1-1 *QCS6490 functional block diagram*: Updated the block diagram ■ Table 1-1 *QCS6490 features*: Updated the table
AD	August 2021	■ Chapter 3 *Electrical specifications*: Added information in the following tables: □ Table 3-1 *Absolute maximum ratings* through Table 3-12 *Supported SD standards and exceptions* ■ Table 4-4 *Device identification details*: Updated CS details ■ *Part reliability*: Added this chapter
AC	June 2021	■ Global: □ Updated Kryo CPU 6xx to 670 □ Updated Adreno GPU 6xx to 642 L □ Updated Spectra ISP 5xx to 570 L □ Added PMK7325-1 and PM7250B-2 support □ Added SMB1355 and SMB1394 support ■ Section 5.1.2 *Matrix tray information*: Added this section
AB	April 2021	■ Global: □ Updated the Kryo Gold application frequency □ Updated the LPDDR5 SDRAM frequency to 3200 MHz ■ Table 1-1 *QCS6490 features*: □ Updated the video decode 4K60 ■ Section 3.3 *Power delivery network specification*: Added this section ■ *Mechanical information*: Added the following sections: □ Section 4.2 *Part marking* □ Section 4.3 *Device ordering information* □ Section 4.4 *Device moisture sensitivity level* □ Section 4.5 *Thermal characteristics*

Revision	Date	Description
		■ *Carrier, storage, and handling information*: Added information ■ *PCB mounting guidelines*: Added information
AA	December 2020	Initial release

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