
CIX CP8180

Datasheet Brief

Preliminary Rev D

For Reference Only

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Introduction

SOC Features

The CP8180 is the model number of CIX's first-generation big. LITTLE-core, 64-bit Armv9.2-based, general-purpose SOC, built for the development board.

The CP8180 is a SOC (System-On-Chip), which includes CPU, GPU, NPU, VPU, ISP, CSU, HSIO, LSIO, etc. subsystems fabricated onto one common Die/chip.

SOC Core Features

Table 1 SOC Core Features

Item	Descriptions
Purpose	CP8180 was designed as a general-purpose SoC
Package	FBGA 27x36x1.743mm, 1979x balls
TDP	28~35W
Technology Node	6nm TSMC
CPU	■ (Big core) Arm Cortex A720X4 ■ (Medium core) Arm Cortex A720X4 ■ (Little core) Arm Cortex A520X4 12MB L3 shared across all cores
GPU	Arm Immortalis-G720 MC10
VPU	■ Video decode up to 8K@60 fps ■ Video encode up to 8K@30 fps
Audio	■ Dedicated audio DSP
ISP	■ 8k@15FPS video recording ■ Max 4 cameras

Item	Descriptions
HSIO	■ USB: - o 4x USB3.2 Gen2 Type C (one dual-role port) - o 2x USB 3.2 Gen2 Type A Dual Role - o 4x USB 2.0 ■ MIPI CSI, DP ■ PCIe 4.0 Interfaces: - o 2 × X1 links - o 1 × X2 link - o 1 × X4 link - o 1 × X8 link
LSIO	■ SPI ports ■ I2S ■ PWM ■ I2C ■ I3C ■ UART support
Memory	■ 4x32 bits ■ LPDDR4X up to 4267Mbps ■ LPDDR5 up to 6400Mbps
Display	■ Max of 10 simultaneously display monitors ■ Max resolution for each display is 4K@120FPS (not simultaneously) ■ Support RGB, YUV422/420 ■ 1x DP/eDP ■ 2xDP over DP/USB Combo ■ Support 2 streams MST for each DP port ■ HDCP 1.3/1.4 and 2.2/2.3
NPU	■ Up to 30 TOPS

Item	Descriptions
Security	■ Crypto engine to support AES/SHA/ECC/TRNG/RSA/DRM/SM2/SM3/SM4; ■ Secure boot ■ Secure element (SE) ■ Life cycle management ■ Key provision ■ System configuration security management and System data security management ■ MTE ■ TrustZone ■ Crypto extension
Power Management	DVFS, DFS; xPU Runtime; CPU Idle; S3/S4/S5

Block Diagram

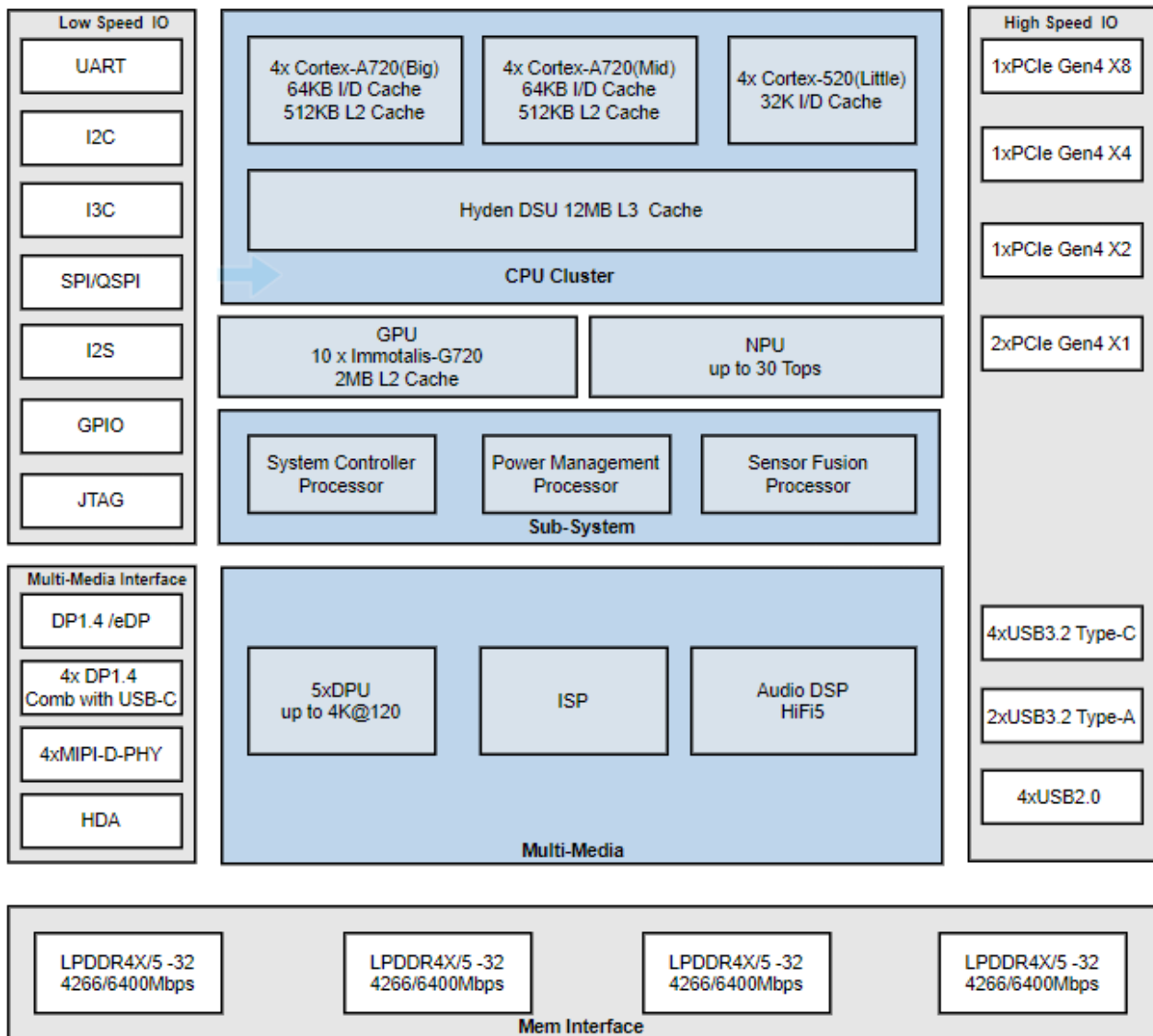


Figure 1 Block Diagram

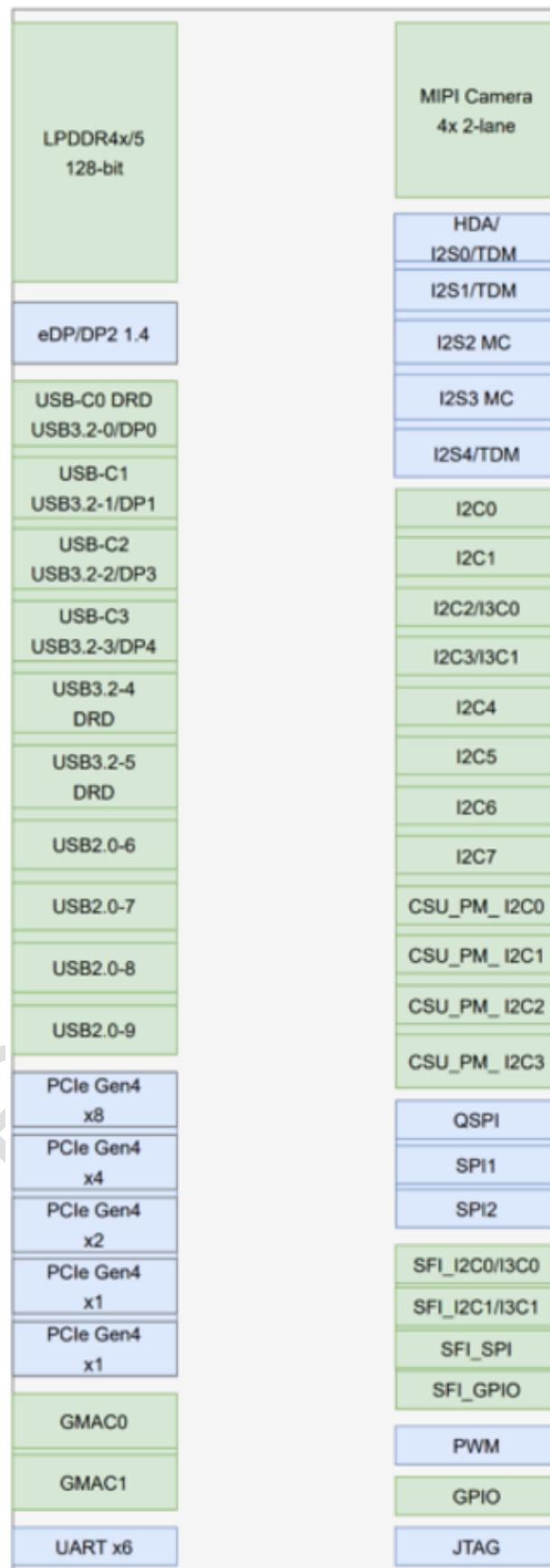


Figure 2 CP8180 I/O Block Diagram

GPU Features

- Arm Immortalis-G720
- API: OpenGL ES3.2, Vulkan 1.3, OpenCL 3.0

NPU Features

Table 2 NPU Features

Feature	Capability
TEC General-Purpose Functions	General-purpose unit includes scalar processing unit (SPU), vector/tensor processing engine (VPE) and floating-point processing unit (FPU)
AI Fixed Functions	■ AI fixed function (AIFF) accelerator supports: ■ Matrix-to-Tensor Processing (MTP) ■ Intro-tensor and Inter-Tensor processing (ITP) ■ Planar-to-tensor processing (PTP)
Memory Hierarchy	Allows for a balance between the need for fast access to frequently used data and the need for larger storage capacities at a lower cost.

VPU Features

Table 3 VPU Features

Item	Capability
VPU features	■ Supports dynamic power gating of each core and the whole VPU subsystem. ■ CP8180 VPU supports multi-session decoding and encoding. ■ Support for YUV420, 8-bit, or 10-bit depth. ■ Video encoded up to 8K@30 fps.

Item	Capability
	■ Native encode supports for H.265 Main/Main 10 Profile, H.264 Baseline/Main/High/High 10, VP9 profile 0/profile 2(10bits), VP8. ■ Encode supports for stride, horizontal and vertical mirroring, and optional rotation of the source frame in 90 degrees. ■ Encode supports I/P/B frame progressive encoding. ■ Encode supports constant bit rate control and variable bit rate control. ■ Video decode up to 8K@60 fps. ■ Native decode supports AV1 Main Profile (8/10 bits), H.265 Main/Main 10 Profile, H.264 Baseline/Main/High/High 10, VP9 Profile 0/Profile 2 (10 bits), VP8, H.263, and MPEG-4/MPEG-2 codecs. ■ Decode supports stride, rotation of the output frame by 90 degrees, and scaling. ■ Decode supports error concealment and stream parameter information output. ■ Support AFBC 16 x16 super-block 8/10bits Input and Output.

Audio Features

Table 4 Audio Subsystem

Item	Components
Audio subsystem	■ DSP x1: a processor for high-performance audio data processing ■ DMA engine x1 ■ HDA x1 ■ AUD_CRU x1: For sub-system control ■ Mailbox x2; Timer x1; WDT x1 ■ I2S x10 ■ SRAM up to 1MB

Table 5 Audio Features

Feature	Capability
Audio subsystem	■ Support multiple sample rate, 8k/11.025k/22.05k/32k/44.1k/48k/96k/192k ■ Support multiple bit width, 8b/16b/24b/32b ■ Support multiple channel numbers, mono, stereo, 2.1, 5.1, 7.1 ■ Support HDA interface codec ■ Dedicated audio DSP

Display Features

DPU Features

- CP8180 DPU: 4K

Table 6 DPU Features

Item	Descriptions
Display Processing Unit (DPU) Display Interface/ Performance	■ DPU provides various functions that support graphics processing. These functions relieve loading on the main graphics processing unit and provide image composition for display. ■ DPU has 2 separate display pipelines. ■ DPU supports up to 4K@60Hz display resolution for single display, and up to 4K@120Hz resolution for image merge display. ■ DPU processor provides: ■ Layer pre-processing - Support for reading display layers of various pixel formats - Image rotation by 90,180, and 270 degrees, flip horizontally and vertically - Image cropping, AFBC decoding, and AFBC encoding - Image scaling and enhancement, color space conversion, gamma transformation

Item	Descriptions
	■ Multi-layer composition - Composition of up to 8 layers - Programmable Z-order of display layers before scaling - Support pixel alpha and layer alpha - Support trusted layer composition ■ Rich post-processing features - Scaling and memory-writeback of composition result - Dithering, color space conversion, gamma transformation ■ Support of display operations - Side-by-side processing

DP Features

Table 7 DP Features

Item	Descriptions
DP (DisplayPort)	■ DisplayPort 1.4 TX - Support SDP - HDCP (High-bandwidth Digital Content Protection) - SST & MST (Single Stream Transport & Multi-Stream Transport) (up to 2 sources) ■ Full link rate & lane count - Support 1,2, or 4 lanes - Main link rates from 1.62Gbps to 8.1Gbps ■ Embedded DisplayPort 1.4a ■ Aux Channel transaction ■ Hot Plug Detection

USB Features

- Support 4x USB2 host-only

- Support 2x USB SSP DRD controller with Type-A interface
- Support 1x USB SSP DRD controller with Type-C interface
- Support 3x USB SSP host-only controller with Type-C interface

For detailed USB interfaces please refer to the block diagram.

LPDDR4x/5 Controller

- Width of Memory Data Bus (in Bits): 32bits per controller
- Maximum data rate (in MT/S):
 - LPDDR4X up to 4267Mbps
 - LPDDR5 up to 6400Mbps
- Protocols: LPDDR5/4X

PCI Express® Interface

- PCI Express(PCIe®) Controller quantities: 3
- PCIe Gen4, 16GT/S

Table 8 PCIe Interface

PCIe Link	X1_0	X1_1	X2	X4	X8
Pin Name	PCIE3	PCIE4	PCIE2	PCIE1	PCIE0
RC Mode	Y	Y	Y	Y	Y
EP Mode	N	N	N	N	N
Traffic Type	WIFI	Ethernet	5G	NVMe	GPU
Power Gating	N	N	N	N	Y
Highest Generation	Gen4	Gen4	Gen4	Gen4	Gen4
Max Lane Number	1	1	2	4	8

LSIO

- DMA
- 4x UART
- 2x SPI
- 2x I3C
- 1x xSPI
- 8x I2C
- 1x Timer inside
- 1x IO_S0
- 4x general I/O controller

CIX System Unit

CIX System Unit (CSU) has 2x instances, CSU_SE and CSU_PM.

CSU_SE

The CSU_SE is a dedicated processor or hardware module within an ARM-based SoC (System on Chip) responsible for secure boot and handling security-related tasks. It is designed to provide a secure environment for executing sensitive operations and storing sensitive data, separate from the main application processor. This includes boot code, security firmware, and the cryptography coprocessor.

CSU_PM

The CSU_PM is a component that runs based on a microarchitecture processor, which plays a crucial role in managing power, clock, and system control functions. It is responsible for coordinating and controlling various aspects of the system, such as power

management, thermal management, and system-level suspend and resume. CSU_PM includes a power management FW as well. This allows the CSU_PM subsystem to operate independently of the main application processor, enabling it to manage system resources and respond to events even when the main processor is in a low-power state.

Remote CSU

The remote CSU (RCSU) is organized as a set of AXI-enabled components communicating via the internal AXI/APB/AHB interconnect for each IP. The RCSU includes below functions:

- Security gasket for each IP configuration space
- SRAM memory repair
- Strap-pin management for each IP
- Power gating (PGFSM/PPU)
- Power Control
- Fuse distribution for some IPs

Acronyms and Abbreviations

The following is a list of the acronyms and abbreviations used in this manual.

Table 9 Acronyms and abbreviations

Acronym	Full Expression
ACPI	Advanced Configuration and Power Interface
DDR	Double Data Rate
DRAM	Dynamic RAM
DVD	Digital Video Disc
DVFS	Dynamic Voltage and Frequency Scaling
GPIO	General Purpose Input/Output

Acronym	Full Expression
I2C	Inter Integrated Circuit
I3C	Improved Inter Integrated Circuit
ISP	Image Signal Processor
IPA	Intelligent Power Allocation
JTAG	Joint Test Access Group. An IEEE standard.
MB	Mega Byte
MIPI	Mobile Industry Processor Interface
PCI	Peripheral Component Interface
PCIe	PCI Express
PLL	Phase Locked Loop
POST	Power On Self Test
SLC	System Level Cache
SPI	Serial peripheral Interface
TWS	True Wireless Stereo
VESA	Video Electronics Standards Association
WDT	Watchdog Timer