Radxa Dragon Q6A schematic

V1.20

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radxa

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When the recovery button is pressed, the device enters USB boot mode. Firmware download and USB boot have the highest priority, and other boot modes are disabled.

LPDDR5
32BIT
315 BALL

EMMC/UFS
Module

UFS Detected
EMMC Detected

BOOT
LOGIC

BOOT CFG

UFS detected
0b000
UFS →
SDC2→EDL(USB)

EMMC detected
0b001
eMMC
→SDC2→EDL(USB)

CARD Detected

USB Download

HDMI

RA620
DP 2LANE
TO
HDMI

DP 2LANE

SDIO 3.1

TF SLOT

USB
TYPE-C PWR IN

USB
CC

CH224D

12V IN

USB3.0*1

For HOST/DEVICE(ADB/EDL)

USB0 3.0

USB3.0*3

USB2.0*3

FE1.1S

USB2.0

USB1 2.0

DC/DC
12V-5V

HIGH Transient
current DC/DC
12V-4.2V

5V

4.2V For
VPH_PWR

USB3.0*1

USB2.0
Wifi Module
FCU760K

M.2 M-KEY
2230

PCIEX2

PCIe Gen 3 2-lane

QCS6490

2-lane CSI

CAM0

2-lane CSI

CAM1

4-lane CSI

CAM2

4-lane CSI

CAM3

4-lane EDP

EDP LCD

Optional by SW

4-lane MIPI DSI

MIPI LCD

DC/DC
LDOs

PM7325
PM7350C

3.3V

1.8V

DC/DC
LDOs

Peripherals

SYS

2.5G RJ45

MDI

RTL8125B

PCIEX1

PCIe Gen 3 1-lane

GPIOS

SPI
GPIO
IIC

40 Pins
GPIO
2.54mm

HP

MIC Array

WCD9380

SWR_TX/RX

Connector

Chips

Power IC

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Size	Title: RADXA DRAGON Q5A	REV
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QCM6490 CONTROL

CAD Note:
Single 50Ω
sensitive signals, away from noise sources/high speed signals..

CAD Note:
Add a placeholder cap to RESIN_N pin of QCM6490
meeting its max transition (rise/fall) time of 200 ns

unconnected for native mode

Pull-down:
to solve unexpected random boot issue

CAD Note:
Place the resistors connected to the REXT pins near to MSM
and route away from noisy siganls.

Ensure there is an external 10k pull-up resistor placeholder (DNI) on the SDC2_CMD for SD card.

single 45
Ω

diff 90
Ω

AUX

lane_0_1 DP0

lane_0_0 DP1

diff 85
Ω

lane_1_1 RX

lane_1_0 TX

diff 85
Ω

CAD Note:
PLACE SPMI resistors close to QCM
Route the SPMI signals in Daisy Chain/Start routing
from MSM to the PMICS to avoid stubs.

diff 90
Ω

Place away from PMIC and heat-sources

Place near to the QCM about 1cm and put into the shielding

Size C	Title: RADXA DRAGON Q5A		REV X1.0
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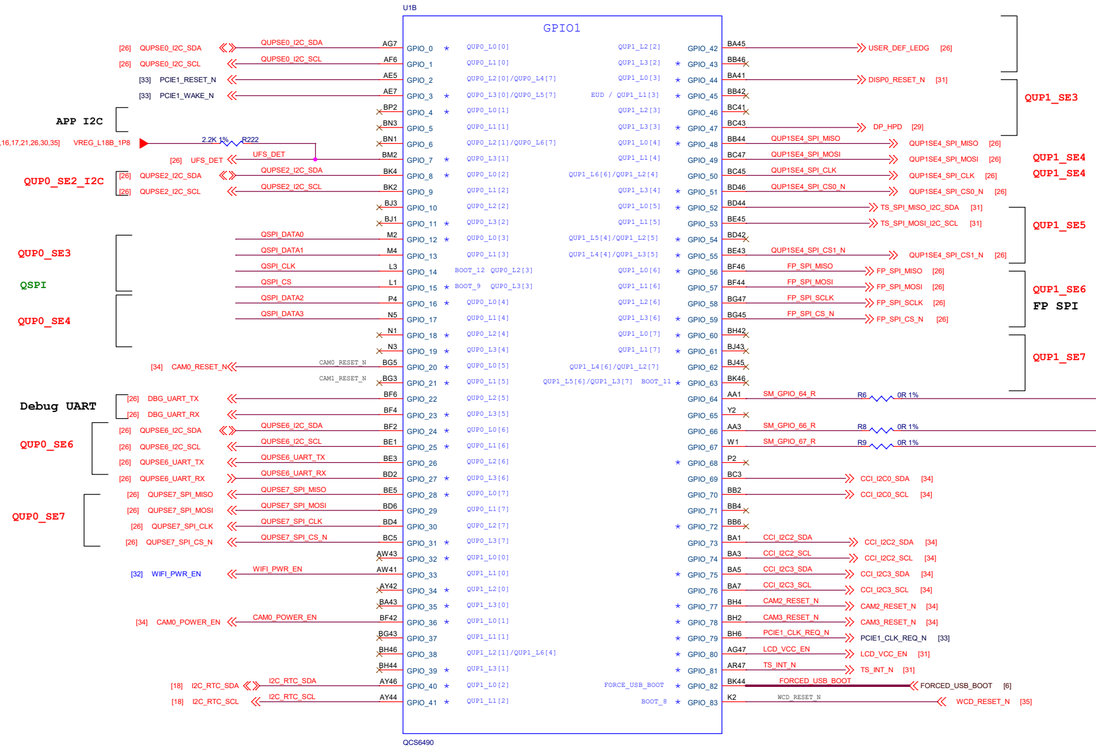
QCM6490 GPIO



Note:
Only one protocol can be selected in one QUP engine at a time.
For example, simultaneous UART and I2C functionality are no longer supported.

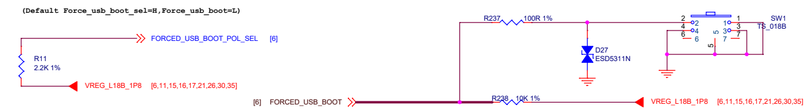
I/O	UART	I2C/I3C	SPI
QUP_L0	CTS	SDA	MISO
QUP_L1	RFR	SCL	MOSI
QUP_L2 SCLK	Tx –		
QUP_L3 CS_0	Rx –		
QUP_L4 CS_1	– –		
QUP_L5 CS_2	– –		
QUP_L6 CS_3	– –		

It is recommended to use GPIO_38 (internal pull up) for NFC_EN.
Add 12 K pull up to VDD_PX3. In case if other GPIO with internal pull down is re-purposed for NFC_EN, then this signal should have 2.7 K pull up to VDD_PX3. In such case software changes are required.

FORCE_USB_BOOT

Note:
The polarity of FORCED_USB_BOOT(GPIO_82) as active high or active low is set by FORCED_USB_BOOT_POLARITY_SEL(GPIO_139).

FORCED_USB_BOOT_POLARITY_SEL=L, FORCE_USB_BOOT=H;
FORCED_USB_BOOT_POLARITY_SEL=H, FORCE_USB_BOOT=L;



Typc C / Micro USB

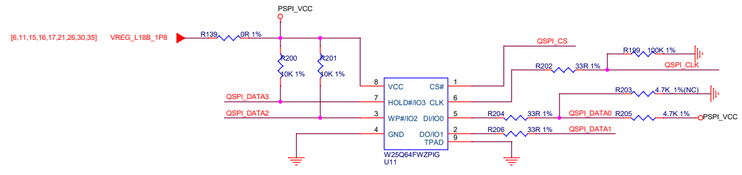
Type-C:
R710 = NC.
R707 = 0 ohm
R709 = NC

Micro USB: (USB_SS-H_HS-L_SEL connect to USB port ID pin)
R710 = 7.32K ohm within 1% accuracy.
R707 = NC
R709 = 0 ohm

I2C BUS pull-ups

Note:
All I2C bus pull-up resistors are placed on other board, unless they are used on the SOM.

QSPI FLASH FOR BOOT



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Size	Title: RADXA DRAGON Q5A		REV
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QCM6490 EBI0/1 LPDDR5

U1D

EBI0

[15] EBI0_WCK0_M	H18	EBI0_LP4_NC_LP5_WCK0_C				
[15] EBI0_WCK0_P	G17	EBI0_LP4_NC_LP5_WCK0_T				
[15] EBI0_WCK1_M	J11	EBI0_LP4_NC_LP5_WCK1_C				
[15] EBI0_WCK1_P	K10	EBI0_LP4_NC_LP5_WCK1_T				
[15] EBI0_CLK_M	E15	EBI0_LP4_CK_C_LP5_CK_C	EBI0_LP4_CS1_LP5_NC	F12		
[15] EBI0_CLK_P	F16	EBI0_LP4_CK_T_LP5_CK_T				
[15] EBI0_CS_1	C13	EBI0_LP4_CKE0_LP5_CS1				
[15] EBI0_CS_0	F14	EBI0_LP4_CKE1_LP5_CS0				
[15] EBI0_DMI_1	G9	EBI0_LP4_DMI0_LP5_DMI1	EBI0_LP4_DQ8_LP5_DQ0	B18	EBI0_DQ0	EBI0_DQ[0:15] [15]
[15] EBI0_DMI_0	A17	EBI0_LP4_DMI1_LP5_DMI0	EBI0_LP4_DQ9_LP5_DQ1	A19	EBI0_DQ1	
[15] EBI0_DQS_0_M	F20	EBI0_LP4_DQS1_C_LP5_DQS0_C	EBI0_LP4_DQ10_LP5_DQ2	B20	EBI0_DQ2	
[15] EBI0_DQS_0_P	G21	EBI0_LP4_DQS1_T_LP5_DQS0_T	EBI0_LP4_DQ11_LP5_DQ3	D18	EBI0_DQ3	
[15] EBI0_DQS_1_M	J7	EBI0_LP4_DQS0_C_LP5_DQS1_C	EBI0_LP4_DQ12_LP5_DQ4	D20	EBI0_DQ4	
[15] EBI0_DQS_1_P	K8	EBI0_LP4_DQS0_T_LP5_DQS1_T	EBI0_LP4_DQ13_LP5_DQ5	B16	EBI0_DQ5	
[15] EBI0_CA_0	D14	EBI0_LP4_CA0_LP5_CA0	EBI0_LP4_DQ14_LP5_DQ6	A15	EBI0_DQ6	
[15] EBI0_CA_1	A13	EBI0_LP4_CA1_LP5_CA1	EBI0_LP4_DQ15_LP5_DQ7	B14	EBI0_DQ7	
[15] EBI0_CA_2	B12	EBI0_LP4_CS0_LP5_CA2	EBI0_LP4_DQ0_LP5_DQ8	F6	EBI0_DQ8	
[15] EBI0_CA_3	A11	EBI0_LP4_CA2_LP5_CA3	EBI0_LP4_DQ1_LP5_DQ9	C5	EBI0_DQ9	
[15] EBI0_CA_4	D12	EBI0_LP4_CA3_LP5_CA4	EBI0_LP4_DQ2_LP5_DQ10	D6	EBI0_DQ10	
[15] EBI0_CA_5	E11	EBI0_LP4_CA4_LP5_CA5	EBI0_LP4_DQ3_LP5_DQ11	F8	EBI0_DQ11	
[15] EBI0_CA_6	G11	EBI0_LP4_CA5_LP5_CA6	EBI0_LP4_DQ4_LP5_DQ12	C7	EBI0_DQ12	
			EBI0_LP4_DQ5_LP5_DQ13	C9	EBI0_DQ13	
			EBI0_LP4_DQ6_LP5_DQ14	D8	EBI0_DQ14	
			EBI0_LP4_DQ7_LP5_DQ15	D10	EBI0_DQ15	

QCS6490

[13,15,21] VREG_L3B_0P504

U1E

EBI1

[15] EBI1_WCK0_M	J37	EBI1_LP4_NC_LP5_WCK0_C				
[15] EBI1_WCK0_P	K38	EBI1_LP4_NC_LP5_WCK0_T	EBI01_CAL	A3	EBI01_CAL	R17 240R 1%
[15] EBI1_WCK1_M	H30	EBI1_LP4_NC_LP5_WCK1_C				
[15] EBI1_WCK1_P	G31	EBI1_LP4_NC_LP5_WCK1_T	DNC_6	M30		
	F36	EBI1_LP4_CA2_LP5_NC				
[15] EBI1_CLK_M	E33	EBI1_LP4_CK_C_LP5_CK_C	DDR_RESET_N	F26	DDR_RESET_N [15]	
[15] EBI1_CLK_P	F32	EBI1_LP4_CK_T_LP5_CK_T				
[15] EBI1_CS_0	C35	EBI1_LP4_CKE0_LP5_CS0				
[15] EBI1_CS_1	F34	EBI1_LP4_CKE1_LP5_CS1				
[15] EBI1_DMI_0	G39	EBI1_LP4_DMI0_LP5_DMI0	EBI1_LP4_DQ0_LP5_DQ0	F42	EBI1_DQ0	EBI1_DQ[0:15] [15]
[15] EBI1_DMI_1	A31	EBI1_LP4_DMI1_LP5_DMI1	EBI1_LP4_DQ1_LP5_DQ1	C43	EBI1_DQ1	
[15] EBI1_DQS_0_M	J41	EBI1_LP4_DQS0_C_LP5_DQS0_C	EBI1_LP4_DQ2_LP5_DQ2	D42	EBI1_DQ2	
[15] EBI1_DQS_0_P	K40	EBI1_LP4_DQS0_T_LP5_DQS0_T	EBI1_LP4_DQ3_LP5_DQ3	F40	EBI1_DQ3	
[15] EBI1_DQS_1_M	F28	EBI1_LP4_DQS1_C_LP5_DQS1_C	EBI1_LP4_DQ4_LP5_DQ4	C41	EBI1_DQ4	
[15] EBI1_DQS_1_P	G29	EBI1_LP4_DQS1_T_LP5_DQS1_T	EBI1_LP4_DQ5_LP5_DQ5	C39	EBI1_DQ5	
[15] EBI1_CA_0	E37	EBI1_LP4_CA5_LP5_CA0	EBI1_LP4_DQ6_LP5_DQ6	D40	EBI1_DQ6	
[15] EBI1_CA_1	G37	EBI1_LP4_CA4_LP5_CA1	EBI1_LP4_DQ7_LP5_DQ7	D38	EBI1_DQ7	
[15] EBI1_CA_2	D36	EBI1_LP4_CA3_LP5_CA2	EBI1_LP4_DQ8_LP5_DQ8	B30	EBI1_DQ8	
[15] EBI1_CA_3	A37	EBI1_LP4_CS1_LP5_CA3	EBI1_LP4_DQ9_LP5_DQ9	A29	EBI1_DQ9	
[15] EBI1_CA_4	B36	EBI1_LP4_CS0_LP5_CA4	EBI1_LP4_DQ10_LP5_DQ10	B28	EBI1_DQ10	
[15] EBI1_CA_5	A35	EBI1_LP4_CA1_LP5_CA5	EBI1_LP4_DQ11_LP5_DQ11	D30	EBI1_DQ11	
[15] EBI1_CA_6	D34	EBI1_LP4_CA0_LP5_CA6	EBI1_LP4_DQ12_LP5_DQ12	D28	EBI1_DQ12	
			EBI1_LP4_DQ13_LP5_DQ13	B32	EBI1_DQ13	
			EBI1_LP4_DQ14_LP5_DQ14	A33	EBI1_DQ14	
			EBI1_LP4_DQ15_LP5_DQ15	B34	EBI1_DQ15	

QCS6490

CAD note: Place Res close to QCM

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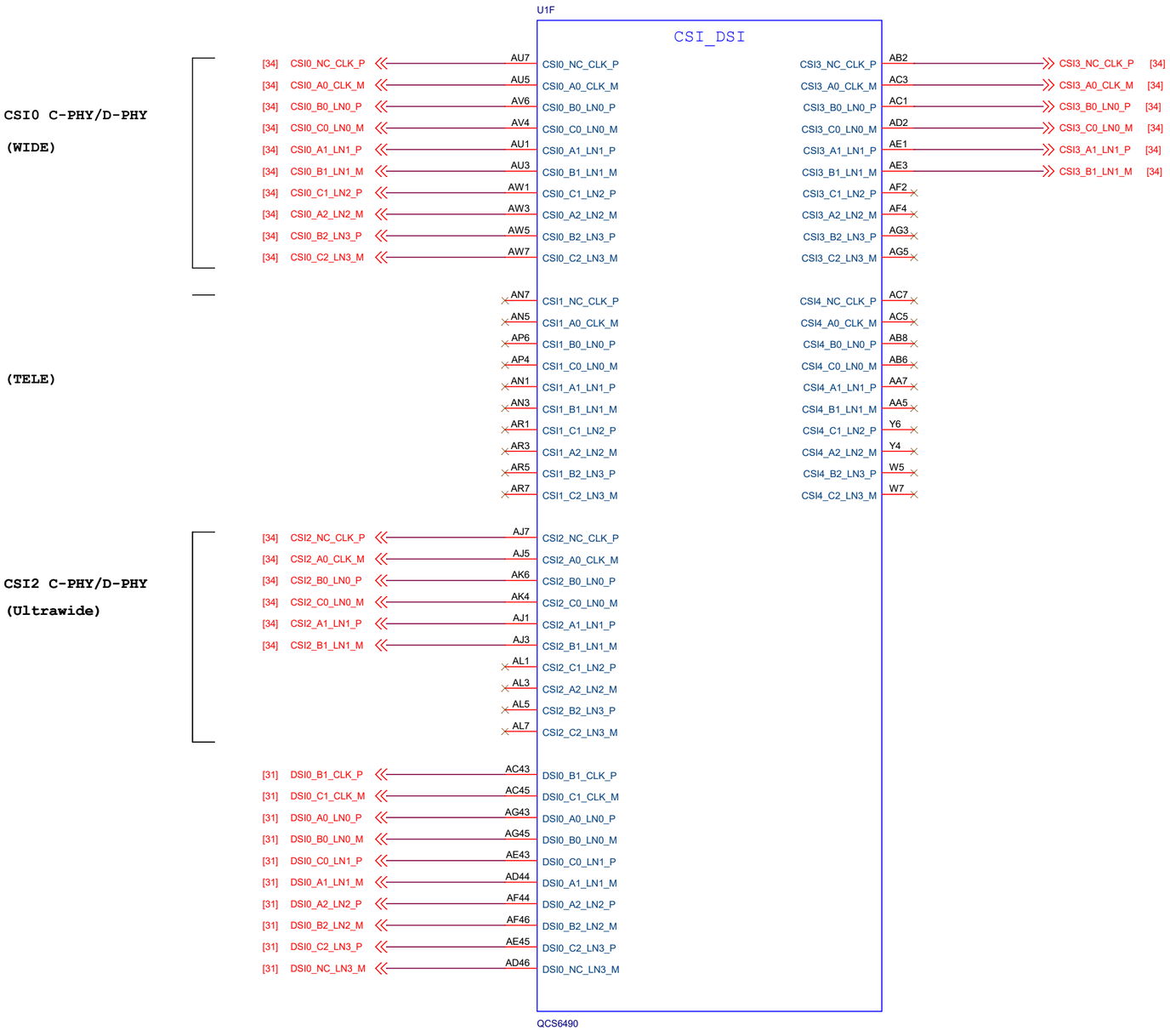
QCM6490 MIPI-CSI/DSI



ISP:
- three IFEs and two IFE lite
- up to five cameras may operate concurrently, up to eight sensors
- IFE lite ISP supports 5 MP at 30 fps

- 36 + 22 MP at 30 fps / 3 x 22 MP 30 fps ZSL
- five concurrent MIPI CSI configurable in 4 + 4 + 4+ 4 + 4 configuration

CSI lane mapping when a 4-lane interface is configured as 2-lane plus 1-lane interfaces:
- DCLK => DCLK_A
- DLN0 => DLN0_A
- DLN1 => DLN1_A
- DLN2 => DLN0_B
- DLN3 => DCLK_B

CSI lane mapping when a 4-lane interface is configured as 1-lane plus 1-lane interfaces:
- DCLK => DCLK_A
- DLN0 => DLN0_A
- DLN2 => DLN0_B
- DLN3 => DCLK_B

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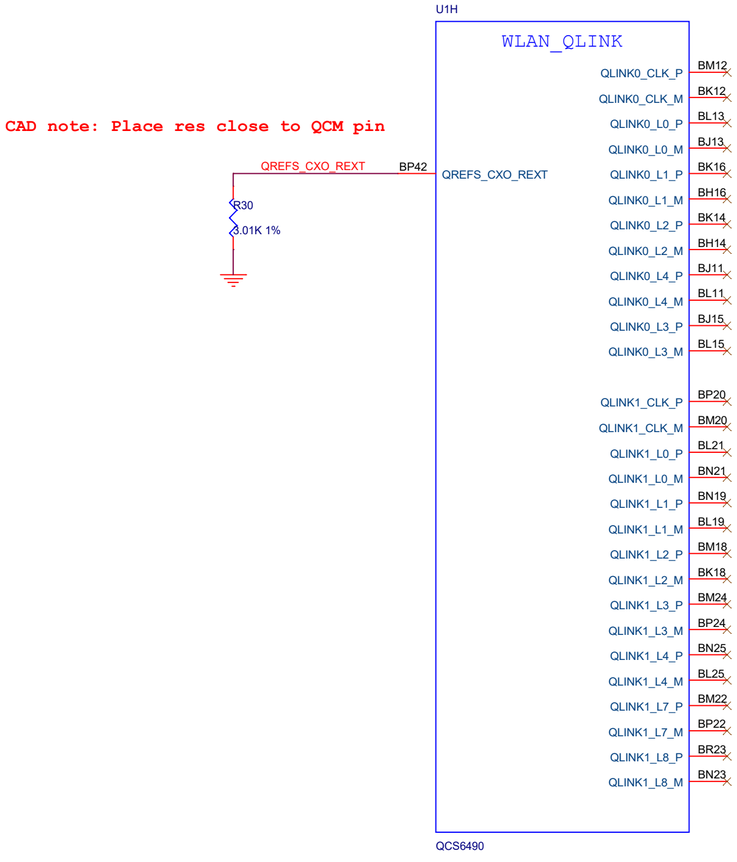
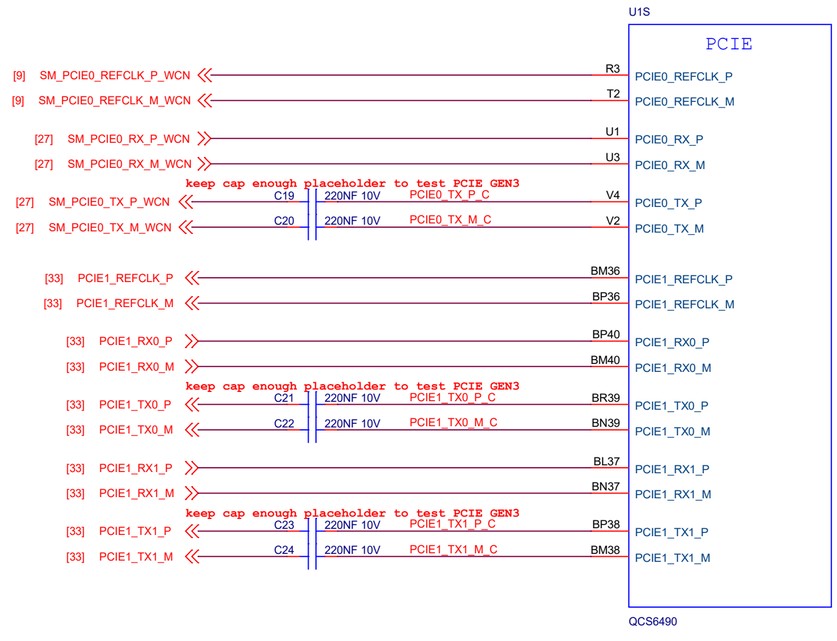
QCM6490 RF/PCIE



	QLINK0	QLINK1
QCS6490	GNSS(SDR735G)	DNC
QCM6490	SDR735	SMR526



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Size	Title:	REV
C	RADXA DRAGON Q5A	
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QCM6490 PWR1

U1I

PWR1

[11,23,24] VREG_S5C_S6C_0P752

[23,24] VSENSE_S5C_S6C_P — Short_L3 — JP1 — VREG_S5C_S6C_0P752:VSENSE_S5C_S6C_P

[23,24] VSENSE_S5C_S6C_M — Short_L3 — JP3 — VSENSE_S5C_S6C_M:GND

C25 10UF 6.3V, C39 22UF 6.3V, C26 10UF 6.3V

C713 22UF 6.3V, C712 22UF 6.3V, C33 4.7UF 6.3V, C34 4.7UF 6.3V, C35 100NF 6.3V, C36 470NF 6.3V, C37 1UF 10V, C38 1UF 10V

C45 4.7UF 6.3V, C46 470NF 6.3V, C47 470NF 6.3V, C48 4.7UF 6.3V

bottom

C53 4.3UF 4V, C54 4.3UF 4V

C826 22UF 6.3V, C827 22UF 6.3V, C714 22UF 6.3V, C715 22UF 6.3V, C716 22UF 6.3V, C717 22UF 6.3V, C718 22UF 6.3V, C719 22UF 6.3V

C371 22UF 6.3V, C411 22UF 6.3V, C412 22UF 6.3V, C413 22UF 6.3V, C414 22UF 6.3V, C415 22UF 6.3V

C4 470NF 6.3V, C5 4.7UF 6.3V, C6 100NF 6.3V, C7 4.7UF 6.3V, C8 100NF 6.3V, C9 100NF 6.3V, C344 470NF 6.3V, C345 100NF 6.3V

C861 470NF 6.3V, C862 100NF 6.3V, C863 4.7UF 6.3V, C864 470NF 6.3V, C865 4.7UF 6.3V, C866 470NF 6.3V, C867 100NF 6.3V, C868 470NF 6.3V, C869 100NF 6.3V, C870 100NF 6.3V

C871 470NF 6.3V, C872 100NF 6.3V, C873 4.7UF 6.3V, C874 470NF 6.3V, C875 4.7UF 6.3V, C876 470NF 6.3V, C877 100NF 6.3V, C878 470NF 6.3V, C879 100NF 6.3V, C880 100NF 6.3V

C881 470NF 6.3V, C882 100NF 6.3V, C883 4.7UF 6.3V, C884 470NF 6.3V, C885 4.7UF 6.3V, C886 470NF 6.3V, C887 100NF 6.3V, C888 470NF 6.3V, C889 100NF 6.3V, C890 100NF 6.3V

C891 470NF 6.3V, C892 100NF 6.3V, C893 4.7UF 6.3V, C894 470NF 6.3V, C895 4.7UF 6.3V, C896 470NF 6.3V

AH14	VDD_MODEM_1	VDD_APC1_1	AA29
AJ11	VDD_MODEM_2	VDD_APC1_2	AA31
AJ13	VDD_MODEM_3	VDD_APC1_3	AA33
AK14	VDD_MODEM_4	VDD_APC1_4	AA35
AL13	VDD_MODEM_5	VDD_APC1_5	AA37
AM14	VDD_MODEM_6	VDD_APC1_6	AA39
AN13	VDD_MODEM_7	VDD_APC1_7	AA41
AN17	VDD_MODEM_8	VDD_APC1_8	AA43
AN19	VDD_MODEM_9	VDD_APC1_9	AD30
AP10	VDD_MODEM_10	VDD_APC1_10	AD32
AP14	VDD_MODEM_11	VDD_APC1_11	AD34
AP18	VDD_MODEM_12	VDD_APC1_12	AD36
AR9	VDD_MODEM_13	VDD_APC1_13	AD38
AR13	VDD_MODEM_14	VDD_APC1_14	AE29
AR17	VDD_MODEM_15	VDD_APC1_15	AE31
AR21	VDD_MODEM_16	VDD_APC1_16	AE35
AT10	VDD_MODEM_17	VDD_APC1_17	AE37
AT14	VDD_MODEM_18	VDD_APC1_18	M38
AT18	VDD_MODEM_19	VDD_APC1_19	M42
AT22	VDD_MODEM_20	VDD_APC1_20	N39
AU13	VDD_MODEM_21	VDD_APC1_21	N41
AU17	VDD_MODEM_22	VDD_APC1_22	N43
AU21	VDD_MODEM_23	VDD_APC1_23	P40
AV10	VDD_MODEM_24	VDD_APC1_24	R39
AV14	VDD_MODEM_25	VDD_APC1_25	T40
AV18	VDD_MODEM_26	VDD_APC1_26	U39
AV22	VDD_MODEM_27	VDD_APC1_27	V40
AW13	VDD_MODEM_28	VDD_APC1_28	W39
AW17	VDD_MODEM_29	VDD_APC1_29	Y28
AW21	VDD_MODEM_30	VDD_APC1_30	Y30
AY10	VDD_MODEM_31	VDD_APC1_31	Y32
AY14	VDD_MODEM_32	VDD_APC1_32	Y34
AY18	VDD_MODEM_33	VDD_APC1_33	Y38
AY22	VDD_MODEM_34	VDD_APC1_34	Y40
BA13	VDD_MODEM_35	VDD_APC1_35	Y42
BA17	VDD_MODEM_36		
BA21	VDD_MODEM_37	VDD_APC0_1	M36
BB10	VDD_MODEM_38	VDD_APC0_2	N35
BB14	VDD_MODEM_39	VDD_APC0_3	P36
BB18	VDD_MODEM_40	VDD_APC0_4	R35
BB22	VDD_MODEM_41	VDD_APC0_5	T36
BC17	VDD_MODEM_42	VDD_APC0_6	U29
BD18	VDD_MODEM_43	VDD_APC0_7	U31
BE17	VDD_MODEM_44	VDD_APC0_8	U33
BF18	VDD_MODEM_45	VDD_APC0_9	U35
		VDD_APC0_10	V32
		VDD_APC0_11	V34
		VDD_APC0_12	V36

QCS6490

VREG_S3B_S4B_S5B_0P752 [11,19,20]

JP2 — VSENSE_S3B_S4B_S5B_P:VREG_S3B_S4B_S5B_0P752 — Short_L6 — VSENSE_S3B_S4B_S5B_P [19,20]

C27 10UF 6.3V, C28 10UF 6.3V, C29 22UF 6.3V, C30 22UF 6.3V, C31 22UF 6.3V, C32 22UF 6.3V

JP4 — VSENSE_S3B_S4B_S5B_M:GND — Short_L6 — VSENSE_S3B_S4B_S5B_M [19,20]

C41 1UF 10V, C42 470NF 6.3V, C43 4.7UF 6.3V, C44 1UF 10V, C40 1UF 10V, C808 100NF 6.3V, C807 100NF 6.3V, C810 4.7UF 6.3V, C809 470NF 6.3V

C49 1UF 10V, C50 470NF 6.3V, C51 470NF 6.3V, C52 100NF 6.3V

C55 4.3UF 4V, C56 4.3UF 4V

bottom

C750 10UF 6.3V, C751 10UF 6.3V, C752 10UF 6.3V, C753 10UF 6.3V, C754 10UF 6.3V, C755 10UF 6.3V, C756 22UF 6.3V, C757 10UF 6.3V, C802 4.7UF 6.3V, C801 4.7UF 6.3V, C804 470NF 6.3V, C803 470NF 6.3V, C806 100NF 6.3V, C805 100NF 6.3V

C834 4.7UF 6.3V, C835 4.7UF 6.3V, C836 470NF 6.3V, C837 470NF 6.3V, C838 100NF 6.3V

VREG_S6B_0P752 [11,20]

JP5 — VSENSE_S6B_P:VREG_S6B_0P752 — Short_L7 — VSENSE_S6B_P [20]

C57 10UF 6.3V, C58 10UF 6.3V, C59 10UF 6.3V

JP6 — VSENSE_S6B_M:GND — Short_L7 — VSENSE_S6B_M [20]

C60 2.2UF 6.3V, C61 470NF 6.3V, C62 470NF 6.3V, C63 4.7UF 6.3V, C64 470NF 6.3V, C65 470NF 6.3V, C66 100NF 6.3V, C67 470NF 6.3V, C68 4.7UF 6.3V, C69 470NF 6.3V, C70 100NF 6.3V, C71 4.7UF 6.3V, C72 470NF 6.3V, C73 470NF 6.3V

C74 4.3UF 4V, C75 4.3UF 4V

bottom

C740 4.7UF 6.3V, C741 4.7UF 6.3V, C742 4.7UF 6.3V, C743 4.7UF 6.3V

radxa

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QCM6490 PWR2

U1J

PWR2

[17,18,22,36] VREG_SYS_1P8 — R37 0R 1%(NC) 2P0201R

[6,11,15,16,17,21,26,30,35] VREG_L18B_1P8 — R38 0R 1%(NC)

[15,24] VREG_S9C_1P084

[16,25] VREG_L6C_2P96 — R39 0R 1%

install R1201 and DNI R1202 when use SDIO.

DDR SDC2

C76 1UF 10V, C77 1UF 10V, C78 1UF 10V

AE41 VDD_PX0
L25 VDD_PX1
AT40 VDD_PX2

IO

[6,11,15,16,17,21,26,30,35] VREG_L18B_1P8

C85 100NF 16V, C86 100NF 16V, C87 1UF 10V, C88 1UF 10V

AC41 VDD_PX3_1
AF8 VDD_PX3_2
AW25 VDD_PX3_3
BG7 VDD_PX3_4
BH40 VDD_PX3_5
P6 VDD_PX3_6

UIM1
UIM2
eMMC
UFS
CXO

[25] VREG_L4C_1P8_3P0
[25] VREG_L5C_1P8_3P0
[6,11,15,16,17,21,26,30,35] VREG_L18B_1P8
[16,21] VREG_L9B_1P2
[17] VREG_BB_1P2

C101 1UF 10V, C102 1UF 10V, C103 1UF 10V, C104 1UF 10V, C105 1UF 10V

BE37 VDD_PX5
BE39 VDD_PX6
M6 VDD_PX7
L23 VDD_PX10
BE35 VDD_PX11

TP1 0.5mm — VDD_GFX_CS_ISENSE — AK30 VDD_GFX_CX_ISENSE

[13,18] VREF_MSM_1P25 — C106 100NF 16V

AV40 VDDPX_VBIAS_SDC
BH36 VDDPX_VBIAS_UIM

QCS6490

VDD_GFX_1 AN37
VDD_GFX_2 AN39
VDD_GFX_3 AP28
VDD_GFX_4 AP32
VDD_GFX_5 AP36
VDD_GFX_6 AR29
VDD_GFX_7 AR33
VDD_GFX_8 AR37
VDD_GFX_9 AT28
VDD_GFX_10 AT32
VDD_GFX_11 AT36
VDD_GFX_12 AU29
VDD_GFX_13 AU33
VDD_GFX_14 AU37
VDD_GFX_15 AV28
VDD_GFX_16 AV32
VDD_GFX_17 AV36
VDD_GFX_18 AW29
VDD_GFX_19 AW33
VDD_GFX_20 AW37
VDD_GFX_21 AY28
VDD_GFX_22 AY32
VDD_GFX_23 AY36
VDD_GFX_24 AY40
VDD_GFX_25 BA29
VDD_GFX_26 BA33
VDD_GFX_27 BA37
VDD_GFX_28 BB40

VREG_S7C_S8C_0P676 [11,24]

JP7 Short_L3 — VREG_S7C_S8C_0P676:VSENSE_S7C_S8C_P — VSENSE_S7C_S8C_P [24]

JP8 Short_L3 — RTM_VREG_S3A_S4A_M:GND — VSENSE_S7C_S8C_M [24]

C79 10UF 6.3V, C80 10UF 6.3V, C81 10UF 6.3V, C82 10UF 6.3V, C83 10UF 6.3V, C84 10UF 6.3V

C89 100NF 6.3V, C90 4.7UF 6.3V, C91 1UF 10V, C92 2.2UF 6.3V, C93 2.2UF 6.3V, C94 4.7UF 6.3V

C95 4.7UF 6.3V, C96 100NF 16V, C97 470NF 6.3V

C98 470NF 6.3V, C99 470NF 6.3V, C100 470NF 6.3V

C720 10UF 6.3V, C721 10UF 6.3V, C722 10UF 6.3V, C723 10UF 6.3V, C724 10UF 6.3V, C725 10UF 6.3V

C786 100NF 6.3V, C785 100NF 6.3V, C788 100NF 6.3V, C787 470NF 6.3V, C790 470NF 6.3V, C789 470NF 6.3V

C897 22UF 6.3V, C898 22UF 6.3V, C899 22UF 6.3V, C900 22UF 6.3V, C901 22UF 6.3V, C902 22UF 6.3V, C903 22UF 6.3V, C904 22UF 6.3V, C905 22UF 6.3V

C906 470NF 6.3V, C907 100NF 6.3V, C908 4.7UF 6.3V, C909 470NF 6.3V, C910 4.7UF 6.3V, C911 470NF 6.3V, C912 100NF 6.3V, C913 470NF 6.3V, C914 100NF 6.3V, C915 100NF 6.3V

C916 470NF 6.3V, C917 100NF 6.3V, C918 4.7UF 6.3V, C919 470NF 6.3V, C920 4.7UF 6.3V

U1M

PWR5

[10,20] VREG_S6B_0P752 — C792 470NF 6.3V, C791 100NF 6.3V, C828 470NF 6.3V, C829 470NF 6.3V, C830 470NF 6.3V, C831 470NF 6.3V, C832 470NF 6.3V, C833 470NF 6.3V

V30 VDD_APC0_13
W29 GND_X_1

[10,19,20] VREG_S3B_S4B_S5B_0P752
AE33 VDD_APC1_36
AF32 GND_X_2

L11 GND_X_3

[12,13,23] VREG_S2C_S3C_S4C_0P676
M10 VDD_CX_81

[11,24] VREG_S7C_S8C_0P676
BC39 VDD_GFX_29
BD38 GND_X_4

[12,24] VREG_S10C_0P752 — C784 100NF 6.3V, C783 470NF 6.3V, C781 4.7UF 6.3V, C780 470NF 6.3V, C782 100NF 6.3V, C708 4.7UF 6.3V, C706 4.7UF 6.3V, C707 100NF 6.3V

AV26 VDD_MX_38

[10,23,24] VREG_S5C_S6C_0P752
BC9 VDD_MODEM_46
BB8 GND_X_5

[13,21] VREG_L5B_0P752 — C710 2.2UF 6.3V, C711 1UF 10V
AG39 VDD_LPI_CX_6
AJ37 GND_X_6

QCS6490

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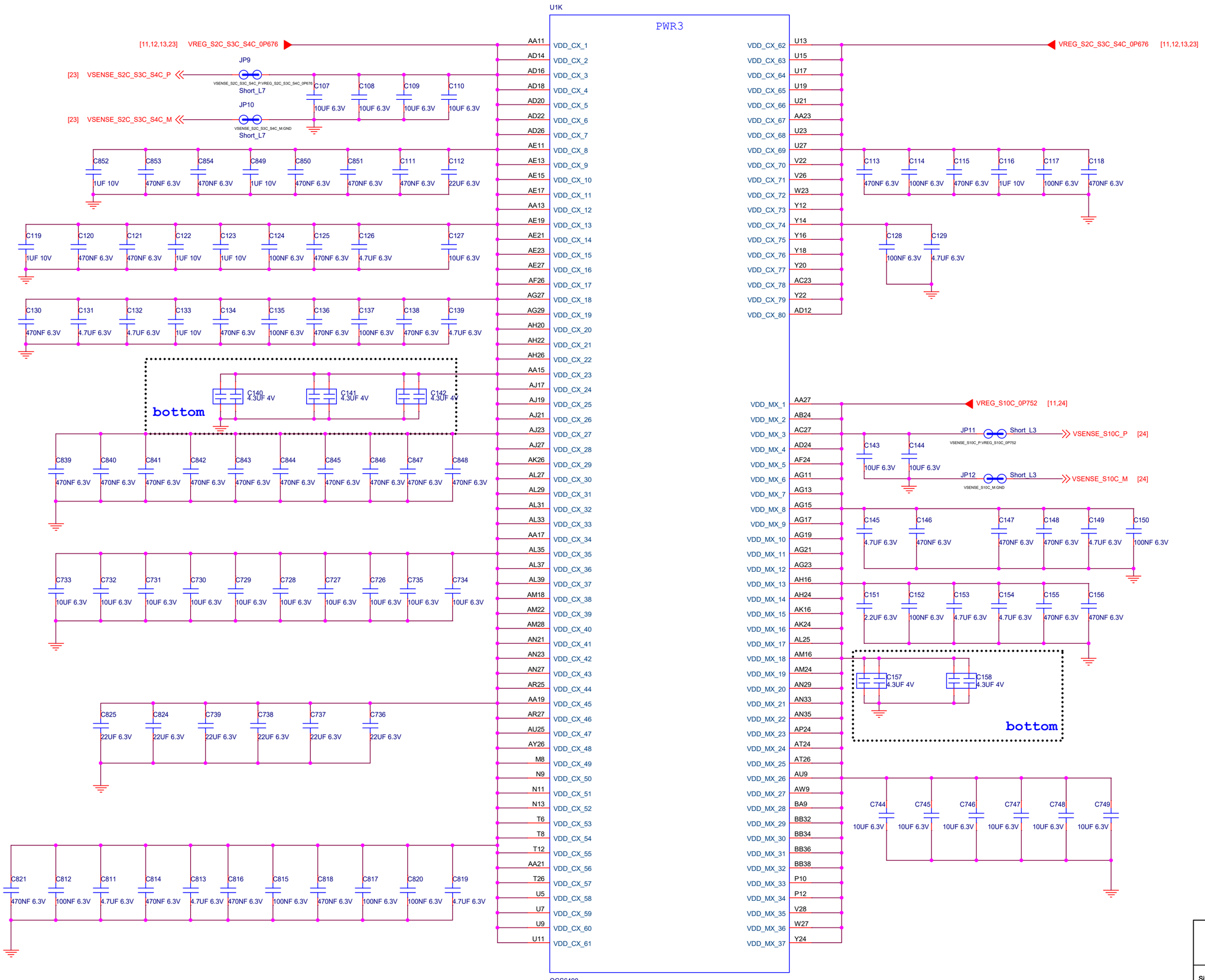
QCM6490 PWR3



Size C	Title: RADXA DRAGON Q5A	REV X1.0
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QCM6490 PWR4

U1L

PWR4

bottom

[11,21] VREG_L5B_0P752
C778 100NF 6.3V
C777 220NF 6.3V
C779 470NF 6.3V
C159 4.3UF 4V
C160 1UF 10V
C161 4.7UF 6.3V
C162 4.7UF 10V
AE39 VDD_LPI_CX_1
AG33 VDD_LPI_CX_2
AG35 VDD_LPI_CX_3
AG37 VDD_LPI_CX_4
AH38 VDD_LPI_CX_5

[13,21] VREG_L6B_1P2
Y8 VDD_A_PCIE_0_1P2
BC31 VDD_A_PCIE_1_1P2

[13,25] VREG_L10C_0P88
AA9 VDD_A_PCIE_0_CORE
BC33 VDD_A_PCIE_1_CORE
C166 1UF 10V
C167 1UF 10V
C168 1UF 10V
C169 1UF 10V

[19,21] VREG_S2B_0P7
N15 VDD_A_EBI0_1
N17 VDD_A_EBI0_2
N19 VDD_A_EBI0_3
N21 VDD_A_EBI0_4

[19] VSENSE_S2B_P
JP13 Short_L7
VSENSE_S2B_P:VREG_S2B_0P7
[19] VSENSE_S2B_M
JP14 Short_L7
VSENSE_S2B_M:GND
C179 10UF 6.3V
C180 10UF 6.3V

N27 VDD_A_EBI1_1
N29 VDD_A_EBI1_2
N31 VDD_A_EBI1_3
N33 VDD_A_EBI1_4
C181 470NF 6.3V
C182 100NF 6.3V
C183 470NF 6.3V
C184 100NF 6.3V
C185 1UF 10V
C186 1UF 10V
C187 4.7UF 6.3V
C188 4.7UF 6.3V
C189 100NF 6.3V
C709 1UF 10V

L17 VDD_A_PLL_EBI0
L29 VDD_A_PLL_EBI1

[13,25] VREG_L10C_0P88
[13,21] VREG_L6B_1P2
AM40 VDD_VREF_0P9
AN41 VDD_VREF_1P2
C196 1UF 10V
C197 1UF 10V

AL9 VDD_A_CSI_01_0P9
AM8 VDD_A_CSI_01_1P2
[13,25] VREG_L10C_0P88
[13,21] VREG_L6B_1P2
AJ9 VDD_A_CSI_23_0P9
AH8 VDD_A_CSI_23_1P2
C202 1UF 10V
C203 1UF 10V
C204 1UF 10V
C205 1UF 10V
C206 1UF 10V
C207 1UF 10V

AC9 VDD_A_CSI_4_0P9
AD8 VDD_A_CSI_4_1P2

[13,25] VREG_L1C_1P8
Y36 VDD_A_APC_CS_1P8
C208 1UF 10V

[13,25] VREG_L10C_0P88
[13,21] VREG_L6B_1P2
AJ41 VDD_A_DSI_0_0P9
AG41 VDD_A_DSI_0_1P2
AH40 VDD_A_DSI_0_PLL_0P9
C211 1UF 10V
C212 1UF 10V
C213 1UF 10V
C214 100NF 16V

[13,25] VREG_L10C_0P88
C220 1UF 10V
C221 100NF 16V
C222 100NF 16V

BD34 VDD_A_QREFS_0P875_1
BE41 VDD_A_QREFS_0P875_2
AL41 VDD_A_QREFS_0P875_3
T42 VDD_A_QREFS_0P875_4
T24 VDD_A_QREFS_0P875_5
BC23 VDD_A_QREFS_0P875_6
BE13 VDD_A_QREFS_0P875_7
AN9 VDD_A_QREFS_0P875_8
Y10 VDD_A_QREFS_0P875_9

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VDD_A_QLINK_0_0P9 BC15
VDD_A_QLINK_1_0P9 BD20
VDD_A_QLINK_0_0P9_CK BD14
VDD_A_QLINK_1_0P9_CK BC21
C163 1UF 10V
C164 1UF 10V
C165 1UF 10V
C170 1UF 10V
[13,25] VREG_L10C_0P88
[13,25] VREG_L10C_0P88
C770 10UF 6.3V
C771 10UF 6.3V
C772 10UF 6.3V
C773 10UF 6.3V
[13,21] VREG_L1B_0P912

VDD_A_UFS_0_CORE P24
VDD_A_UFS_0_1P2 P22
[13,25] VREG_L10C_0P88
[13,21] VREG_L6B_1P2

VDD_A_USBSSDP_0_1P2 BC29
VDD_A_USBSSDP_0_CORE BD28
[13,21] VREG_L6B_1P2
[13,21] VREG_L1B_0P912

VDD_A_USBHS_1P8 BE25
VDD_A_USBHS_3P1 BF26
VDD_A_USBHS_CORE BD24
[13,25] VREG_L1C_1P8
[21,37] VREG_L2B_3P072
[13,25] VREG_L10C_0P88
C171 1UF 10V
C172 1UF 10V
C173 1UF 10V
C174 1UF 10V
C409 1UF 10V
C410 1UF 10V
C175 1UF 10V
C176 1UF 10V
C177 1UF 10V
C178 1UF 10V

VDD_A_CXO_1P8 BH38
[13,25] VREG_L1C_1P8

VDD_A_GNSS_0P9 BB24
[13,25] VREG_L10C_0P88
VDD_QFPROM AY24
[13,25] VREG_L1C_1P8
VDD_WPSS_CX AB26
[11,12,13,23] VREG_S2C_S3C_S4C_0P676
VDD_A_GFX_CS_1P8 AM30
[13,25] VREG_L1C_1P8
VDD_A_TURING_Q6_CS_1P8 W13
[13,25] VREG_L1C_1P8
C190 1UF 10V
C191 1UF 10V
C192 1UF 10V
C193 1UF 10V
C194 100NF 16V
C195 1UF 10V

VDD_IO_EBI0_1 P14
VDD_IO_EBI0_2 P16
VDD_IO_EBI0_3 P18
VDD_IO_EBI0_4 P20
VDD_IO_EBI1_1 P26
VDD_IO_EBI1_2 P28
VDD_IO_EBI1_3 P30
VDD_IO_EBI1_4 P32
C198 1UF 10V
C199 1UF 10V
C200 470NF 6.3V
C201 1UF 10V
[7,15,21] VREG_L3B_0P504
C766 10UF 6.3V
C767 10UF 6.3V
C768 10UF 6.3V
C769 10UF 6.3V

VDD_D_EBI0 R17
VDD_D_EBI1 R29
C209 470NF 6.3V
[11,12,13,23] VREG_S2C_S3C_S4C_0P676
C210 4.3UF 4V

VDD_LPI_NAV_MX BC25
VDD_LPI_MX_1 AG31
VDD_LPI_MX_2 AH30
VDD_LPI_MX_3 AH32
VDD_LPI_MX_4 AH34
VDD_LPI_MX_5 AH36
C215 1UF 10V
C216 1UF 10V
C217 470NF 6.3V
C218 470NF 6.3V
C219 4.3UF 4V
[13,21] VREG_L4B_0P752
C762 10UF 6.3V
C763 10UF 6.3V
C764 10UF 6.3V
C765 10UF 6.3V

VDD_A_QLINK_0_1P2_CK BC13
VDD_A_QLINK_1_1P2 BC19
[13,21] VREG_L6B_1P2
C223 1UF 10V
C224 470NF 6.3V

VDD_A_QREFS_1P25 BH34
[11,18] VREF_MSM_1P25
VDD_A_QREFS_1P8 BJ37
[13,25] VREG_L1C_1P8
C225 100NF 16V
C226 100NF 16V
[13,21] VREG_L4B_0P752
C775 100NF 16V
C774 220NF 16V
C776 4.7UF 6.3V
C822 22UF 6.3V
C823 22UF 6.3V

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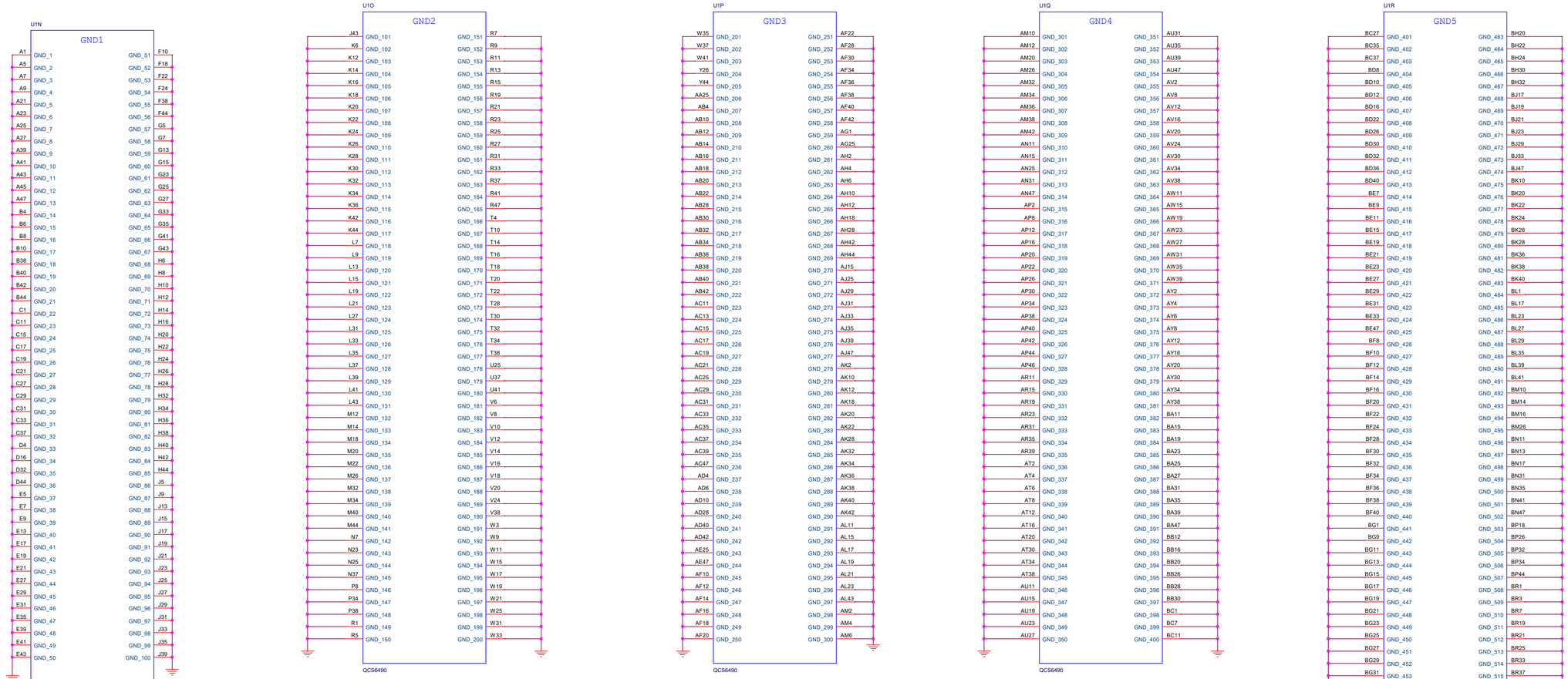
QCM6490 GND



Size	Title: RADXA DRAGON Q5A		REV X1.0
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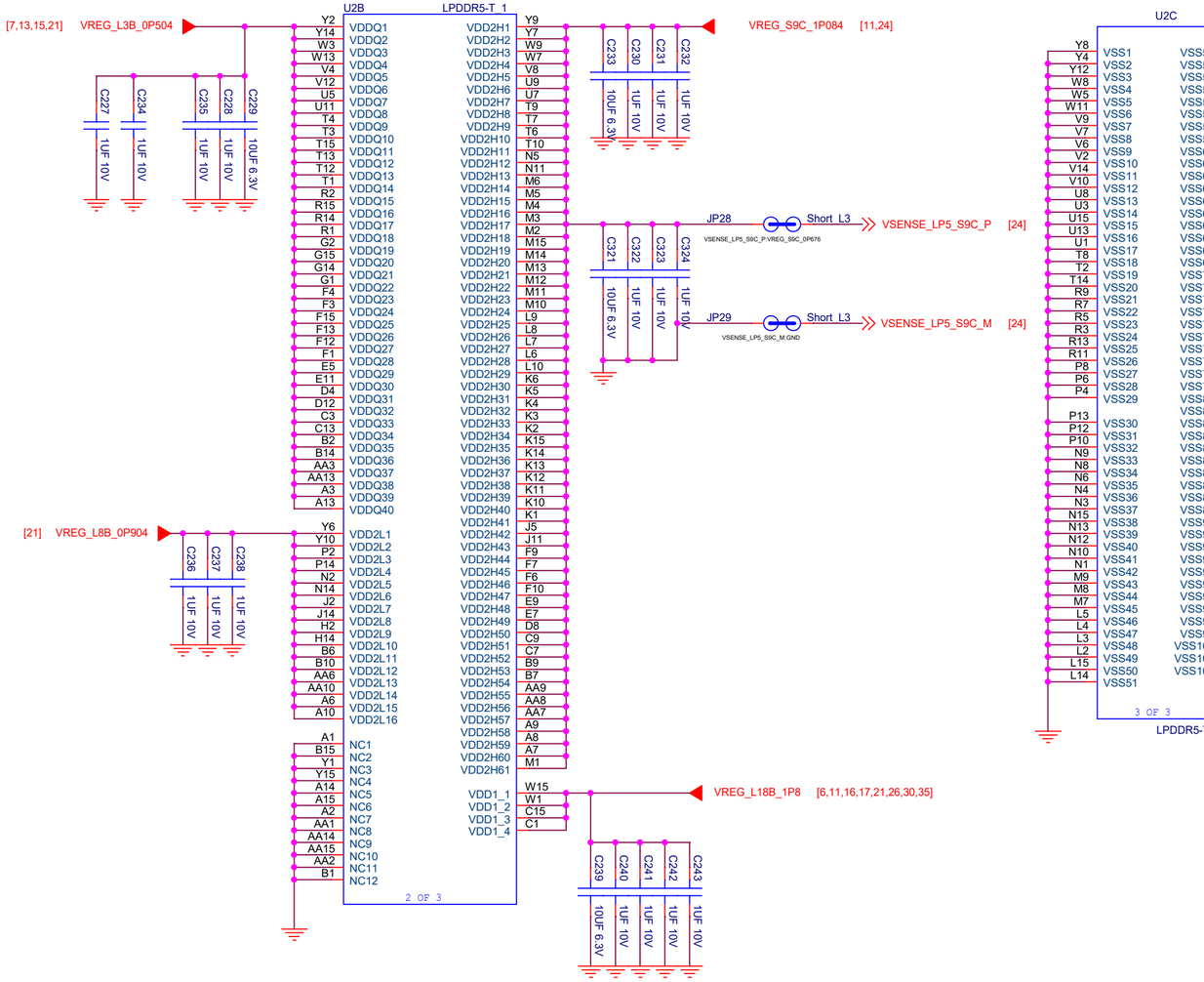
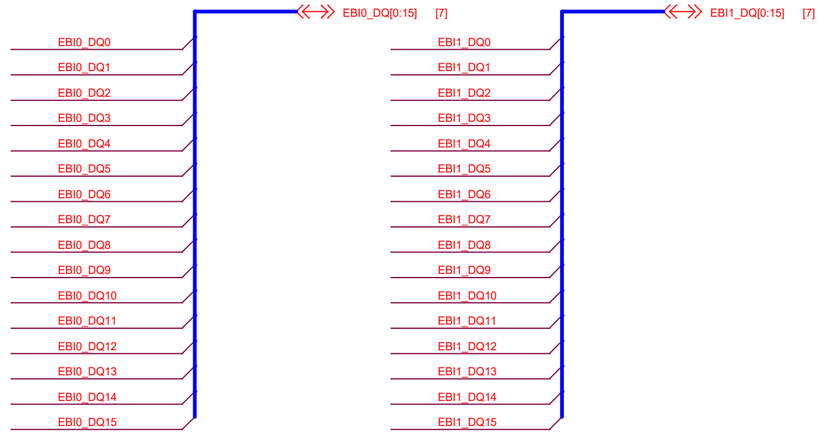
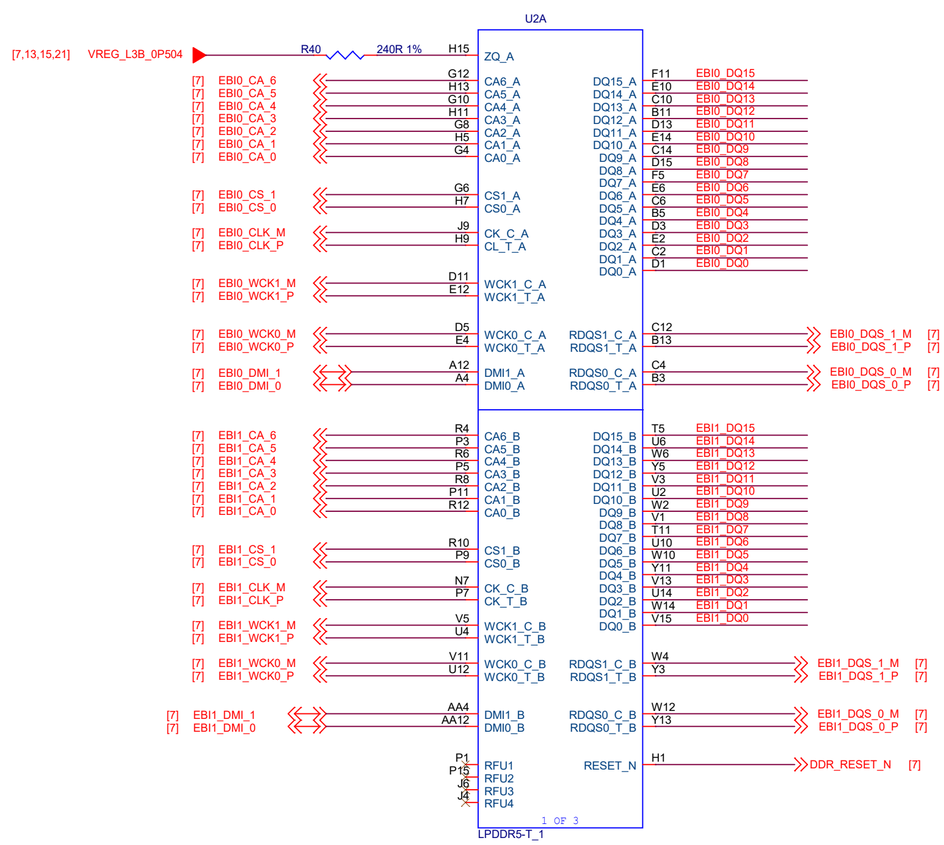
LPDDR5







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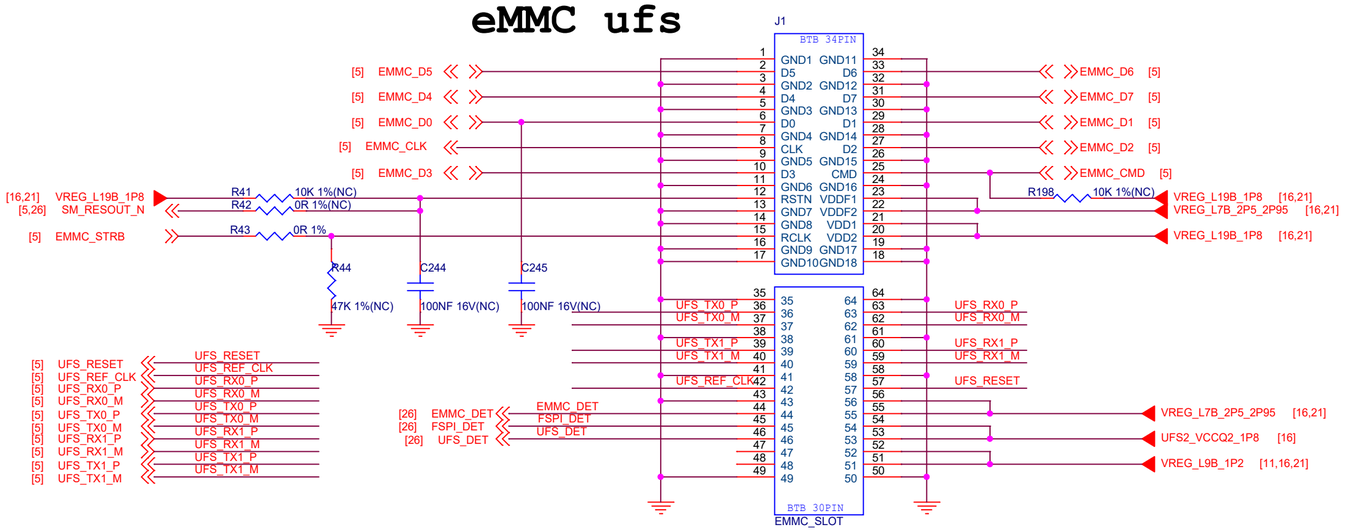
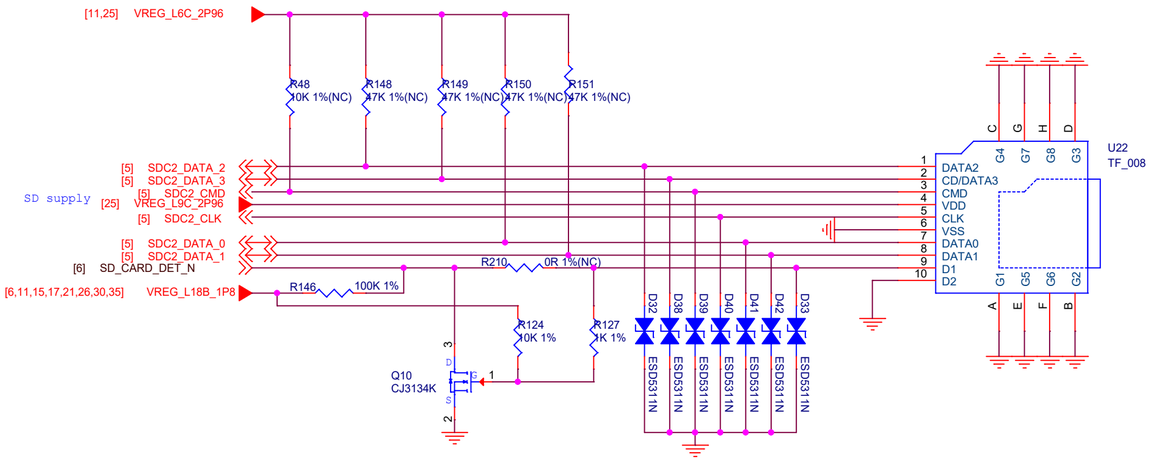
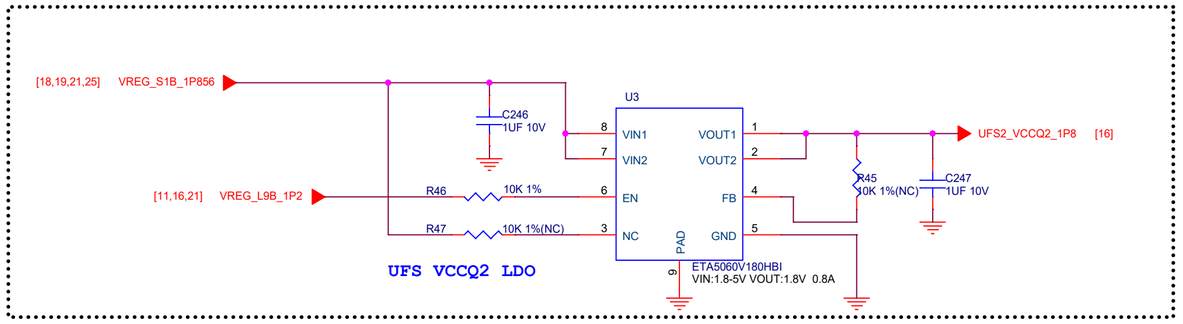
EMMC&UFS

eMMC ufs



Place near to the UFS about 1cm and put ino the shielding





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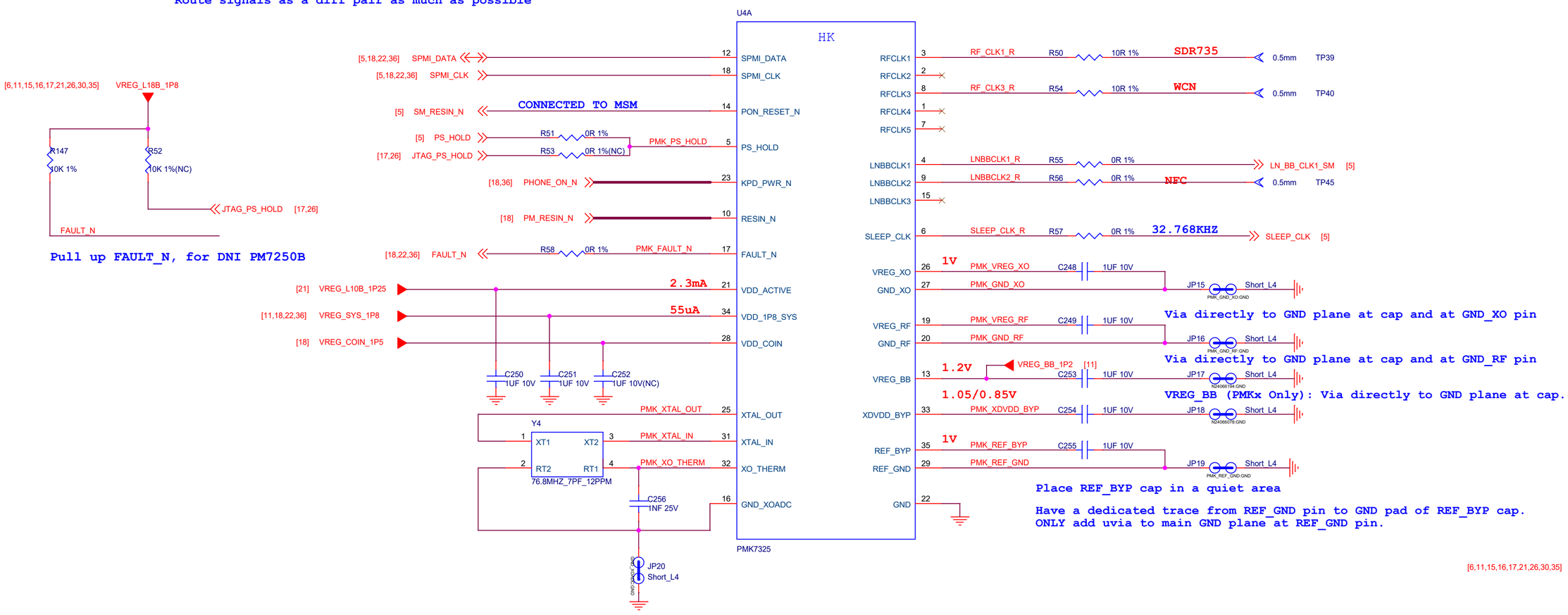
PMK7325

Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible



[6,11,15,16,17,21,26,30,35] VREG_L18B_1P8

R147 10K 1%

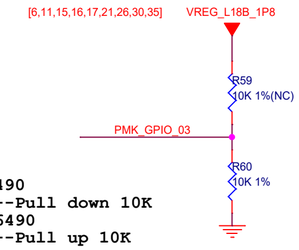
R52 10K 1%(NC)

JTAG_PS_HOLD [17,26]

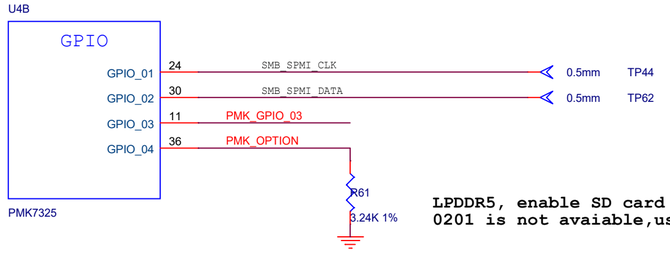
FAULT_N

Pull up FAULT_N, for DNI PM7250B

Layout Note: XTAL
No trace shall be present in at-least two immediate layers below XTAL.
Route XTAL IN/OUT trace with length between 3mm and 10mm



C6490
--Pull down 10K
CT6490
--Pull up 10K



LPDDR5, enable SD card LDO
0201 is not avaiable,use 0402 as alternative

Note:
GPIO_03 is required for easy debug of PMIC faults,
the TP placement on board should be in such a way that it is easily accessible for probe

PMK_OPTION	Configuration
3.24k	LPDDR5, SD card LDO enabled
10.2k	LPDDR5, Skip SD card LDO enable
-	- (Reserved)
113k	LPDDR4x, SD card LDO enabled
147k	LPDDR4x, Skip SD card LDO enable
-	- (Reserved)

Note:
SD card boot implies the voltages for SD card will be enabled during power on sequence.
No SD card boot implies the voltages for SD card will be skipped during power on sequence.

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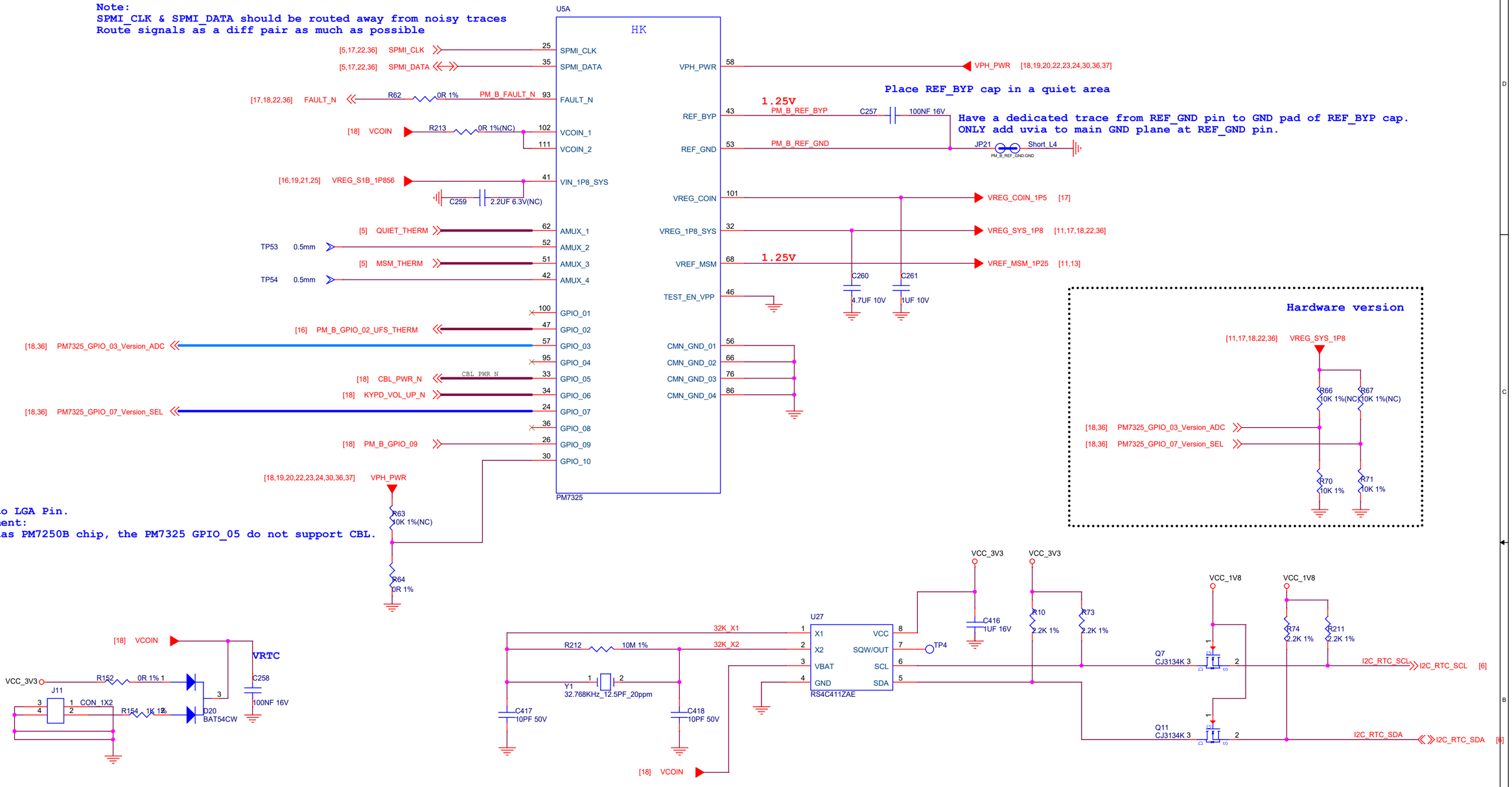
PM7325 CTRL GPIO GND

Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible

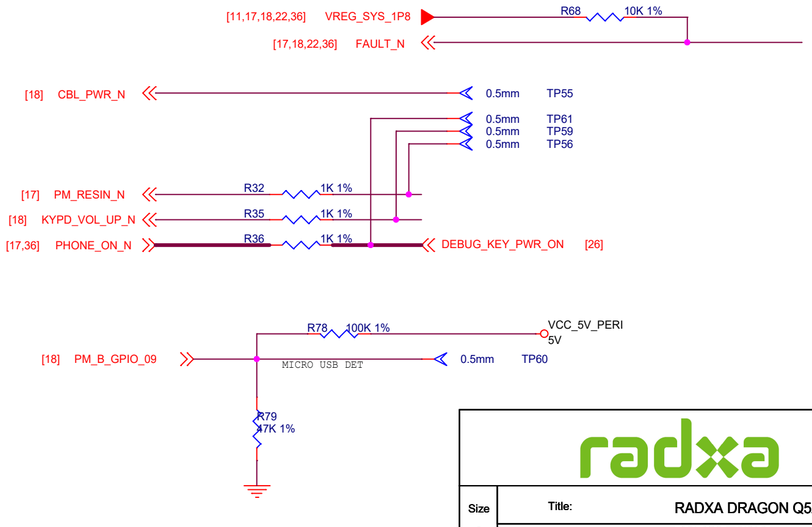


NOTE: CBL
delete CBL net to LGA Pin.
Qualcomm CE comment:
If your device has PM7250B chip, the PM7325 GPIO_05 do not support CBL.

NOTE:
MV: VPH_PWR or 1.8 V
LV : 1.8 V only

GPIO_10(OPT)	Configuration
GND	SM7325
Hi-Z	(Reserved)
VPH_PWR	(Reserved)

GPIO	Type	Configuration	Special function for QCM6490
1	LV	AMUX	PA_THERM1
2	LV	AMUX	
3	LV	AMUX	
4	LV	AMUX	PA_THERM2
5	MV	AMUX	(CBL_PWR_N)
6	MV		KYPD_VOL_UP_N
7	MV		
8	MV		USB1_HOST_EN_SW
9	MV		USB1_VBUS_DET
10	MV		PM7325_OPTION



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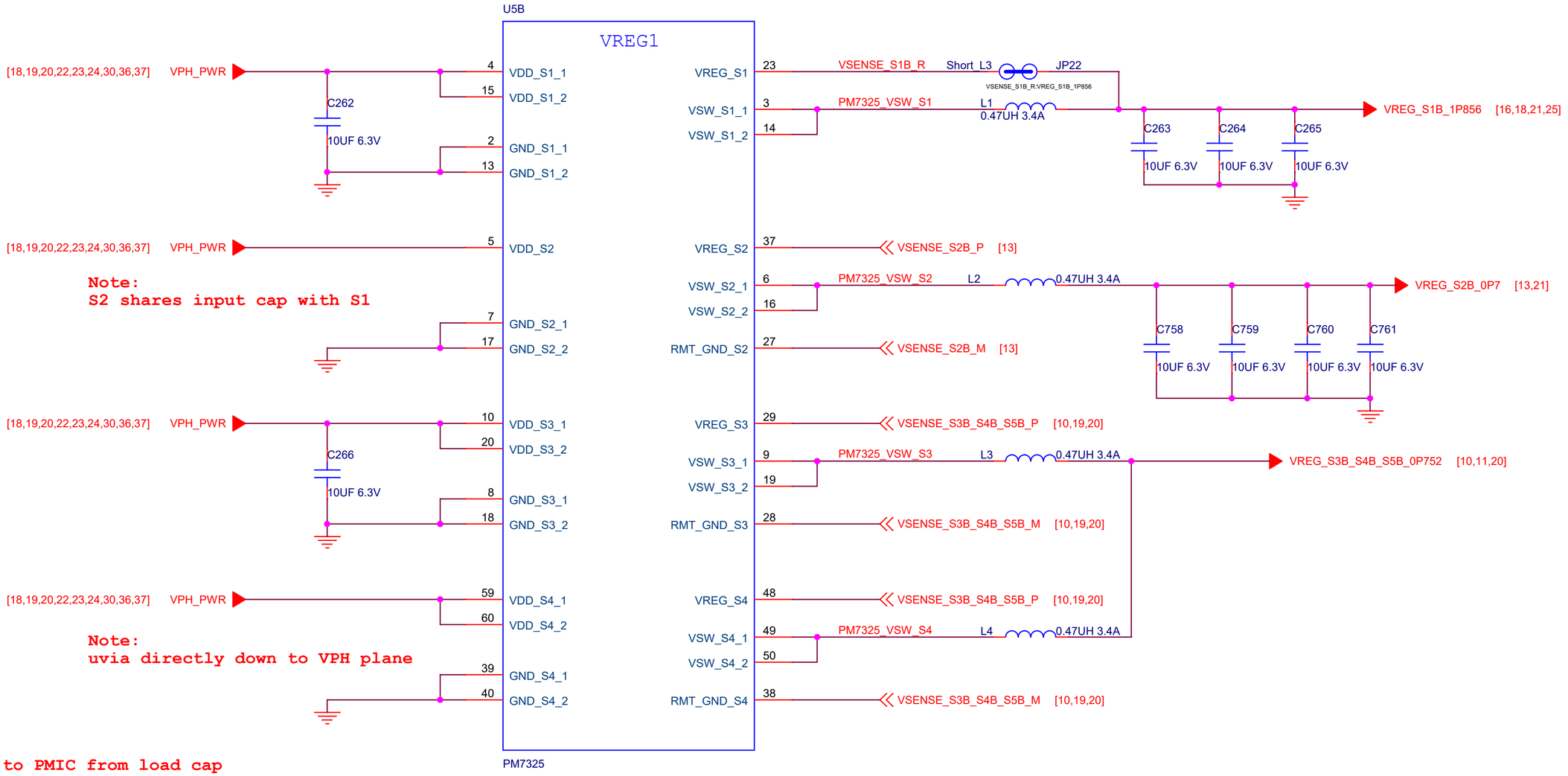
PM7325 BUCKS 1 OF 2

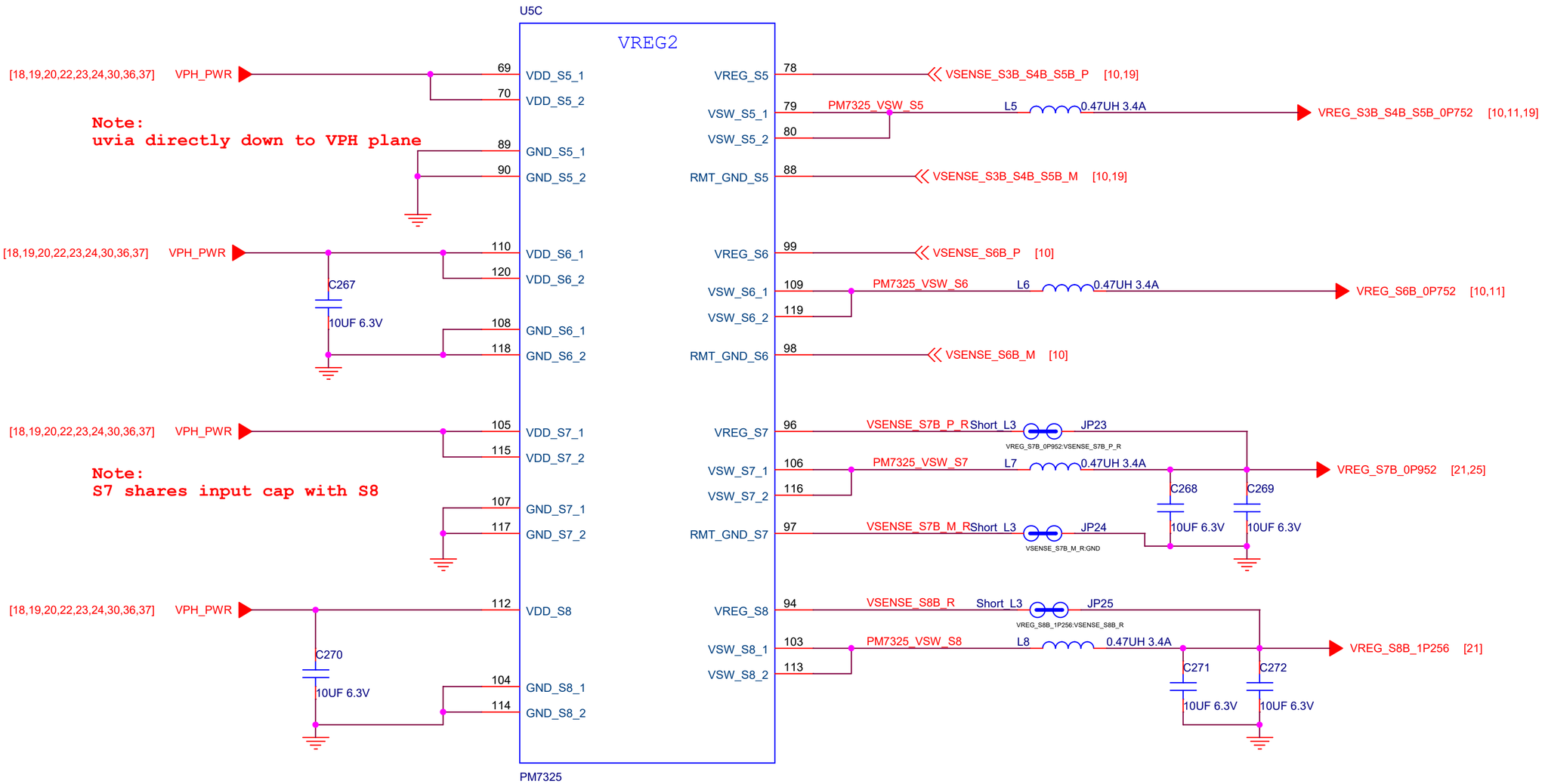


Note:
RMT P/M Diff Pair back to PMIC from load cap

Regulator	type	IRATED (A)	voltage	use
S1B	HFS510	3500	1.856	HV sub regulation
S2B	FTS520	2500	0.876	EBI
S3B_S4B_S5B	FTS520	13500	0.752	APC1
S6B	FTS520	4500	0.752	APC0
S7B	FTS520	4500	0.952	LV sub regulation
S8B	HFS510	4000	1.256	MV sub regulation

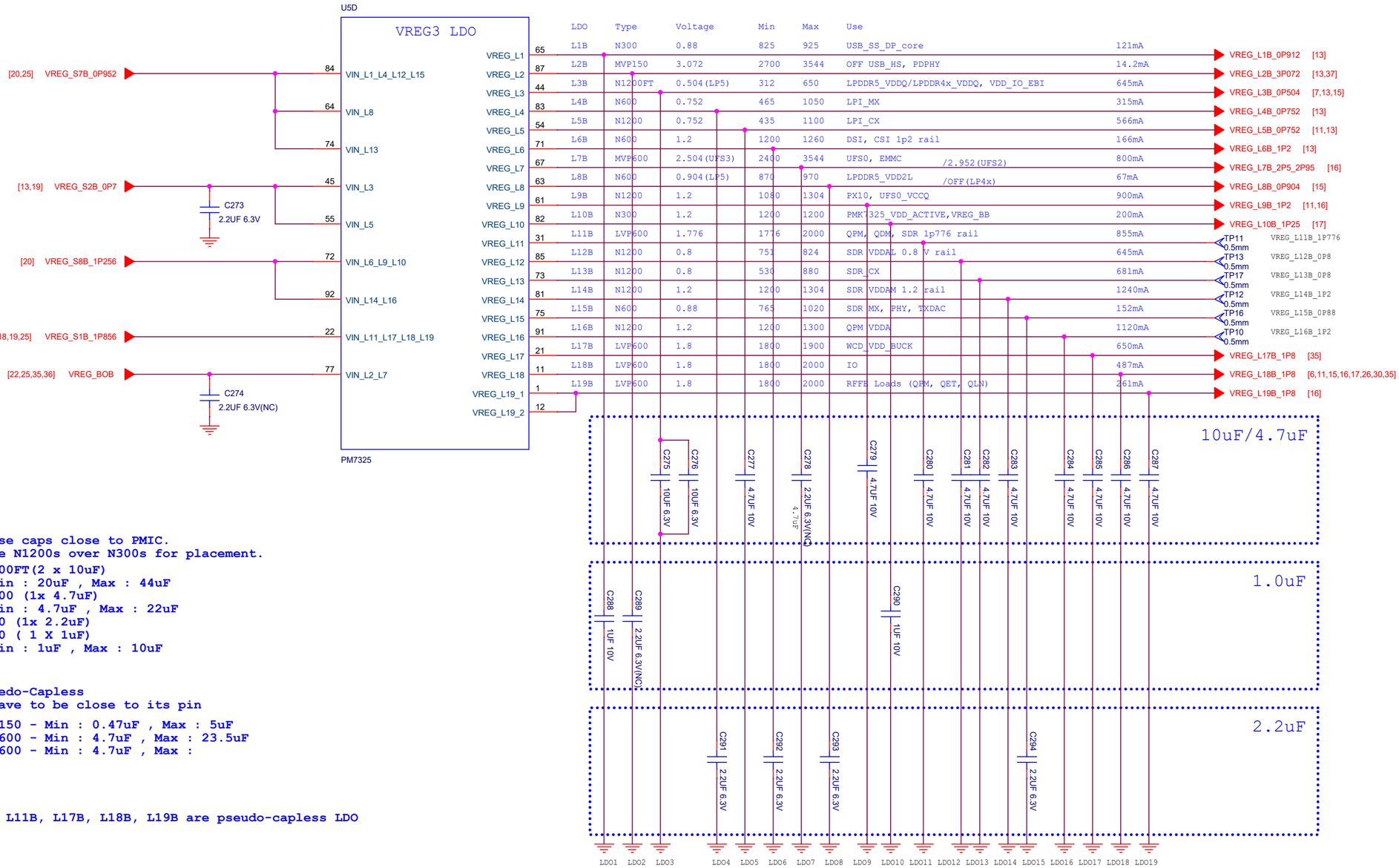
Size: Custom	Title: RADXA DRAGON Q5A	REV: X1.0
	Page Name: PM7325_Bucks_S1-S4	
Date: Friday, June 20, 2025	Sheet 19 of 37	

PM7325 BUCKS 2 OF 2



Size	Title:	RADXA DRAGON Q5A	REV
Custom	Page Name:	PM7325_Bucks_S5-S8	X1.0
Date:	Friday, June 20, 2025	Sheet 20 of 37	

PM7325 LDOs



NOTE:
Place these caps close to PMIC.
Prioritize N1200s over N300s for placement.

- **N1200FT(2 x 10uF)**
  - **--Min : 20uF , Max : 44uF**
- **N1200 (1x 4.7uF)**
  - **--Min : 4.7uF , Max : 22uF**
- **N600 (1x 2.2uF)**
- **N300 (1 X 1uF)**
  - **--Min : 1uF , Max : 10uF**

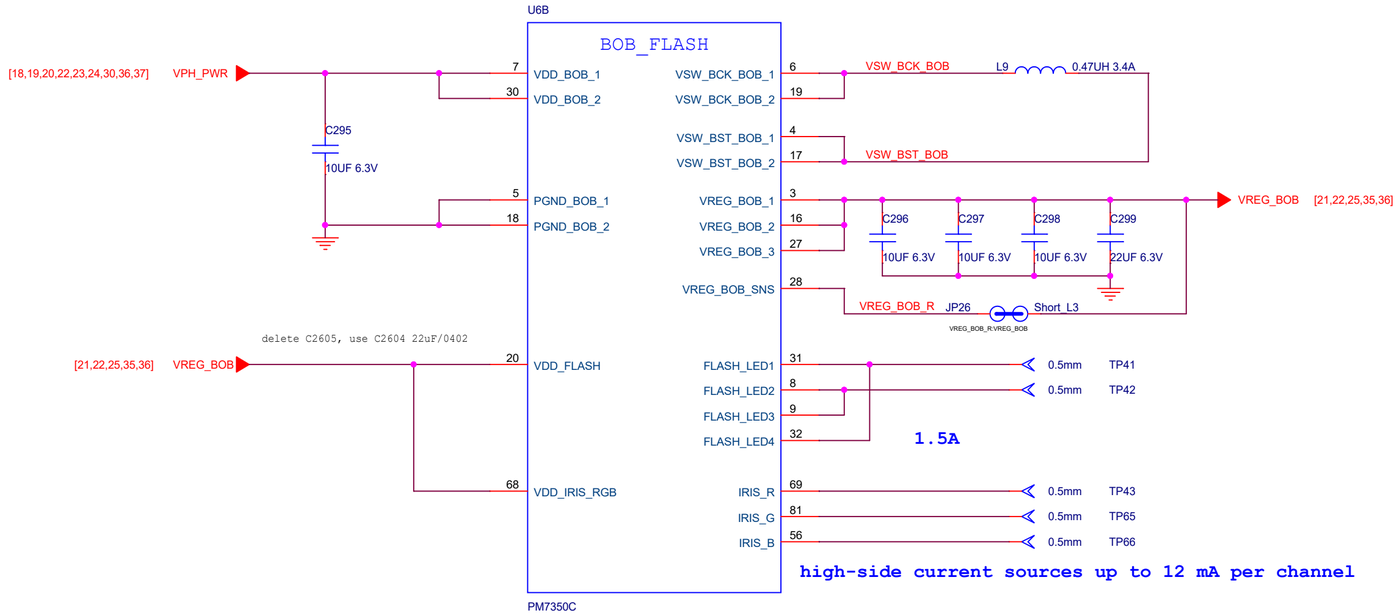
NOTE: Psuedo-Capless
Doesn't have to be close to its pin

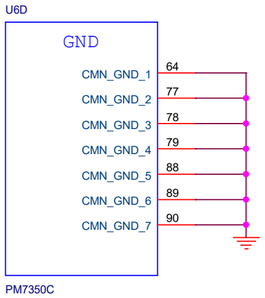
- **MVP150 - Min : 0.47uF , Max : 5uF**
- **MVP600 - Min : 4.7uF , Max : 23.5uF**
- **LVP600 - Min : 4.7uF , Max :**

NOTE:
L2B, L7B, L11B, L17B, L18B, L19B are pseudo-capless LDO

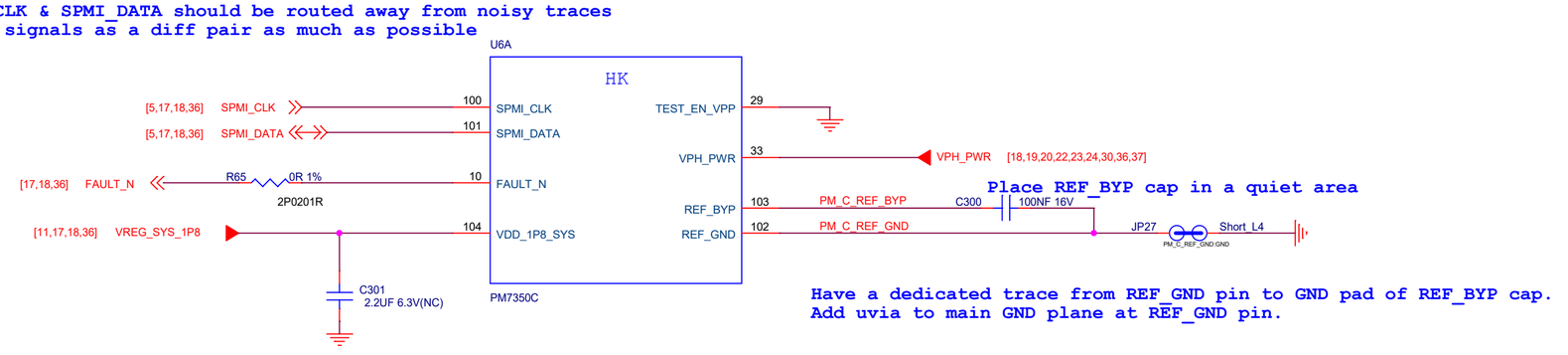
Size C	Title: RADXA DRAGON 5A		REV X1.0
	Page Name: PM7325_LDOs		
Date: Friday, June 20, 2025		Sheet 21 of 37	

PM7350C CTRL GPIO GND





Note:
SPMI_CLK & SPMI_DATA should be routed away from noisy traces
Route signals as a diff pair as much as possible



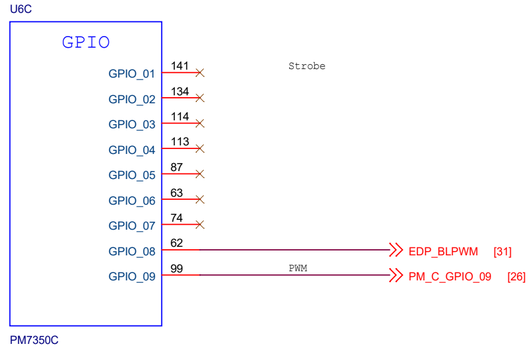
Place REF_BYP cap in a quiet area

Have a dedicated trace from REF_GND pin to GND pad of REF_BYP cap.
Add uvia to main GND plane at REF_GND pin.

NOTE:
MV: VPH_PWR or 1.8 V
LV : 1.8 V only

GPIO	Type	Configuration	Special function for QCM6490
1	LV	AMUX	FLASH_STROBE
2	LV	AMUX	FLASH_STROBE
3	LV	AMUX	FLASH_STROBE / PM8008_1_EN
4	LV	AMUX	FLASH_STROBE / PM8008_2_EN
5	MV	AMUX	AOSS_SLEEP_INDICATOR
6	MV		
7	MV		EDP_LCD_BL_EN
8	MV	PWM	EDP_LCD_PWM
9	MV	PWM	

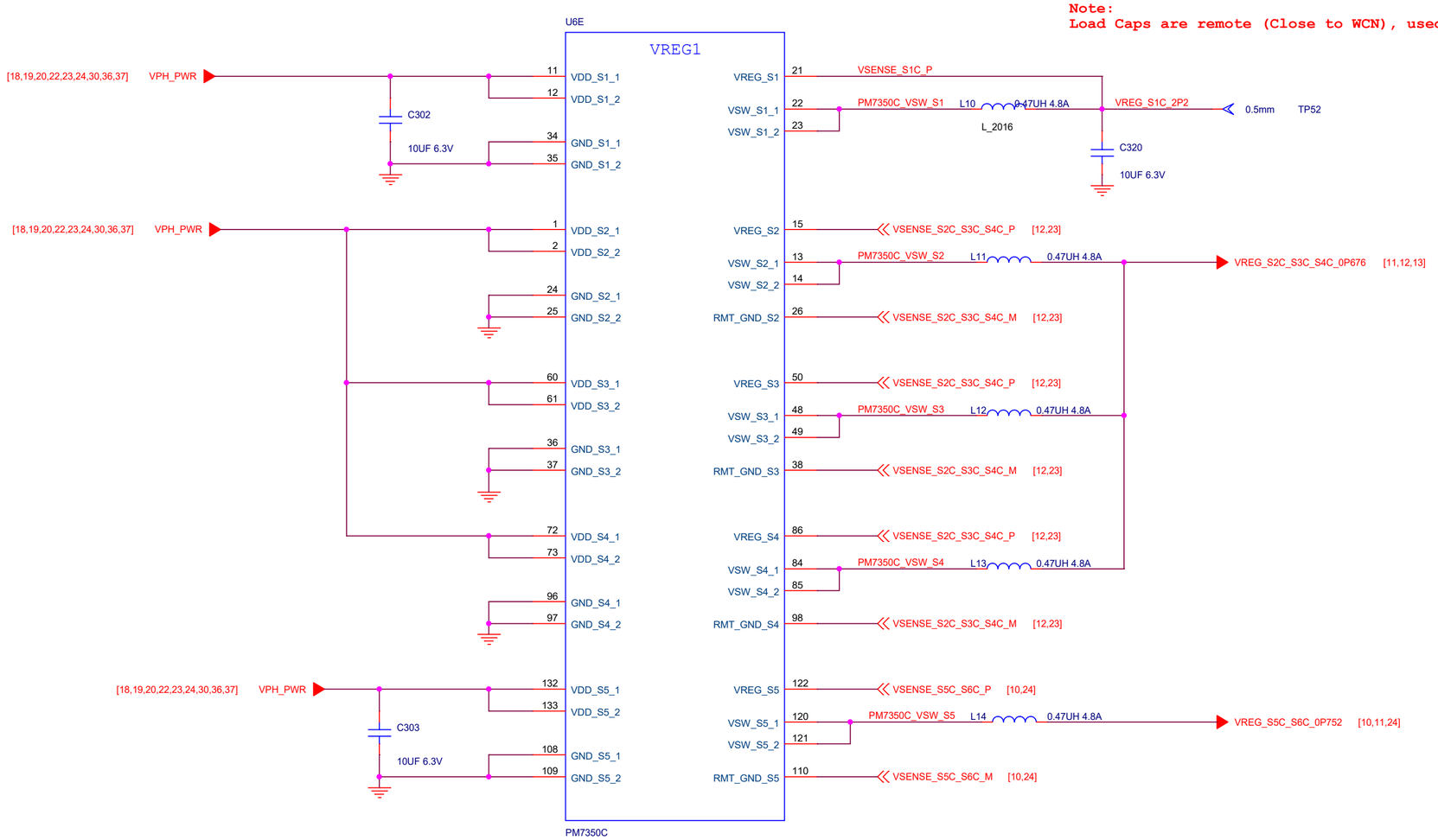
Please note that only GPIO_08 is available for fixed duty cycle variable frequency mode.



radxa

Size	Title:	REV
C	RADXA DRAGON 5A	X1.0
	Page Name: PM7350C_HK/IO/BOB_FLASH	
Date: Friday, June 20, 2025	Sheet 22 of 37	

PM7350C BUCKS 1 OF 2



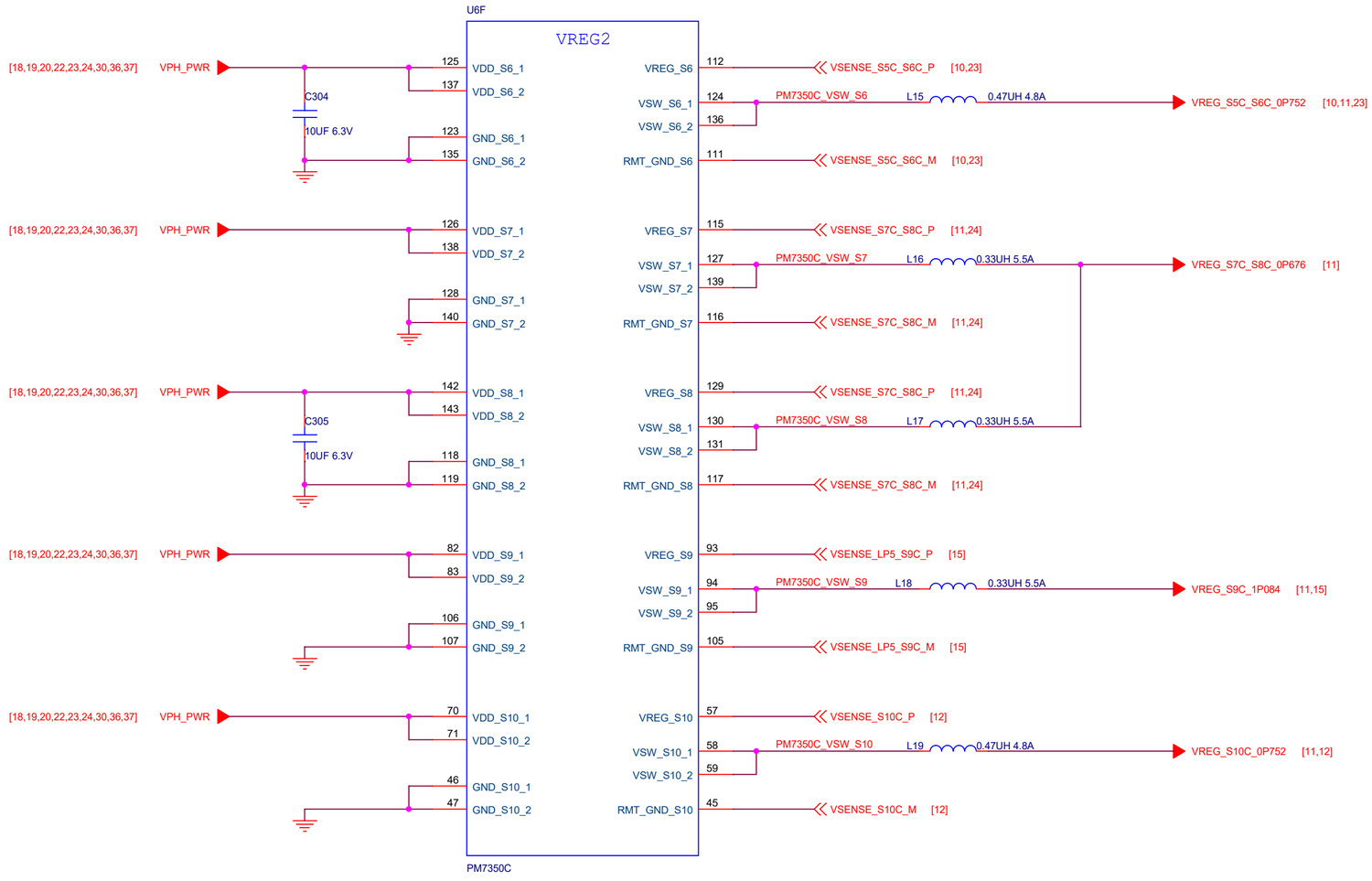
Note:
RMT P/M Diff Pair back to PMIC from load cap

Regulator	type	IRATED (A)	voltage	use
S1C	HFS515	1.5	2.2	WCN IPA
S2C	FTS520	13.5	0.816	CX, EBI
S3C	FTS520			
S4C	FTS520			
S5C	FTS520	2	0.752	Modem
S6C	FTS520			
S7C	FTS520	4	0.752	GFX
S8C	FTS520			
S9C	FTS520	1	1.084	LP_VDD2/2H
S10C	FTS520	1	0.752	MX

radxa

Size	Title:	REV
C	RADXA DRAGON 5A	X1.0
	Page Name: PM7350C_Bucks_S1-S5	
Date: Friday, June 20, 2025	Sheet 23 of 37	

PM7350C BUCKS 2 OF 2



Size C	Title: RADXA DRAGON Q5A	REV X1.0
	Page Name: PM7350C_Bucks_S6-S10	
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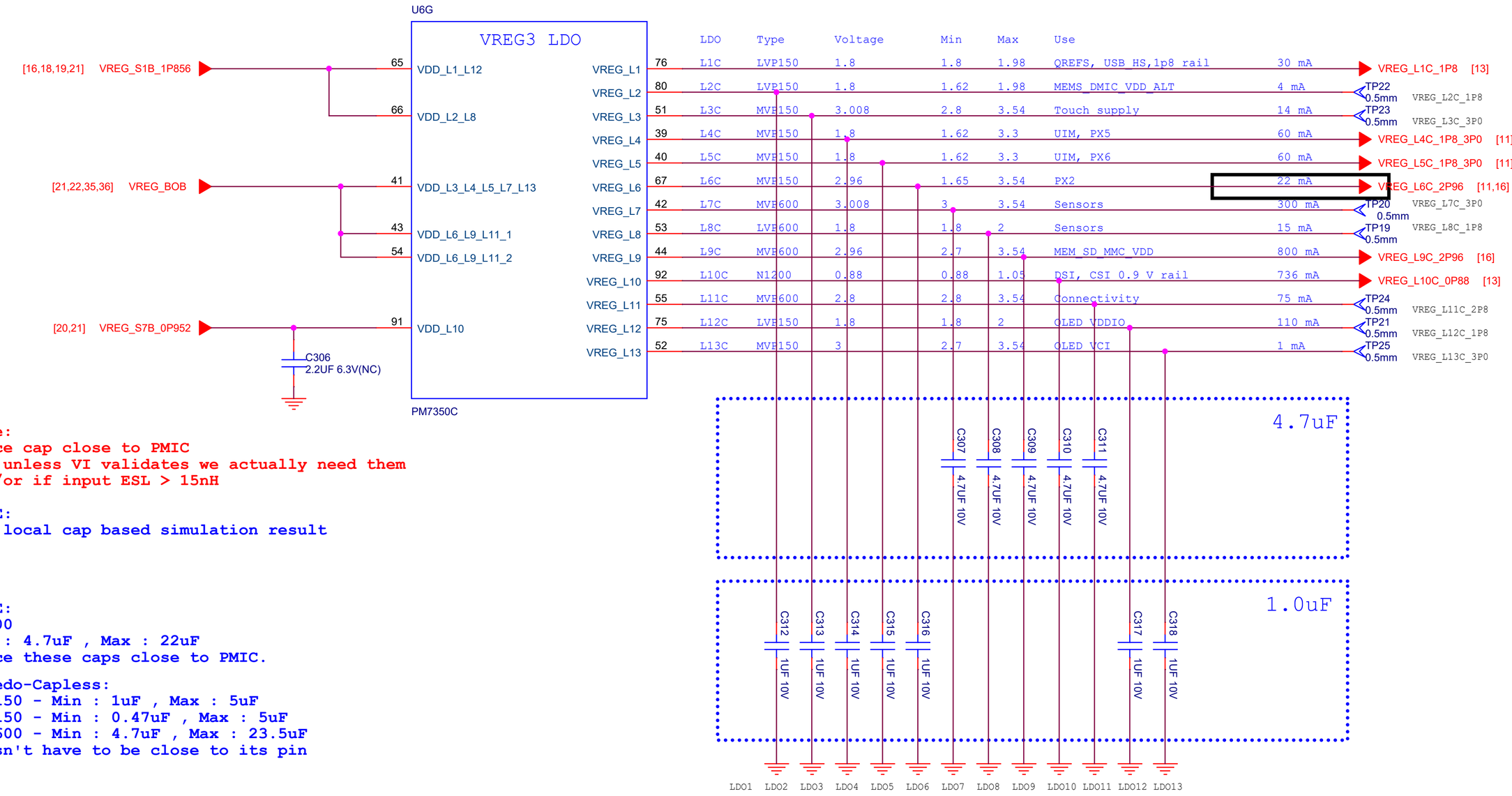
PM7350C LDOs



Note:
Place cap close to PMIC
DNI unless VI validates we actually need them and/or if input ESL > 15nH

NOTE:
Add local cap based simulation result

NOTE:
N1200
Min : 4.7uF , Max : 22uF
Place these caps close to PMIC.

Psuedo-Capless:
LVP150 - Min : 1uF , Max : 5uF
MVP150 - Min : 0.47uF , Max : 5uF
MVP600 - Min : 4.7uF , Max : 23.5uF
Doesn't have to be close to its pin

Pseudo capless allows users to place the LDO output capacitor physically/electrically far from the LDO output, near the load.
The routing ESL/ESR between the PMIC pin and the remote Cout should meet the capless LDO spec.
All PMOS LDOs are considered pseudo-capless, unless it has internal PMIC load.
If an internal PMIC load, the output cap must be placed close to the PMIC.

radxa

Size	Title:	REV
Custom	RADXA DRAGON Q5A	X1.0
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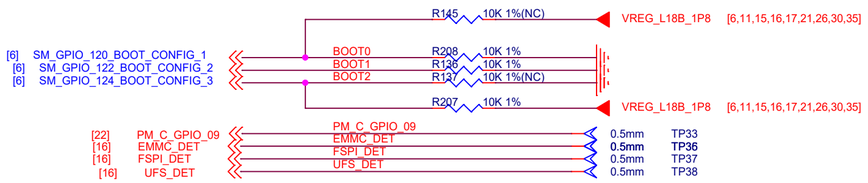
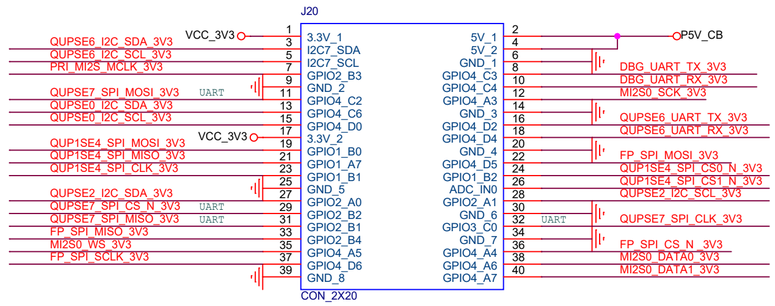
jtag testpoint

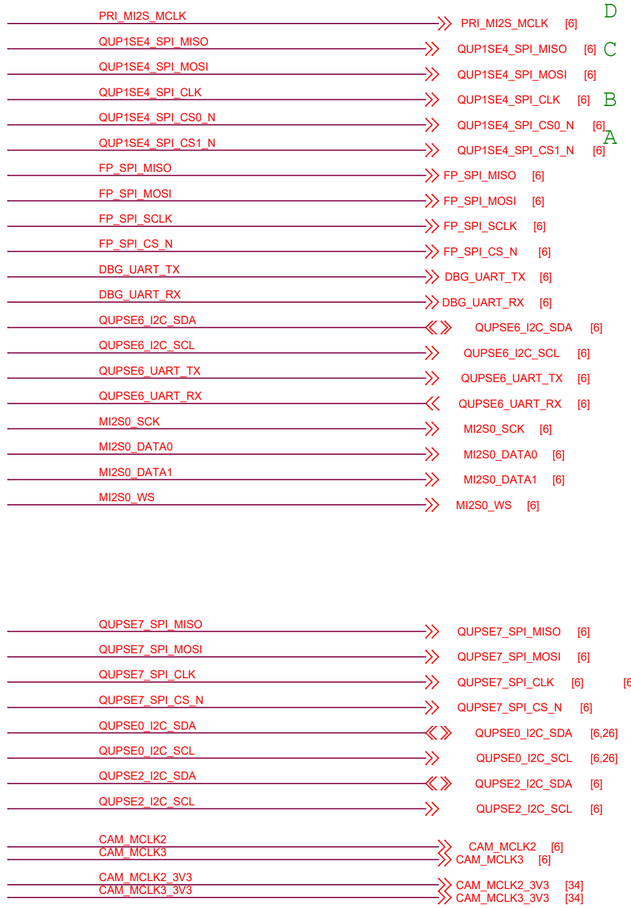
TP2 0.5mm — SM_RESOUT_N [5,16]

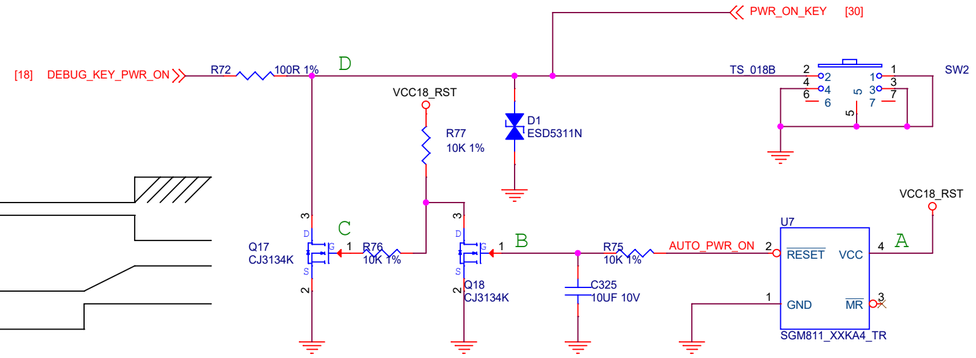
TP3 0.5mm — JTAG_PS_HOLD [17]

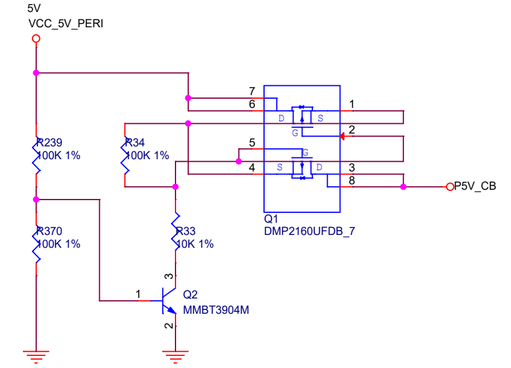


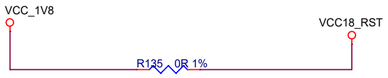


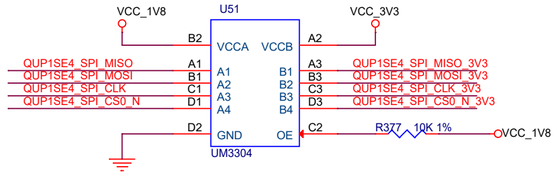
SDH FRAME&COVER Mark

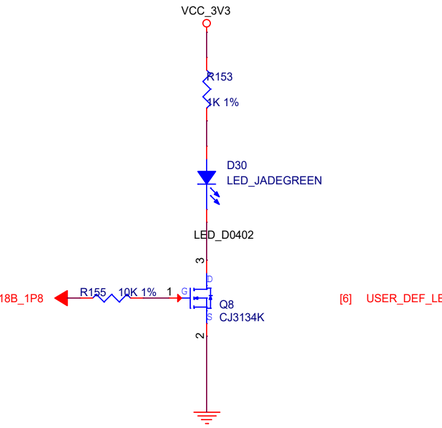


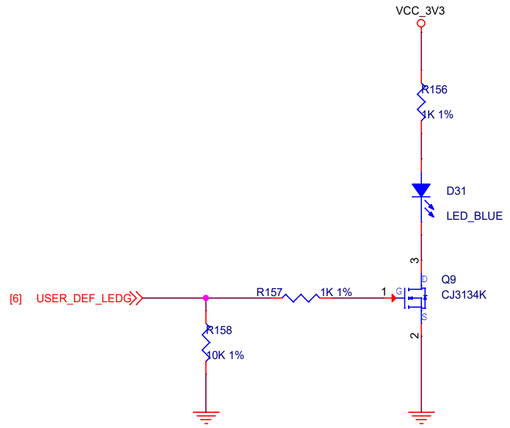


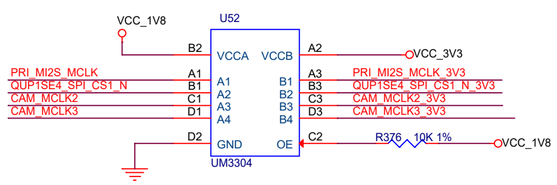


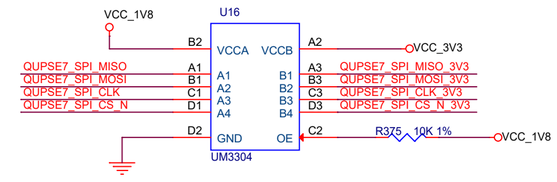


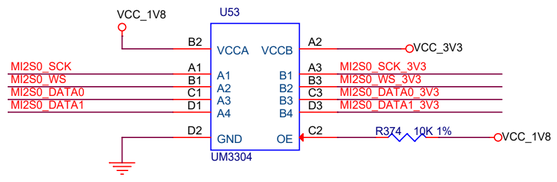


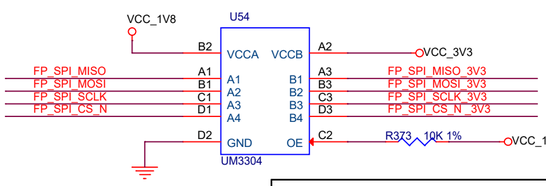


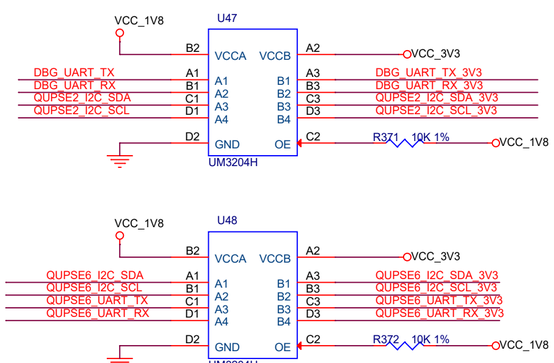


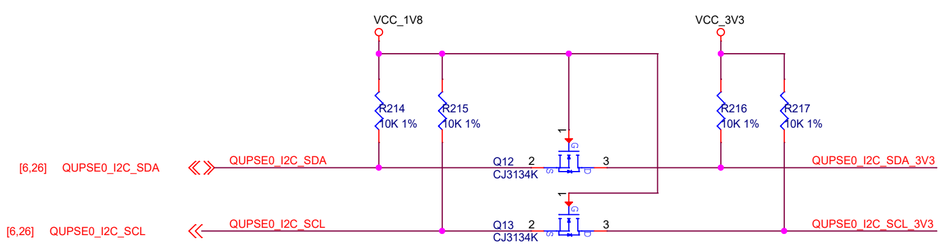












radxa			
Size C	Title: RADXA DRAGON Q5A		REV X1.0
	Page Name: JTAG&TP&SHD		
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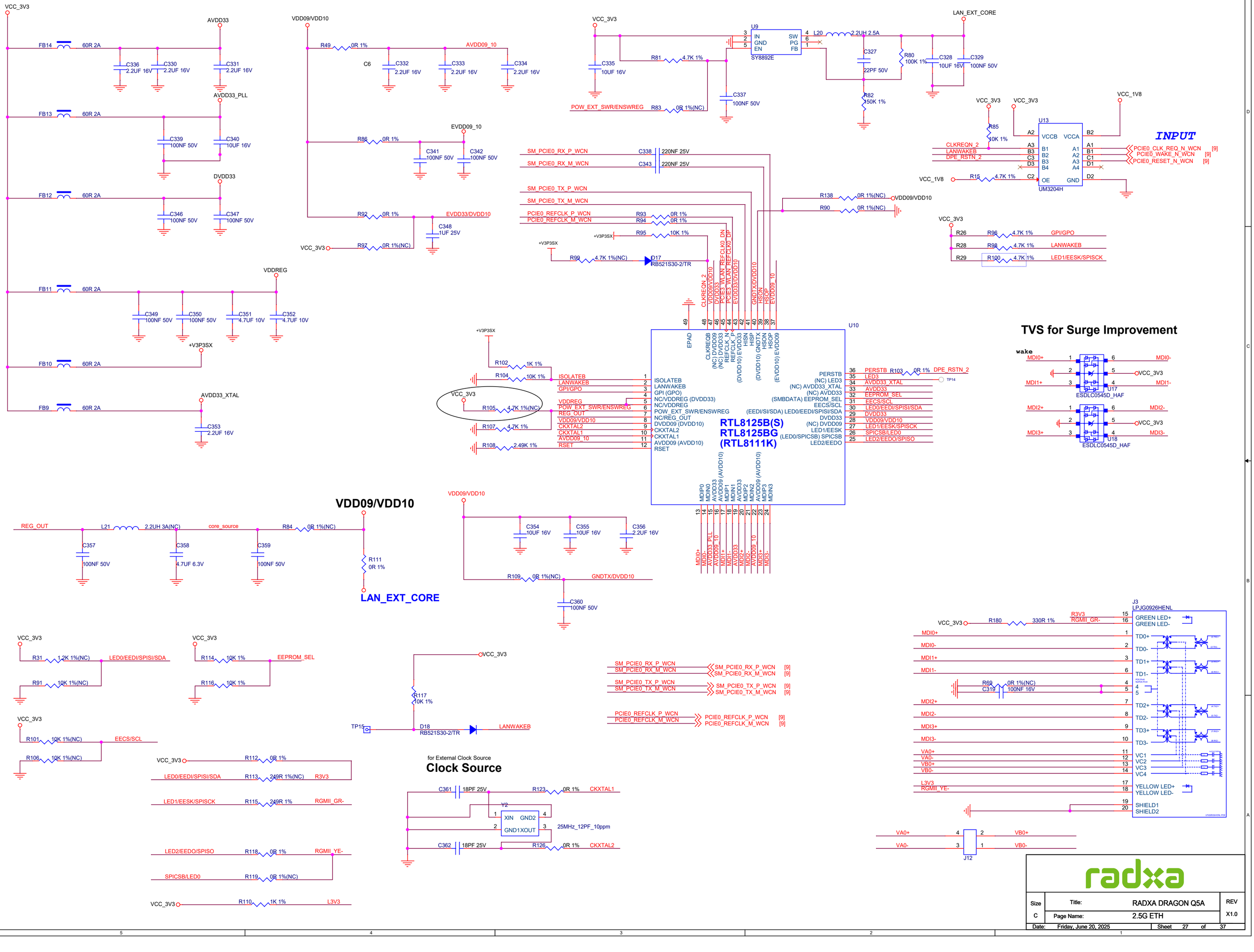
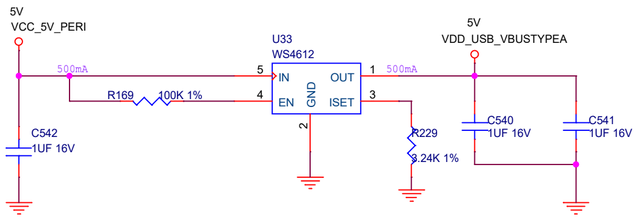
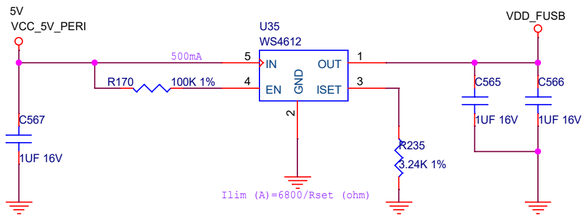
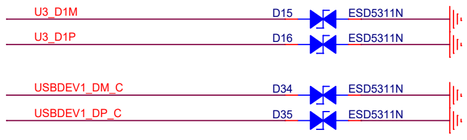

VCC_3V3
AVDD33
FB14 60R 2A
C336 2.2UF 16V
C330 2.2UF 16V
C331 2.2UF 16V
AVDD33_PLL
FB13 60R 2A
C339 100NF 50V
C340 10UF 16V
DVDD33
FB12 60R 2A
C346 100NF 50V
C347 100NF 50V
VDDREG
FB11 60R 2A
C349 100NF 50V
C350 100NF 50V
C351 4.7UF 10V
C352 4.7UF 10V
+V3P3SX
FB10 60R 2A
AVDD33_XTAL
FB9 60R 2A
C353 2.2UF 16V
VDD09/VDD10
R49 0R 1%
C6
C332 2.2UF 16V
C333 2.2UF 16V
C334 2.2UF 16V
AVDD09_10
EVDD09_10
R86 0R 1%
C341 100NF 50V
C342 100NF 50V
R92 0R 1%
EVDD33/DVDD10
C348 1UF 25V
VCC_3V3
R97 0R 1%(NC)
U9
IN
GND
EN
SW
PG
FB
SY8892E
L20 2.2UH 2.5A
C335 10UF 16V
R81 4.7K 1%
POW_EXT_SWR/ENSWREG
R83 0R 1%(NC)
C337 100NF 50V
C327 22PF 50V
R82 150K 1%
R80 100K 1%
C328 10UF 16V
C329 100NF 50V
LAN_EXT_CORE
SM_PCIE0_RX_P_WCN
SM_PCIE0_RX_M_WCN
C338 220NF 25V
C343 220NF 25V
SM_PCIE0_TX_P_WCN
SM_PCIE0_TX_M_WCN
PCIE0_REFCLK_P_WCN
PCIE0_REFCLK_M_WCN
R93 0R 1%
R94 0R 1%
+V3P3SX
R95 10K 1%
R99 4.7K 1%(NC)
D17
RB521S30-2/TR
R138 0R 1%(NC)
R90 0R 1%(NC)
VDD09/VDD10
VCC_3V3
R85 10K 1%
U13
VCCB
VCCA
OE
GND
UM3204H
CLKREQN_2
LANWAKEB
DPE_RSTN_2
VCC_1V8
R15 4.7K 1%
PCIE0_CLK_REQ_N_WCN [9]
PCIE0_WAKE_N_WCN [9]
PCIE0_RESET_N_WCN [9]
INPUT
R26 R96 4.7K 1% GPI/GPO
R28 R98 4.7K 1% LANWAKEB
R29 R100 4.7K 1% LED1/EESK/SPISCK
CLKREQN_2
VDD09/VDD10
DVDD33
PCIE3_WLAN_REFCLK0_DN
PCIE3_WLAN_REFCLK0_DP
EVDD33/DVDD10
GNDTX/DVDD10
HISON
HSOP
EVDD09_10
EPAD
CLKREQB
(NC) DVDD33
REFCLK_N
REFCLK_P
(DVDD10) EVDD33
HISN
HISP
(DVDD10) GNDTX
HSON
HSOP
(EVDD10) EVDD09
U10
RTL8125B(S)
RTL8125BG
(RTL8111K)
+V3P3SX
R102 1K 1%
R104 10K 1%
VCC_3V3
R105 4.7K 1%(NC)
R107 4.7K 1%
R108 2.49K 1%
ISOLATEB
LANWAKEB
GPI/GPO
VDDREG
POW_EXT_SWR/ENSWREG
REG_OUT
VDD09/VDD10
CKXTAL2
CKXTAL1
AVDD09_10
RSET
ISOLATEB
LANWAKEB
GPI (GPO)
NC/VDDREG (DVDD33)
NC/VDDREG
POW_EXT_SWR/ENSWREG
NC/REG_OUT
DVDD09 (DVDD10)
CKXTAL2
CKXTAL1
AVDD09 (AVDD10)
RSET
PERSTB
(NC) LED3
(NC) AVDD33_XTAL
(NC) AVDD33
(SMBDATA) EEPROM_SEL
EECS/SCL
(EEDI/SI/SDA) LED0/EEDI/SPISI/SDA
DVDD33
(NC) DVDD09
LED1/EESK
(LED0/SPICSB) SPICSB
LED2/EEDO
R103 0R 1% DPE_RSTN_2
TP14
PERSTB
LED3
AVDD33_XTAL
AVDD33
EEPROM_SEL
EECS/SCL
LED0/EEDI/SPISI/SDA
DVDD33
VDD09/VDD10
LED1/EESK/SPISCK
SPICSB/LED0
LED2/EEDO/SPISO
MDIP0
MDIN0
AVDD33
AVDD09 (AVDD10)
MDIP1
MDIN1
AVDD33
MDIP2
MDIN2
AVDD09 (AVDD10)
MDIP3
MDIN3
MDI0+
MDI0-
AVDD33_PLL
AVDD09_10
MDI1+
MDI1-
AVDD33
MDI2+
MDI2-
AVDD09_10
MDI3+
MDI3-
TVS for Surge Improvement
wake
MDI0+
MDI0-
VCC_3V3
MDI1+
MDI1-
U17
ESDLC0545D_HAF
MDI2+
MDI2-
VCC_3V3
MDI3+
MDI3-
U18
ESDLC0545D_HAF
VDD09/VDD10
REG_OUT
L21 2.2UH 3A(NC)
core_source
R84 0R 1%(NC)
C357 100NF 50V
C358 4.7UF 6.3V
C359 100NF 50V
R111 0R 1%
LAN_EXT_CORE
VDD09/VDD10
C354 10UF 16V
C355 10UF 16V
C356 2.2UF 16V
R109 0R 1%(NC)
GNDTX/DVDD10
C360 100NF 50V
VCC_3V3
R31 1.2K 1%(NC)
LED0/EEDI/SPISI/SDA
R91 10K 1%(NC)
VCC_3V3
R114 10K 1%
EEPROM_SEL
R116 10K 1%
VCC_3V3
R101 10K 1%(NC)
EECS/SCL
R106 10K 1%(NC)
R117 10K 1%
TP15
D18
RB521S30-2/TR
LANWAKEB
SM_PCIE0_RX_P_WCN
SM_PCIE0_RX_M_WCN
SM_PCIE0_RX_P_WCN [9]
SM_PCIE0_RX_M_WCN [9]
SM_PCIE0_TX_P_WCN
SM_PCIE0_TX_M_WCN
SM_PCIE0_TX_P_WCN [9]
SM_PCIE0_TX_M_WCN [9]
PCIE0_REFCLK_P_WCN
PCIE0_REFCLK_M_WCN
PCIE0_REFCLK_P_WCN [9]
PCIE0_REFCLK_M_WCN [9]
VCC_3V3
R112 0R 1%
LED0/EEDI/SPISI/SDA
R113 249R 1%(NC)
R3V3
LED1/EESK/SPISCK
R115 249R 1%
RGMII_GR-
LED2/EEDO/SPISO
R118 0R 1%
RGMII_YE-
SPICSB/LED0
R119 0R 1%(NC)
VCC_3V3
R110 1K 1%
L3V3
for External Clock Source
Clock Source
C361 18PF 25V
R123 0R 1%
CKXTAL1
Y2
XIN
GND2
GND1
XOUT
25MHz_12PF_10ppm
C362 18PF 25V
R126 0R 1%
CKXTAL2
J3
LPJG0926HENL
VCC_3V3
R180 330R 1%
R3V3
RGMII_GR-
GREEN LED+
GREEN LED-
MDI0+
MDI0-
MDI1+
MDI1-
R69 0R 1%(NC)
C319 100NF 16V
MDI2+
MDI2-
MDI3+
MDI3-
TD0+
TD0-
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
VA0+
VA0-
VB0+
VB0-
VC1
VC2
VC3
VC4
L3V3
RGMII_YE-
YELLOW LED+
YELLOW LED-
SHIELD1
SHIELD2
VA0+
VA0-
J12
VB0+
VB0-
radxa
Size C
Title: RADXA DRAGON Q5A
REV X1.0
Page Name: 2.5G ETH
Date: Friday, June 20, 2025
Sheet 27 of 37

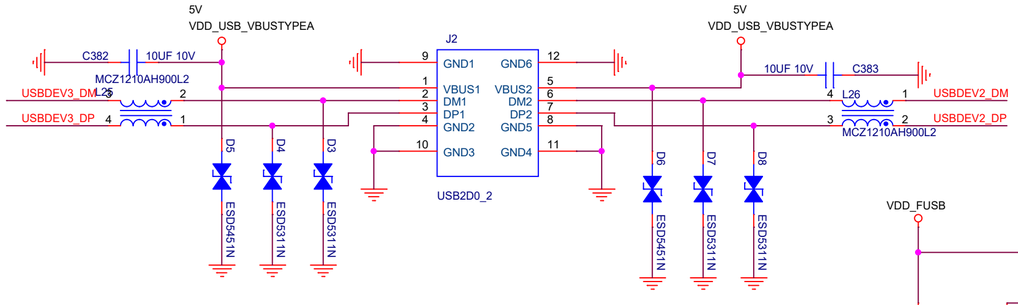
USB HUB x4 PORTS

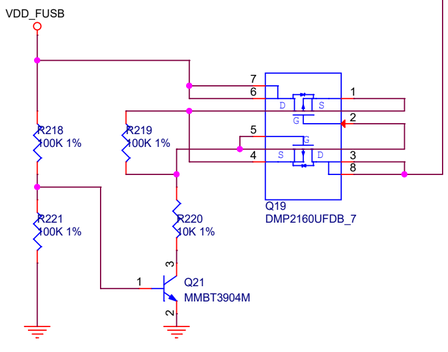
HUB

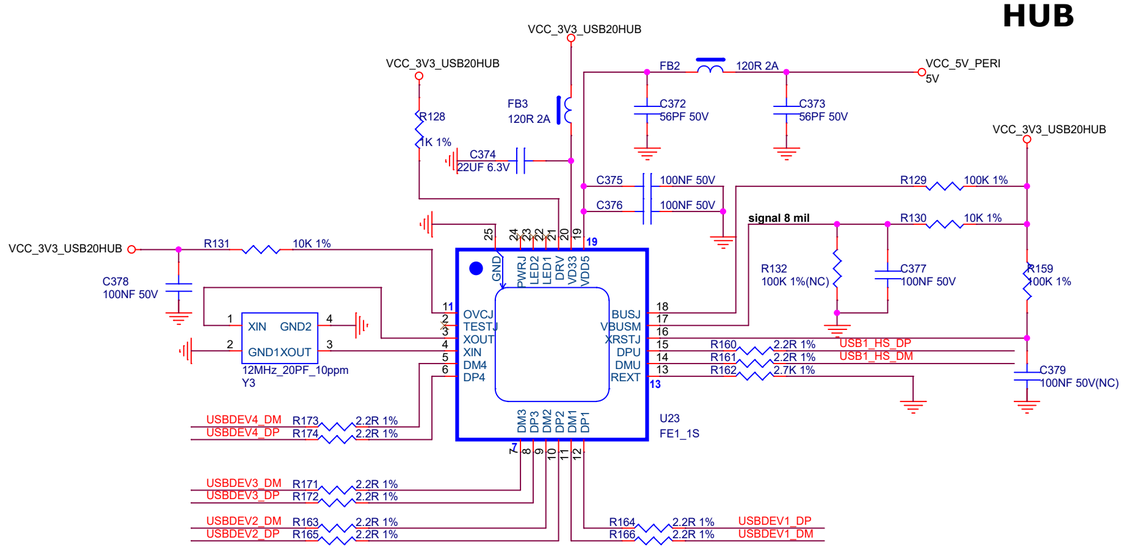


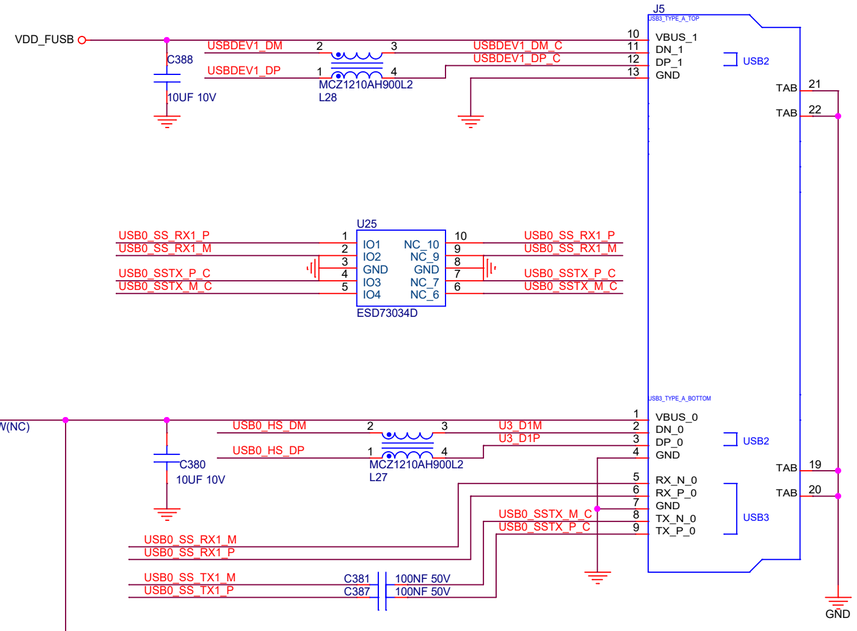












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	Page Name: USB		
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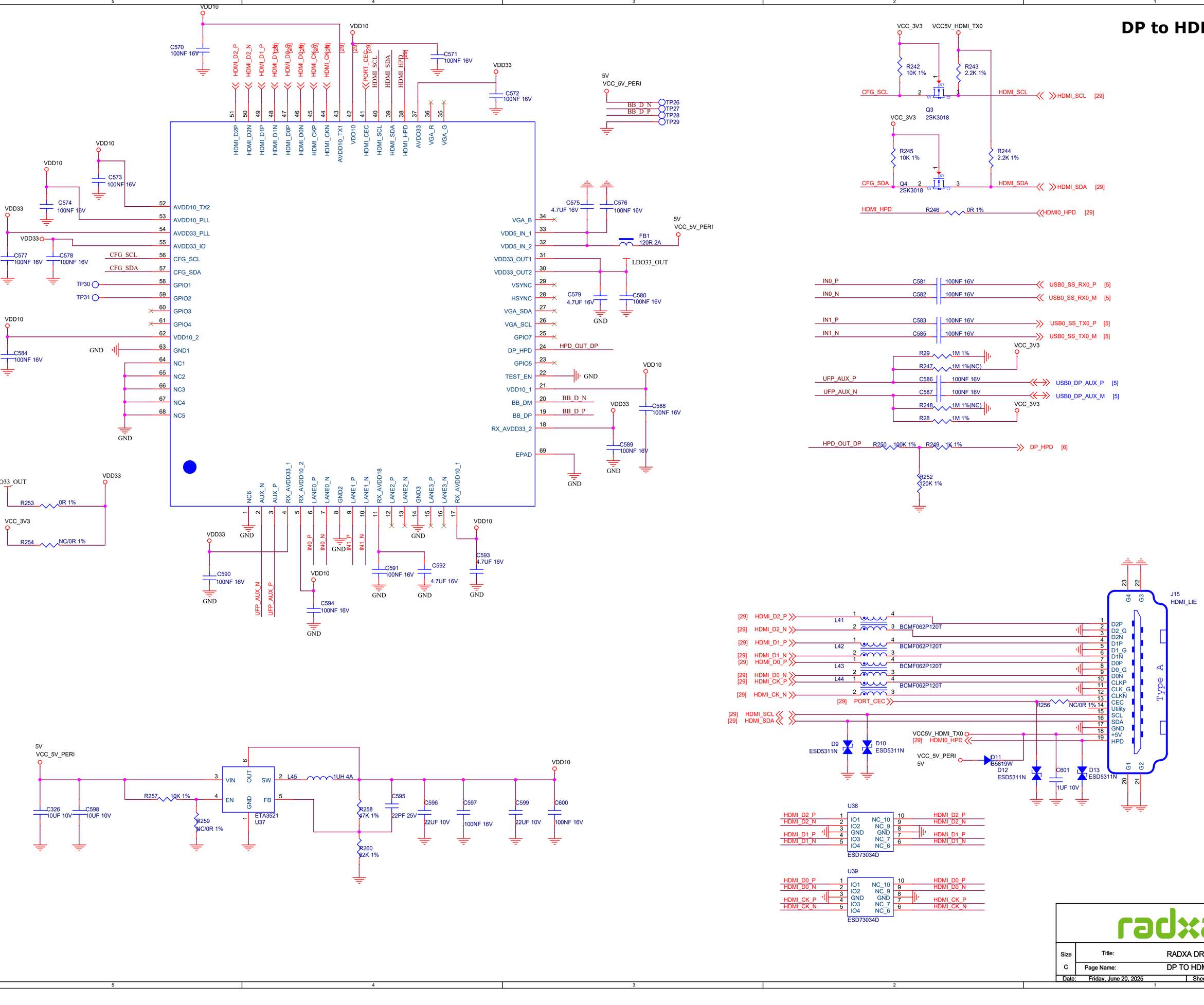
DP to HDMI



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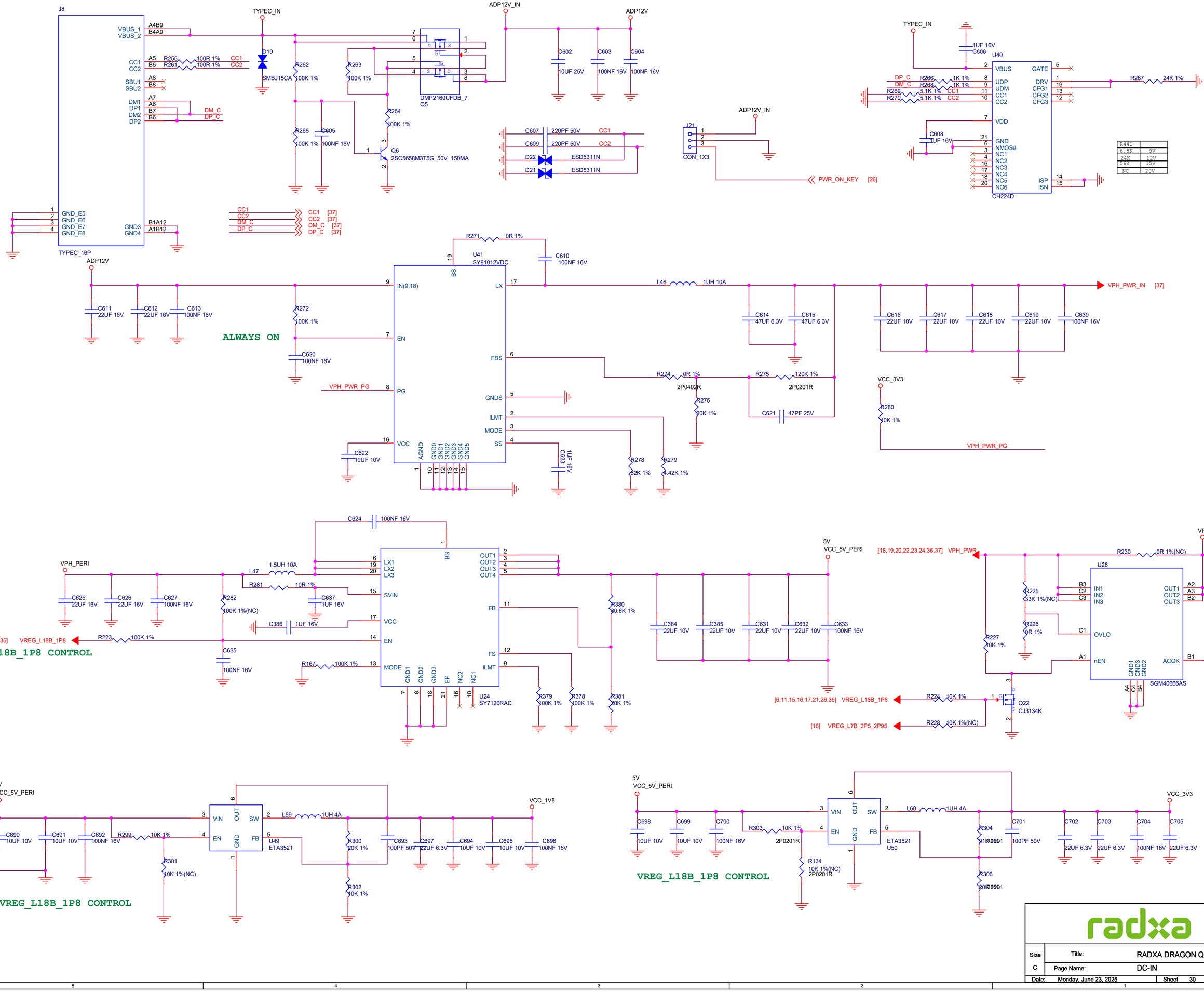
	Page Name: DP TO HDMI	
Date: Friday, June 20, 2025	Sheet 29 of 37	



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REV	X1.0
Page Name:	DC-IN
Date:	Monday, June 23, 2025
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LCD MIPI

TS_INT_N
TS_RESET_N

TS_INT_N [6]
TS_RESET_N [6]

TS_SPI_MISO_I2C_SDA
TS_SPI_MOSI_I2C_SCL

TS_SPI_MISO_I2C_SDA [6]
TS_SPI_MOSI_I2C_SCL [6]

DSI0_B1_CLK_P
DSI0_C1_CLK_M
DSI0_A0_LN0_P
DSI0_B0_LN0_M
DSI0_C0_LN1_P
DSI0_A1_LN1_M
DSI0_A2_LN2_P
DSI0_B2_LN2_M
DSI0_C2_LN3_P
DSI0_NC_LN3_M

DSI0_B1_CLK_P [8]
DSI0_C1_CLK_M [8]
DSI0_A0_LN0_P [8]
DSI0_B0_LN0_M [8]
DSI0_C0_LN1_P [8]
DSI0_A1_LN1_M [8]
DSI0_A2_LN2_P [8]
DSI0_B2_LN2_M [8]
DSI0_C2_LN3_P [8]
DSI0_NC_LN3_M [8]

DISP0_RESET_N

DISP0_RESET_N [6]

VCC_3V3_LCD
VCC_1V8
R312 0R 1%
DISP0_RESET_N
R313 0R 1%
DSI0_B0_LN0_M
DSI0_A0_LN0_P
DSI0_A1_LN1_M
DSI0_C0_LN1_P
DSI0_C1_CLK_M
DSI0_B1_CLK_P
DSI0_B2_LN2_M
DSI0_A2_LN2_P
DSI0_NC_LN3_M
DSI0_C2_LN3_P
TP_RST
VCC_3V3
C640
100NF 16V
TP_INT
TP_SDA
TP_SCL
VCC_3V3_LCD
VCC_LEDK
VCC_LEDA

J10

41	PAD1	
1	VDD3V3	
2	IOVCC1V8-3V3	
3	SENSOR-INT	
4	RESET	
5	6	
6	GND1	
7	MIPI-0N	DSI0_B0_LN0_M
8	MIPI-0P	DSI0_A0_LN0_P
9	GND2	
10	MIPI-1N	DSI0_A1_LN1_M
11	MIPI-1P	DSI0_C0_LN1_P
12	GND3	
13	MIPI-CKN	DSI0_C1_CLK_M
14	MIPI-CKP	DSI0_B1_CLK_P
15	GND4	
16	MIPI-2N	DSI0_B2_LN2_M
17	MIPI-2P	DSI0_A2_LN2_P
18	GND5	
19	MIPI-3N	DSI0_NC_LN3_M
20	MIPI-3P	DSI0_C2_LN3_P
21	GND6	
22	GND7	
23	TP-RESET	TP_RST
24	TP-VCC	VCC_3V3
25	TP-INT	TP_INT
26	TP-SDA	TP_SDA
27	TP-SCL	TP_SCL
28	GND8	
29	GND9	
30	VCC3V31	VCC_3V3_LCD
31	VCC3V32	
32	GND11	
33	GND12	
34	LED-1	VCC_LEDK
35	LED-	
36	37	
37	38	
38	LED+1	VCC_LEDA
39	LED+	
40	PAD2	

LCD_39P

VCC_3V3
U14
SGM2578AAD
VCC_3V3_LCD
A2
VI
VO
A1
[6] LCD_VCC_EN
LCD_VCC_EN
R361 0R 1% B2
ON
G
B1
C464
10UF 10V
C465
100NF 16V

5V
VCC_5V_PERI
VCC_LEDA
L48 4.7UH 2A
D14
B5819W
C641
100NF 16V
C642
10UF 10V
C643
100NF 16V
C644
2.2UF 10V
7
IN
LX1
LX2
4
5
1
NC1
NC2
OVP
NC3
NC4
FB
8
6
10
2
9
EN
GND2
U43
SY7203DBC
11
[22] EDP_BLPWM
EDP_BLPWM
R314
100K 1%
VCC_LEDK
R315
1.1R 1%

VCC_1V8
U8
VCC_3V3
GND
C447
100NF 16V
B2
VCCA
VCCB
A2
TS_RESET_N
TS_INT_N
TS_SPI_MISO_I2C_SDA
TS_SPI_MOSI_I2C_SCL
A1
B1
C1
D1
A1
A2
A3
A4
B1
B2
B3
B4
A3
B3
C3
D3
TP_RST
TP_INT
TP_SDA
TP_SCL
GND
D2
GND
OE
C2
R344
4.7K 1%
VCC_1V8
UM3204H

radxa

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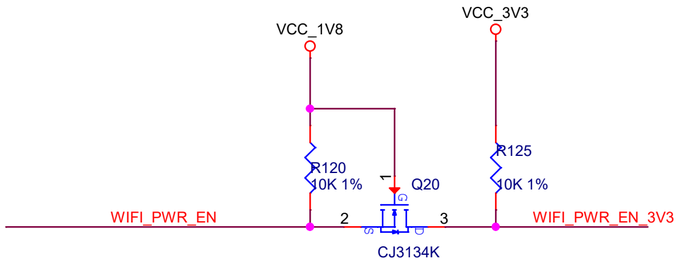
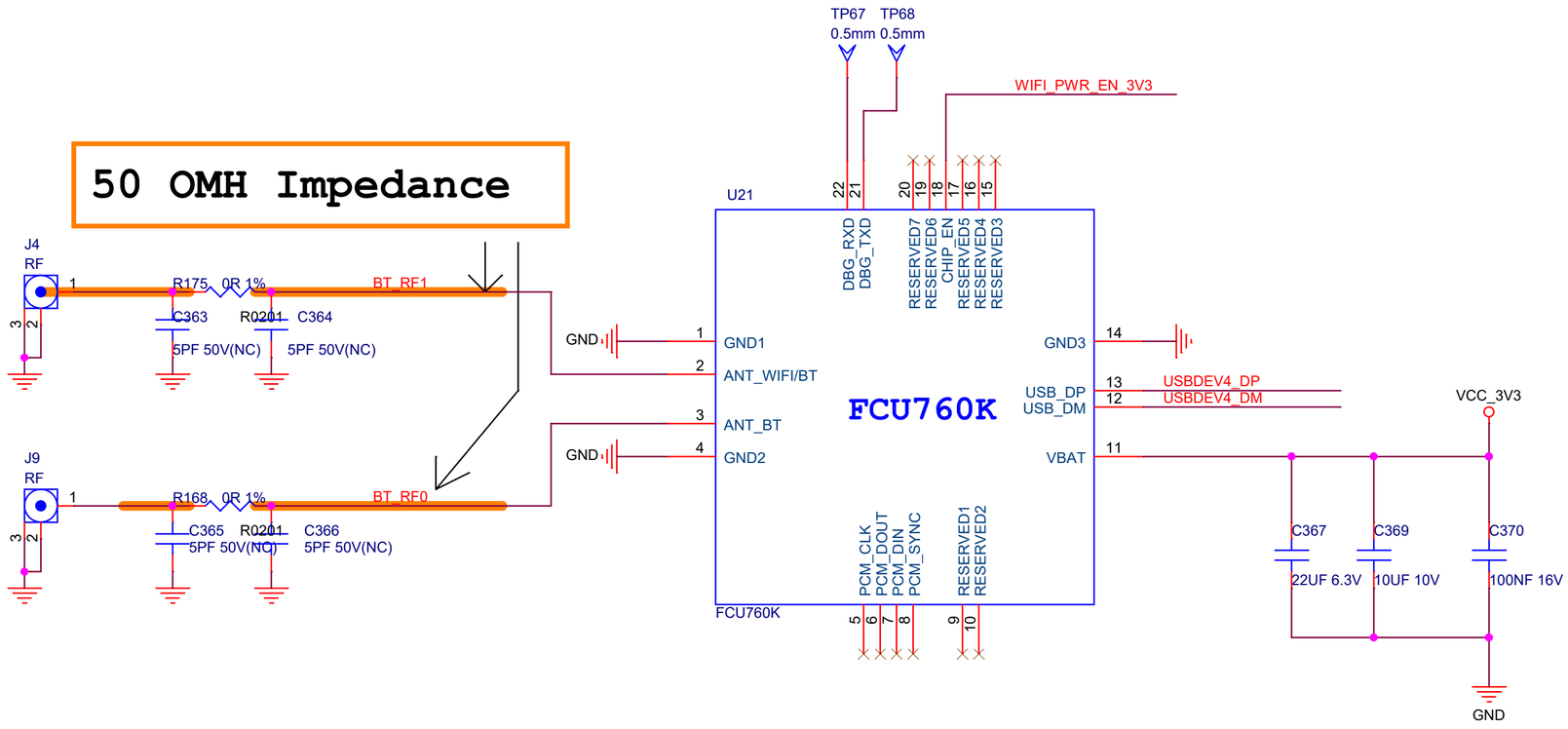
USB2_WLAN





Size	Title:	RADXA DRAGON Q5A	REV
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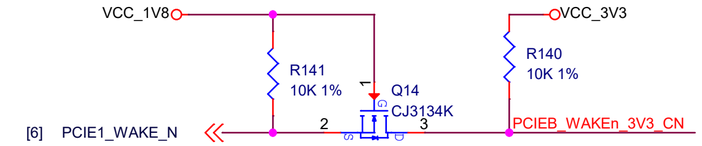
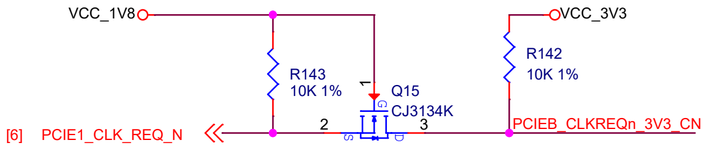
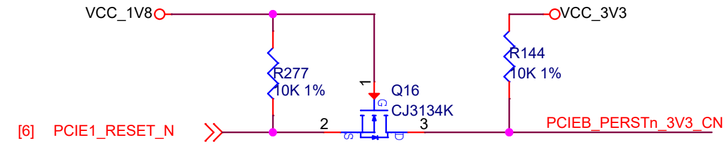
PCIEB







[9] PCIE1_REFCLK_P — PCIE1_REFCLK_P

[9] PCIE1_REFCLK_M — PCIE1_REFCLK_M

[9] PCIE1_RX0_P — PCIE1_RX0_P

[9] PCIE1_RX0_M — PCIE1_RX0_M

keep cap enough placeholder to test PCIE GEN3

[9] PCIE1_TX0_P — PCIE1_TX0_P_C

[9] PCIE1_TX0_M — PCIE1_TX0_M_C

[9] PCIE1_RX1_P — PCIE1_RX1_P

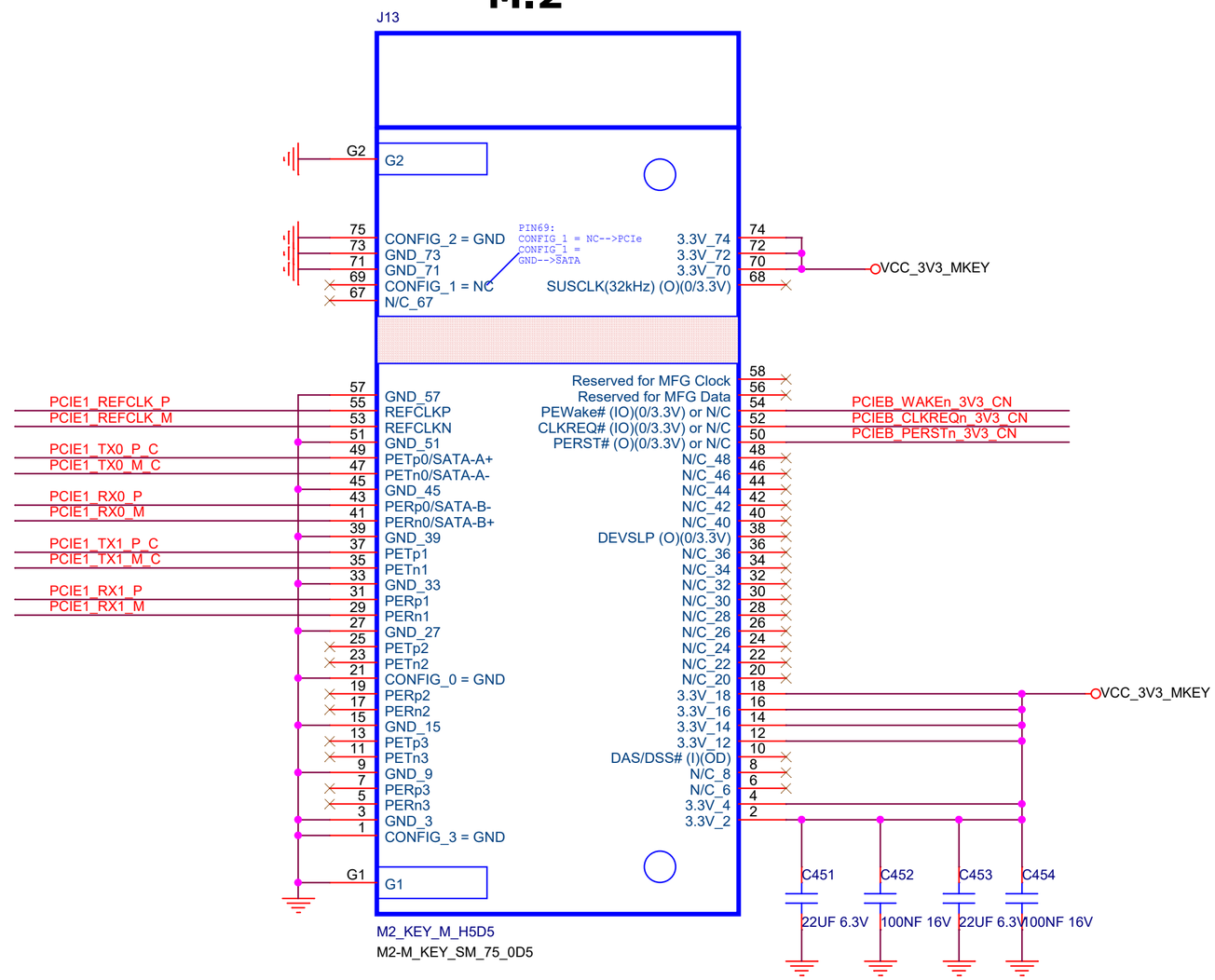
[9] PCIE1_RX1_M — PCIE1_RX1_M

keep cap enough placeholder to test PCIE GEN3

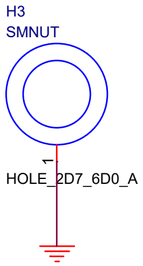
[9] PCIE1_TX1_P — PCIE1_TX1_P_C

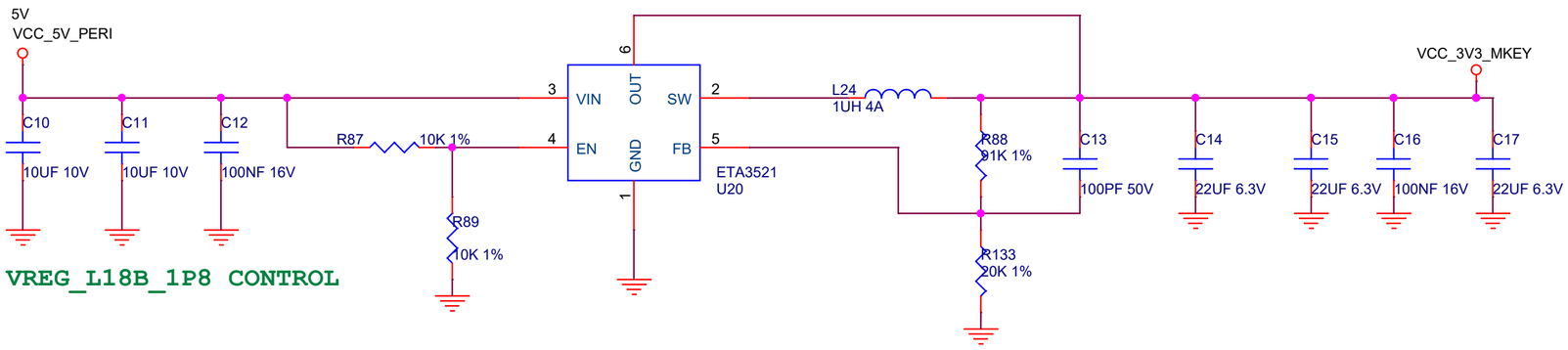
[9] PCIE1_TX1_M — PCIE1_TX1_M_C

M.2



2230





VREG_L18B_1P8 CONTROL

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CSI0 C-PHY/D-PHY

(WIDE)

[8] CSI0_NC_CLK_P → CSI0_NC_CLK_P
[8] CSI0_A0_CLK_M → CSI0_A0_CLK_M
[8] CSI0_B0_LN0_P → CSI0_B0_LN0_P
[8] CSI0_C0_LN0_M → CSI0_C0_LN0_M
[8] CSI0_A1_LN1_P → CSI0_A1_LN1_P
[8] CSI0_B1_LN1_M → CSI0_B1_LN1_M
[8] CSI0_C1_LN2_P → CSI0_C1_LN2_P
[8] CSI0_A2_LN2_M → CSI0_A2_LN2_M
[8] CSI0_B2_LN3_P → CSI0_B2_LN3_P
[8] CSI0_C2_LN3_M → CSI0_C2_LN3_M

[8] CSI2_NC_CLK_P → CSI2_NC_CLK_P
[8] CSI2_A0_CLK_M → CSI2_A0_CLK_M
[8] CSI2_B0_LN0_P → CSI2_B0_LN0_P
[8] CSI2_C0_LN0_M → CSI2_C0_LN0_M
[8] CSI2_A1_LN1_P → CSI2_A1_LN1_P
[8] CSI2_B1_LN1_M → CSI2_B1_LN1_M

[6] CAM0_POWER_EN → CAM0_POWER_EN
[6] CAM0_RESET_N → CAM0_RESET_N

[6] CAM2_RESET_N → CAM2_RESET_N

[6] CCI_I2C0_SDA → CCI_I2C0_SDA
[6] CCI_I2C0_SCL → CCI_I2C0_SCL

[6] CCI_I2C2_SDA → CCI_I2C2_SDA
[6] CCI_I2C2_SCL → CCI_I2C2_SCL

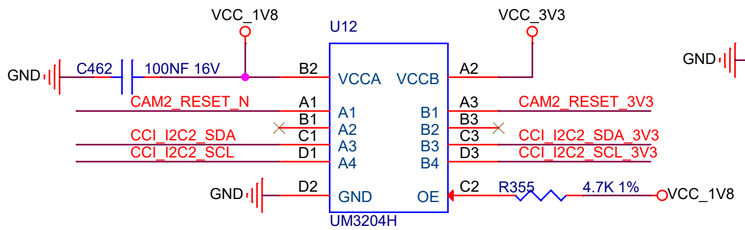
[6] CAM_MCLK0 → CAM_MCLK0

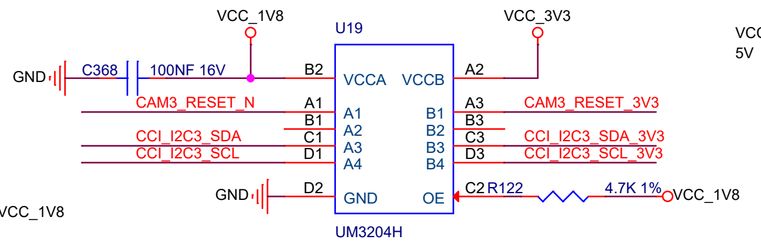
[26] CAM_MCLK2_3V3 → CAM_MCLK2_3V3
[26] CAM_MCLK3_3V3 → CAM_MCLK3_3V3

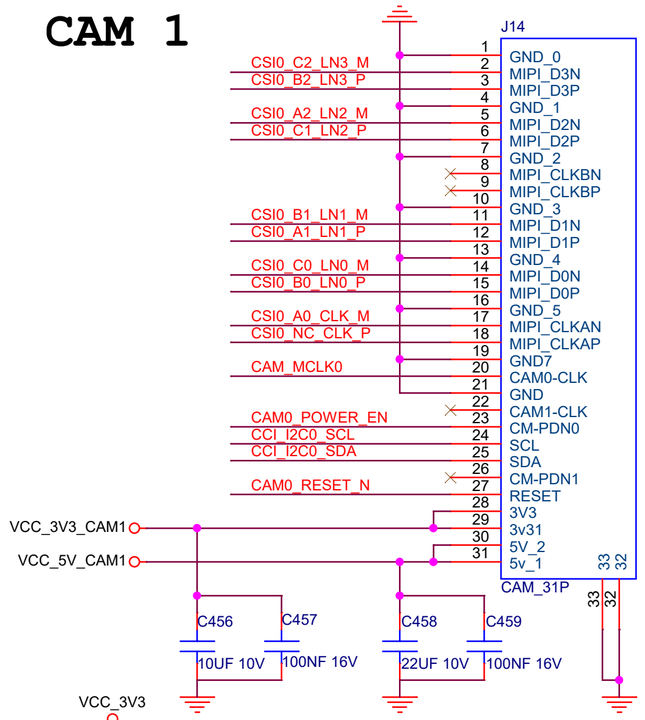
[6] CAM3_RESET_N → CAM3_RESET_N
[6] CCI_I2C3_SDA → CCI_I2C3_SDA
[6] CCI_I2C3_SCL → CCI_I2C3_SCL

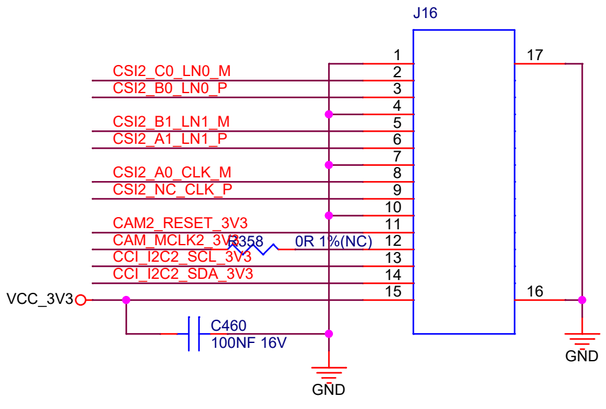
[8] CSI3_NC_CLK_P → CSI3_NC_CLK_P
[8] CSI3_A0_CLK_M → CSI3_A0_CLK_M
[8] CSI3_B0_LN0_P → CSI3_B0_LN0_P
[8] CSI3_C0_LN0_M → CSI3_C0_LN0_M
[8] CSI3_A1_LN1_P → CSI3_A1_LN1_P
[8] CSI3_B1_LN1_M → CSI3_B1_LN1_M

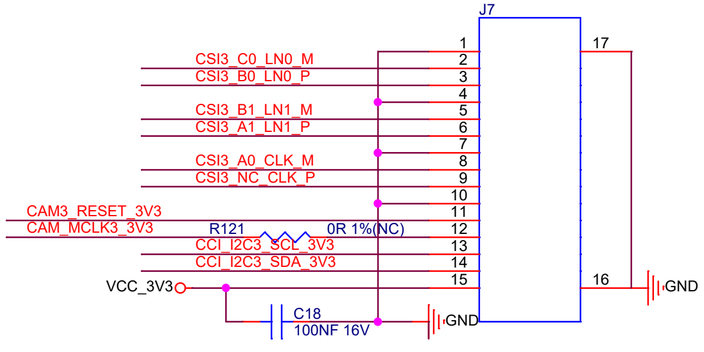
CSI1 C-PHY/D-PHY











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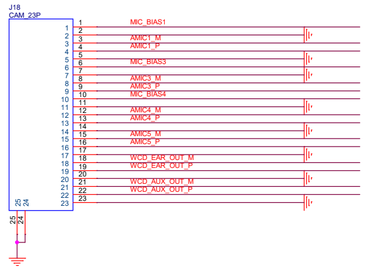
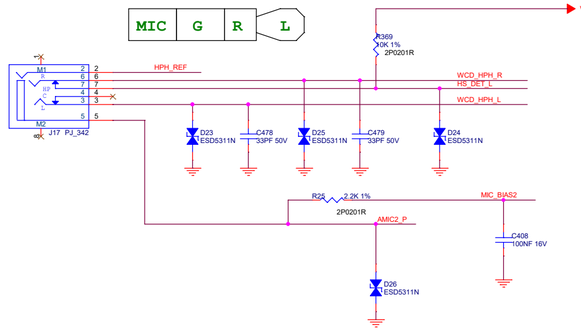
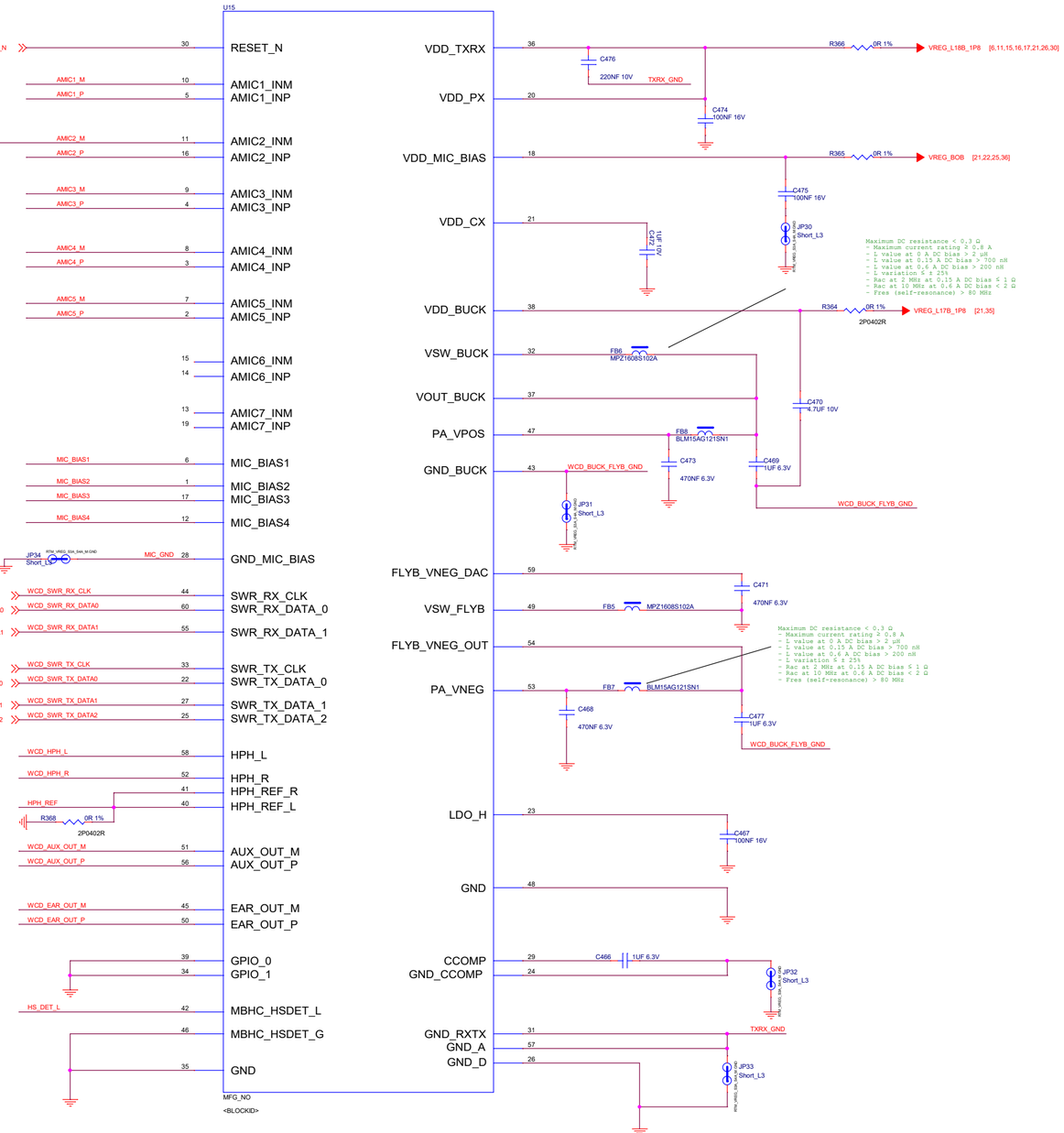
AUDIO







NOTE 1: ROUTE AN ISOLATED GROUND TRACE FROM CCOMP_REF TO THE CAP GROUND, THEN VIA TO THE MAIN GROUND PLANE
NOTE 2: PLACE VDD_BUCK CAP AS CLOSE TO CHIP EDGE AS POSSIBLE AND MINIMIZE LOOP INDUCTANCE
NOTE 3: USE SHORT AND WIDE TRACES FOR BUCK AND FLYBACK RELATED NETS
NOTE 4: ANALOG MIC INPUTS SHOULD BE ISOLATED WITH GROUND FROM NOISY OR SWITCHING SIGNALS AND SUPPLIES

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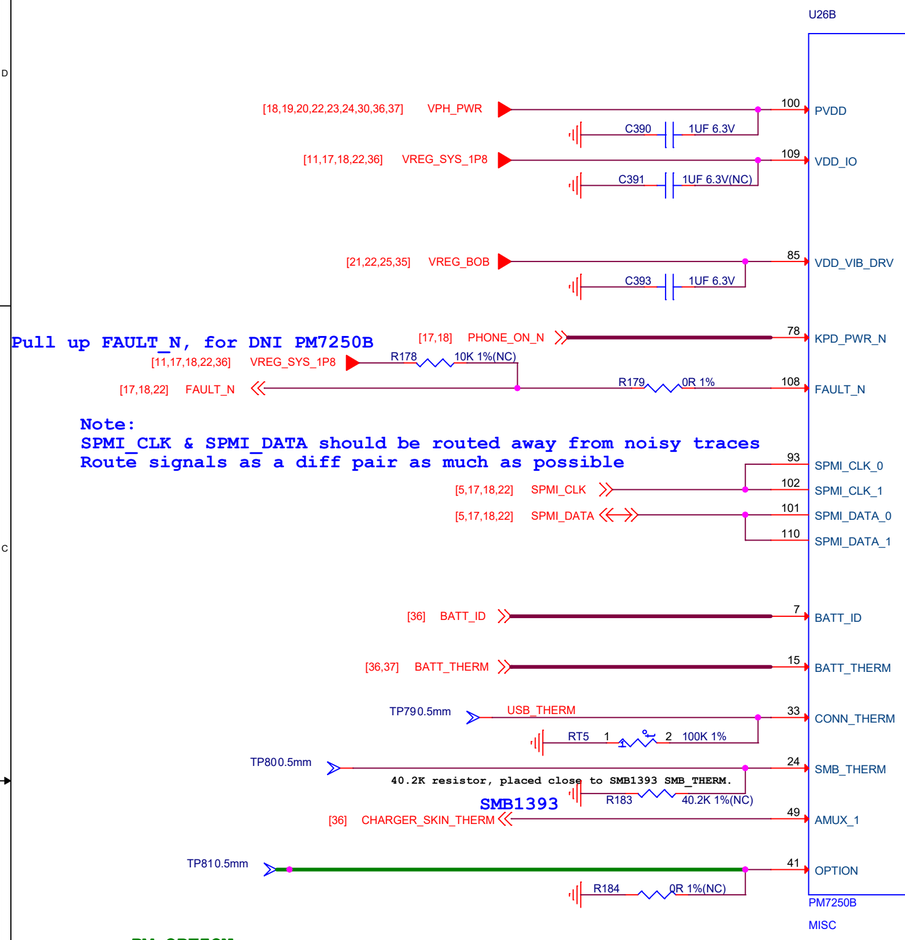
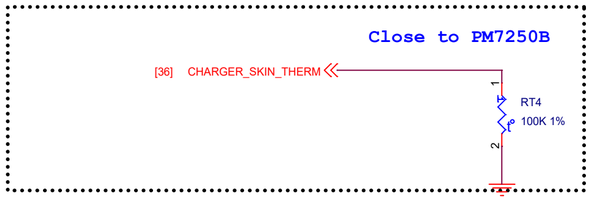
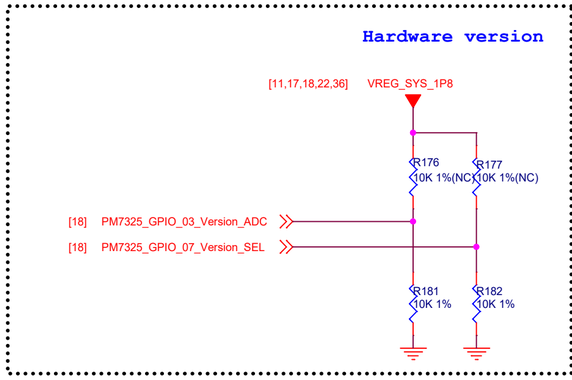
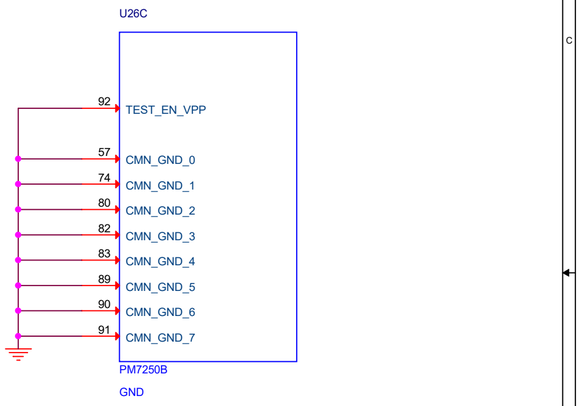
PM7250B CTRL GPIO GND





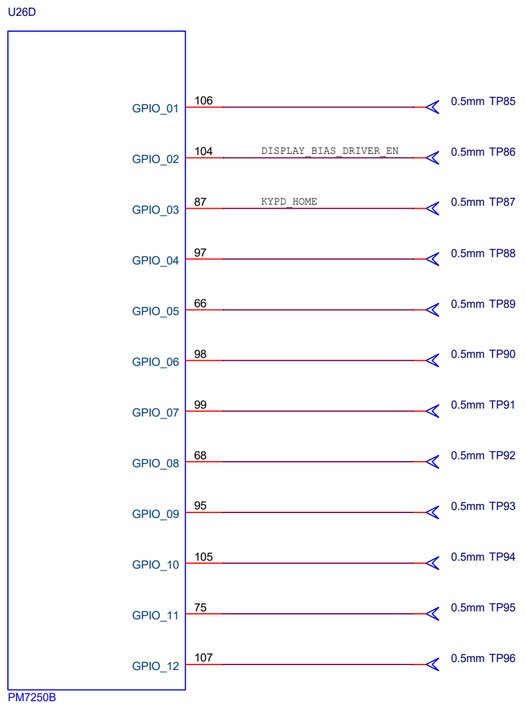


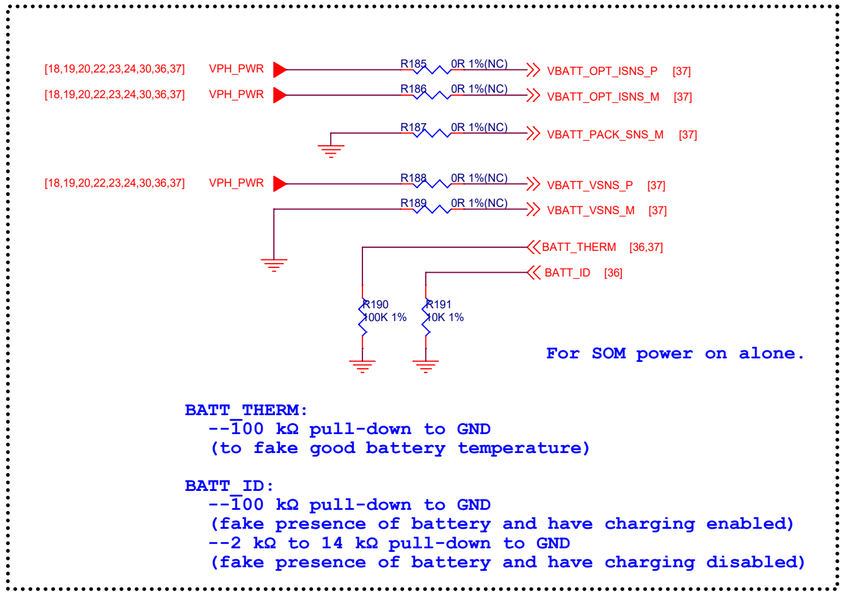


PM_OPTION:
Configuration selection for micro USB and Type-C connectors.
--DNI for Type-C and populate 0 ohm for micro USB
--Disable FMB

NOTE:
MV: VPH_PWR or 1.8 V
LV : 1.8 V only

GPIO	Type	Configuration	Special function for QCM6490
1	LV	AMUX	I2C_INT
2	LV		DISPLAY_BIAS_DRIVER_EN
3	LV		KYPD_HOME
4	LV		
5	MV	AMUX	mmW monitor
6	MV		SMB_STAT
7	MV		
8	MV	AMUX	camera temperature
9	LV		Factory mode boot 1
10	LV		Factory mode boot 2
11	LV	AMUX	
12	LV	AMUX	mmW monitor





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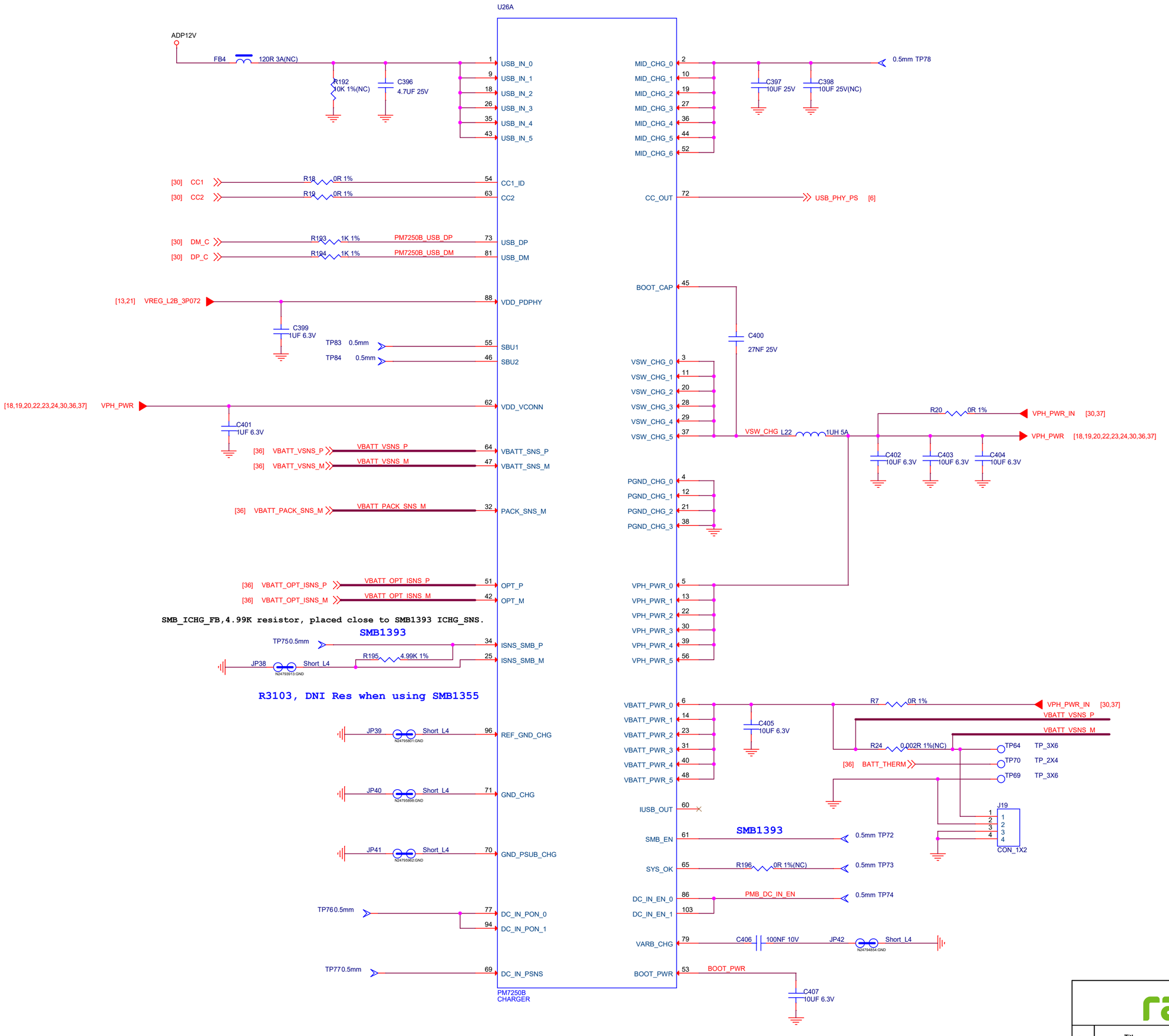
PM7250B CHG FG



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