

ROCK PI 4_CORE

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Note:

器件参数说明

1:如果 Value 为 **DP**,说明暂时不贴。

2:如果 Option 有 **DP**,说明 暂 先 不 贴 。



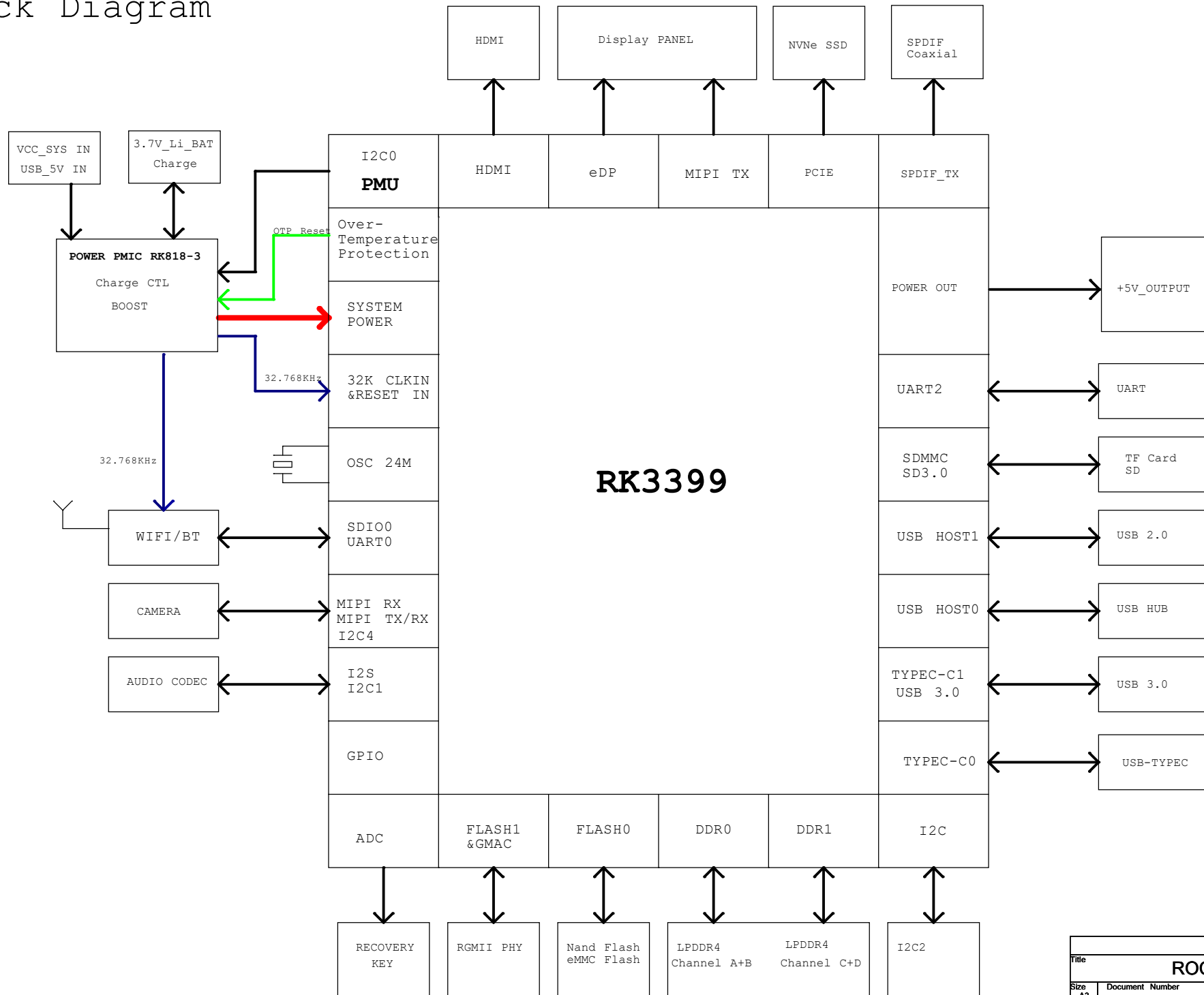
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Change List

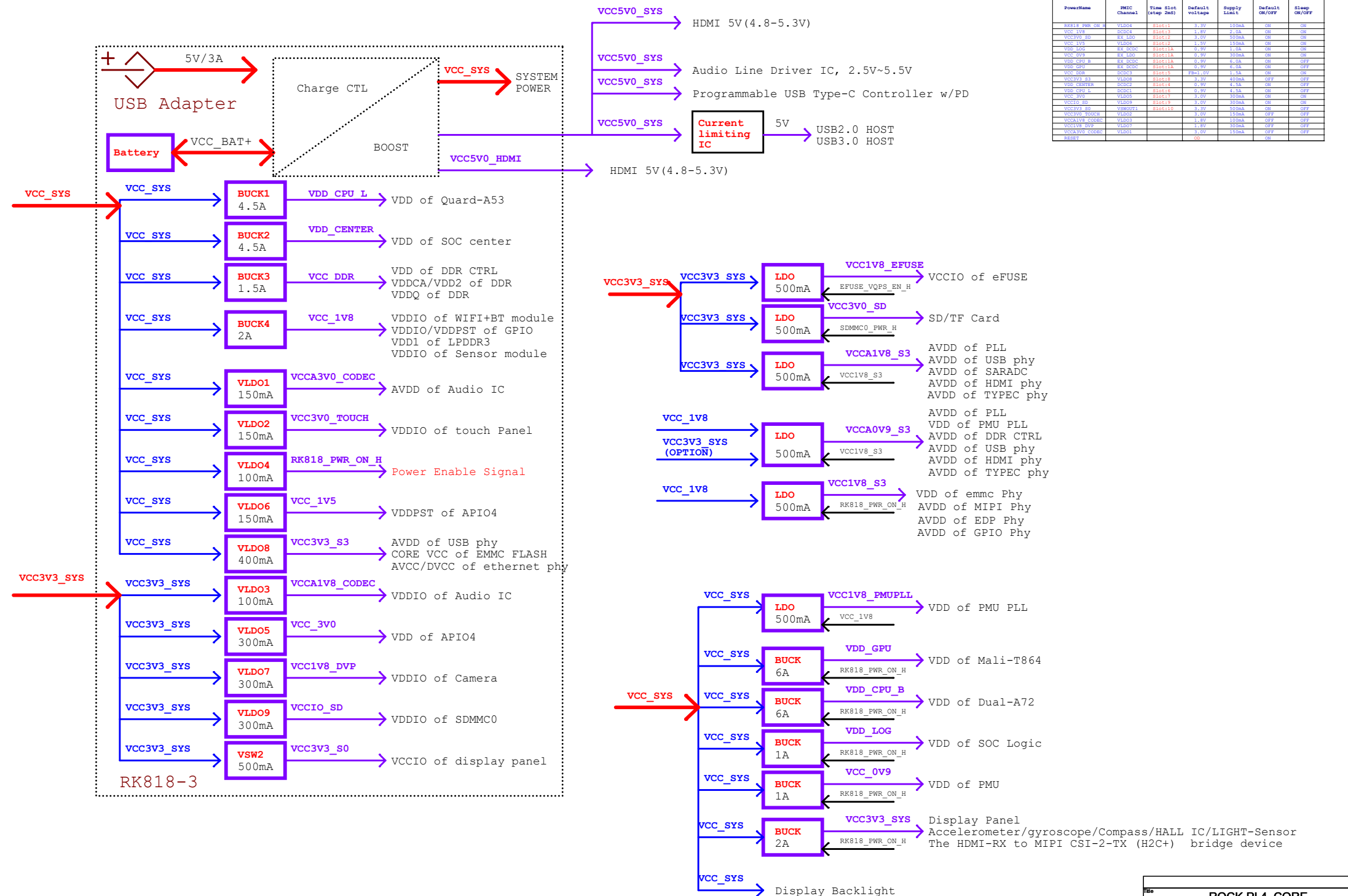
Version	Date	Author	Change Note	Approved
V1.0	20200114			

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Block Diagram



RK818-3 Power Diagram and Sequence



PowerName	PMIC Channel	Time Slot (step 2nd)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF
RK818_PWB_ON	VLD04	Slot11	1.8V	150mA	ON	ON
VCC_1V8	BUCK4	Slot11	1.8V	2.0A	ON	ON
VCC3V0_SD	EX_LDO	Slot12	3.0V	500mA	ON	ON
VCC_1V5	VLD06	Slot12	1.5V	150mA	ON	ON
VDD_405	EX_LDO	Slot11A	0.9V	1.0A	ON	ON
VCC_OV9	EX_LDO	Slot11A	0.9V	500mA	ON	ON
VDD_GPU	EX_BUCK	Slot11A	0.9V	4.0A	ON	OFF
VDD_DDR	BUCK3	Slot11B	1.1V	1.5A	ON	ON
VDD_CENTER	BUCK2	Slot11B	0.9V	4.0A	ON	OFF
VDD_CPU_B	BUCK6	Slot11B	1.0V	500mA	ON	ON
VDD_LOG	VLD09	Slot11B	1.0V	500mA	ON	ON
VDD_OV9	BUCK1A	Slot11B	1.0V	500mA	ON	ON
VCC3V3_SYS	VLD08	Slot11C	3.0V	500mA	OFF	OFF
VCC1V8_DVP	VLD07	Slot11C	1.8V	500mA	OFF	OFF
VCCA3V0_CODECC	VLD01	Slot11C	3.0V	150mA	ON	OFF
VCC1V8	BUCK3	Slot11C	1.8V	150mA	ON	ON

I2C MAP

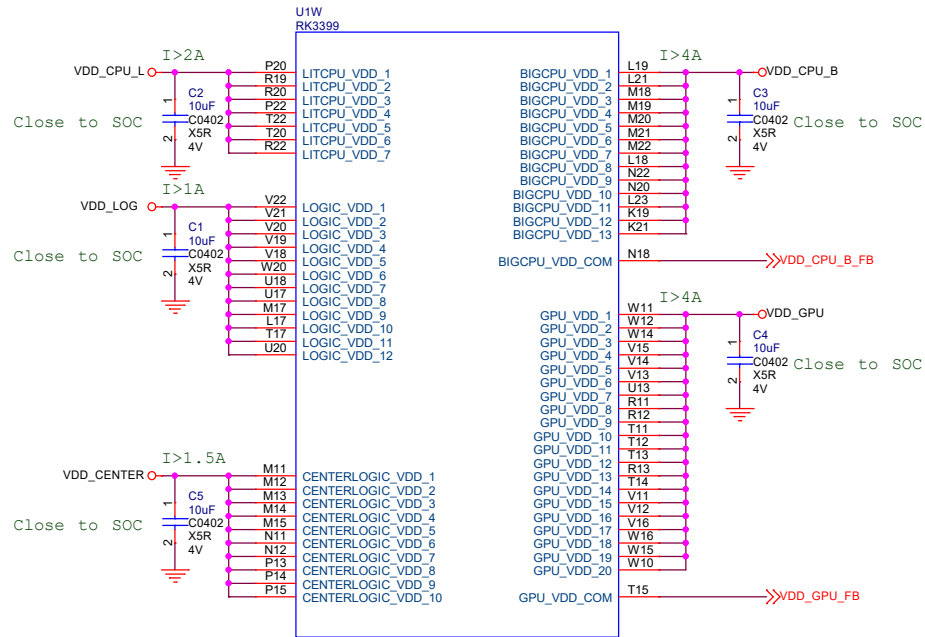
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz, 400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5		VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44, 0x46	USB-TypeC Mux	100kHz, 400KHz, 1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECTOR	
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		VCC_1V8			High Speed CONNECTOR	

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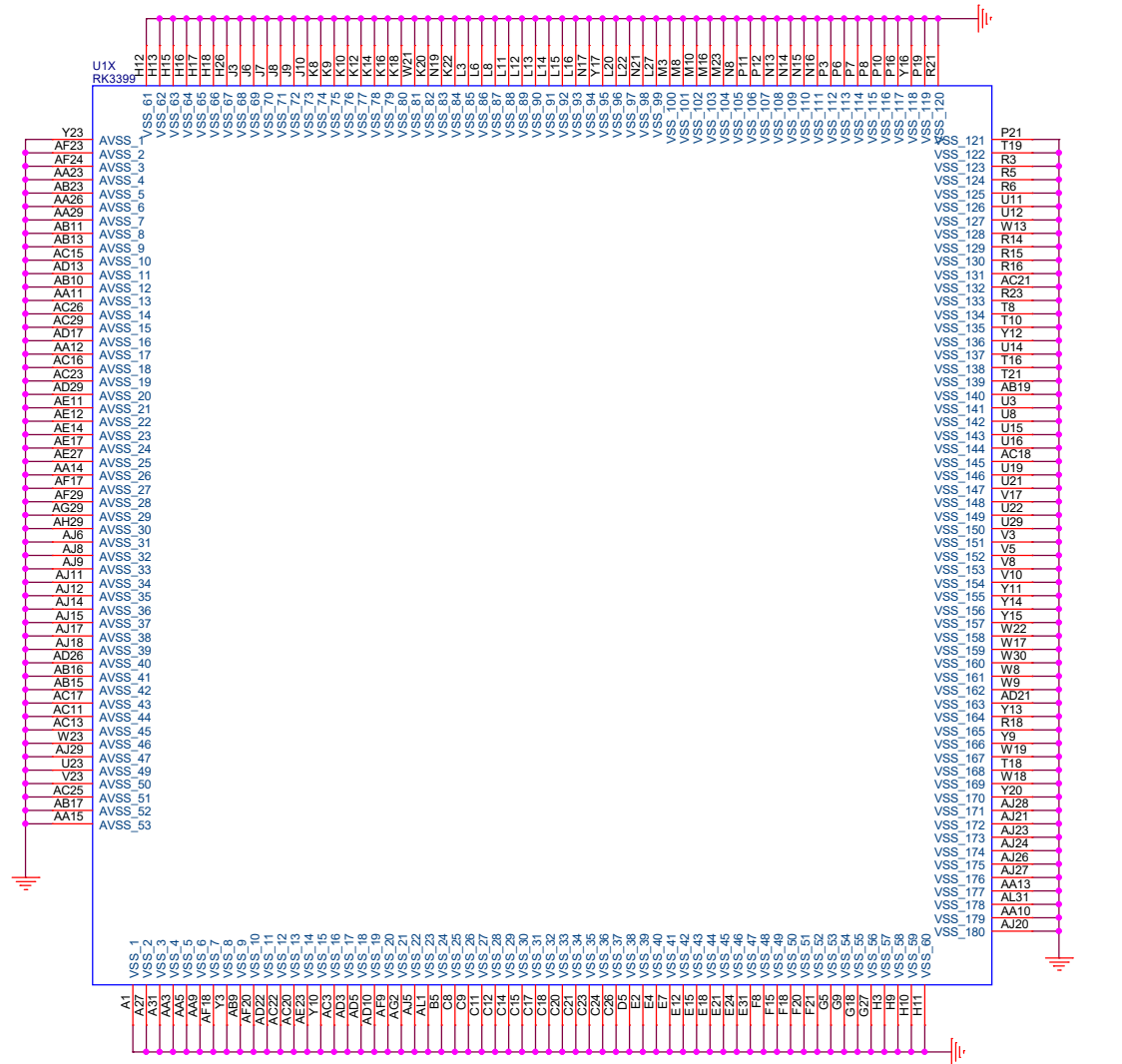
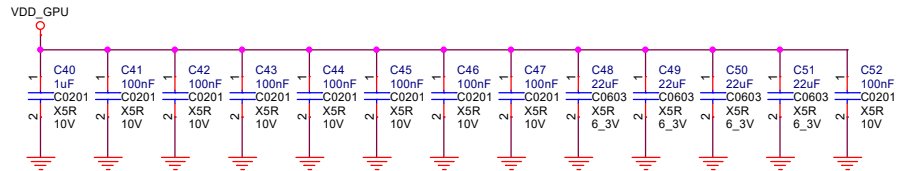
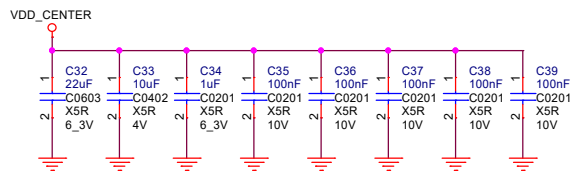
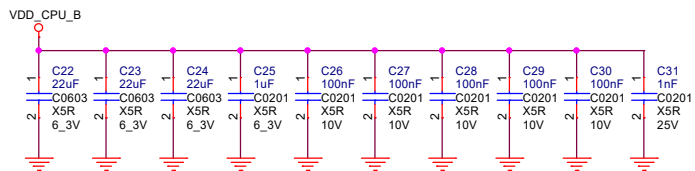
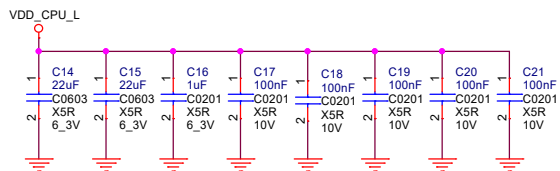
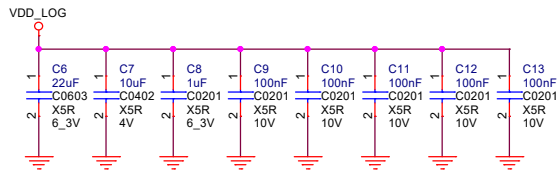
Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuiol_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1	gmac_gpio3abc	3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V (Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V (Default)	VCC_1V5 VCC_3V0	RK808-D VLDO6 RK808-D VLDO8
Part J	APIO5	audio_gpio3d_gpio4a	1.8V (Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V (Default)	VCC_SDIO	RK808-D VLDO4

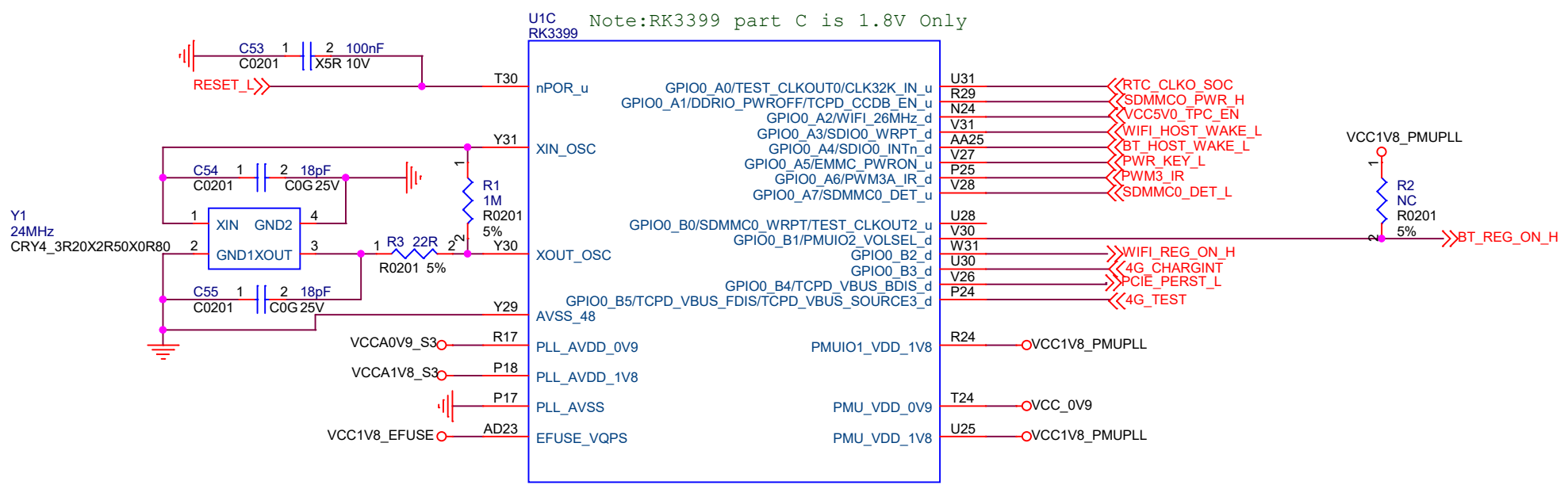
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Note: Power filter CAP please place back of SOC or close to SOC

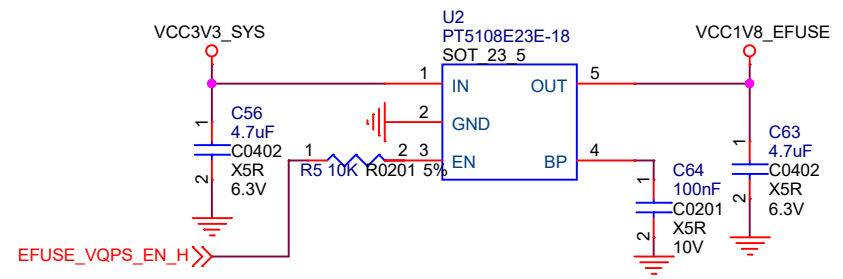
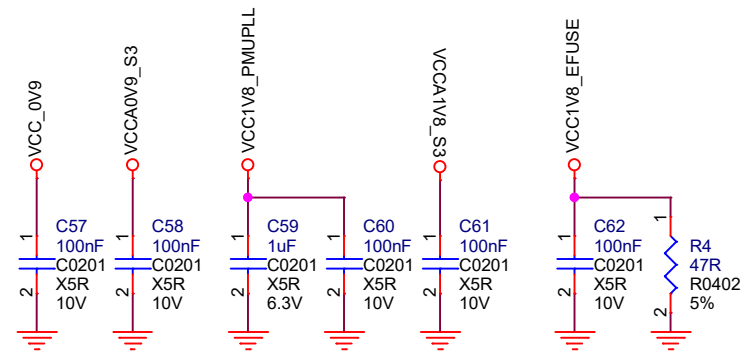


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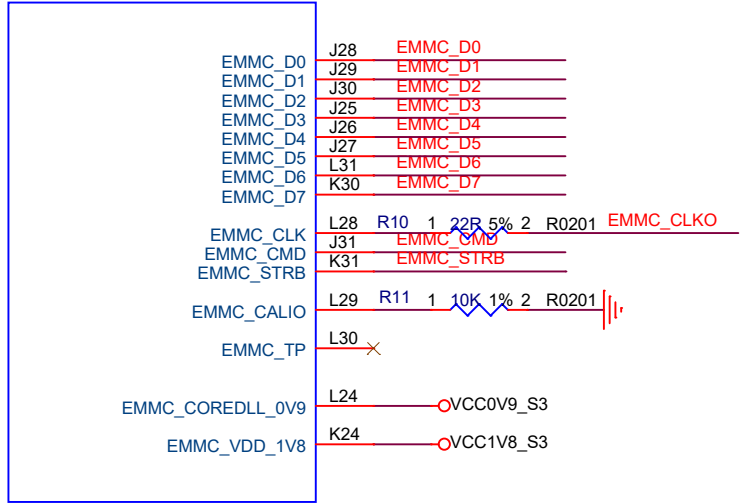
eFUSE (option)

Note:Power for eFUSE Program,it is recommended to reserve on the tooling.It can be deleted if no need.

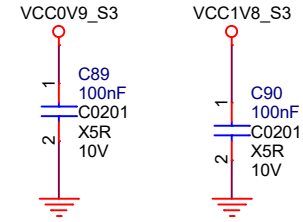
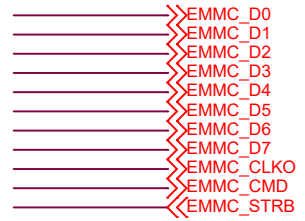


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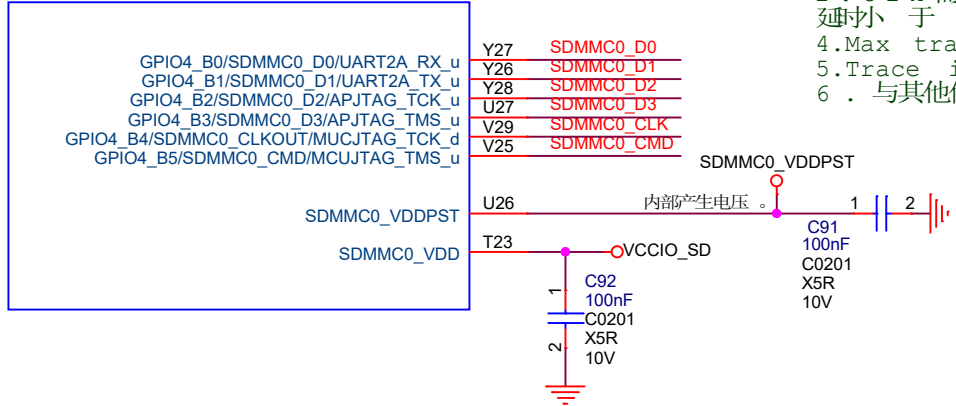
U1H
RK3399



EMMC design rule:
 1. Data[0:7]、cmd strobe 走线为一组，并行走线并包地，组内等长要求为 $\pm 100\text{mil}$ ；
 2. Clk 需要单独走线并包地处理，与 data 间的延时小于 20ps ；
 3. Max trace length $< 3.93\text{ inches}$ ；
 4. Trace impedance $50\text{ohm} \pm 10\%$ ；
 5. 与其他信号间距遵循 3W 原则
 6. R1300 靠近 S 放置



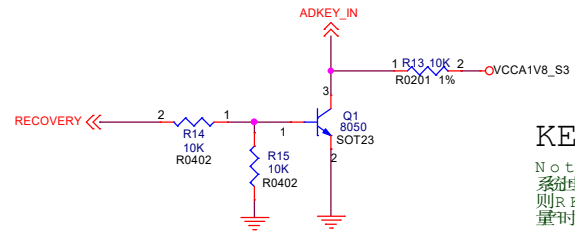
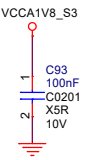
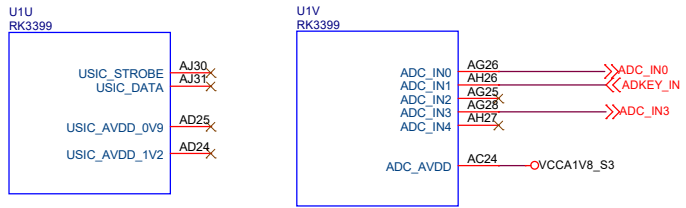
U1F
RK3399



SDMMC design rule:
 1. Data[0:3]、cmd 走线为一组，并行走线并包地，组内等长要求为 $\pm 100\text{mil}$ ；
 2. Clk 需要单独走线并包地处理，与 data 间的延时小于 20ps ；
 4. Max trace length $< 3.93\text{ inches}$ ；
 5. Trace impedance $50\text{ohm} \pm 10\%$ ；
 6. 与其他信号间距遵循 3W 原则



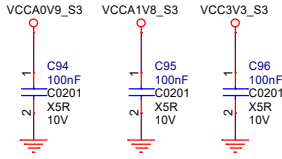
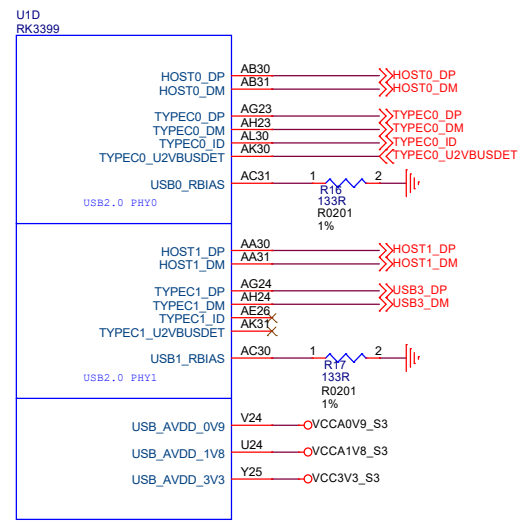
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KEY BAORD

Note:
 系统上电时, 如果 ADKEY_IN 电压为 0V,
 则 RK3399 进入 Recovery 模式;
 量时 R1503, SW1500, ED1 均不用贴片

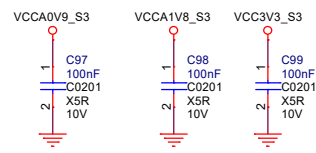
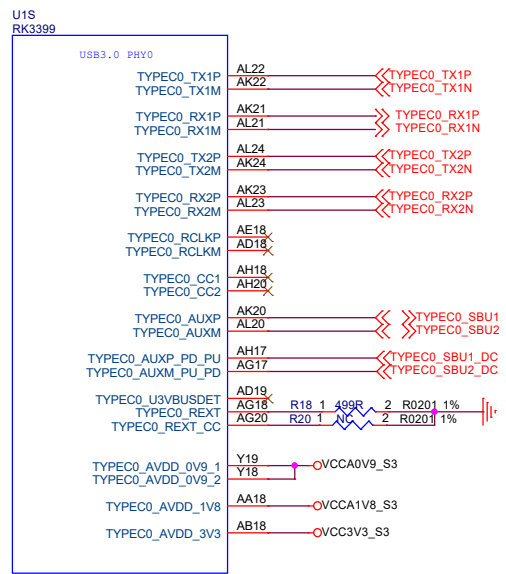
USB2.0



USB2.0 design rule:

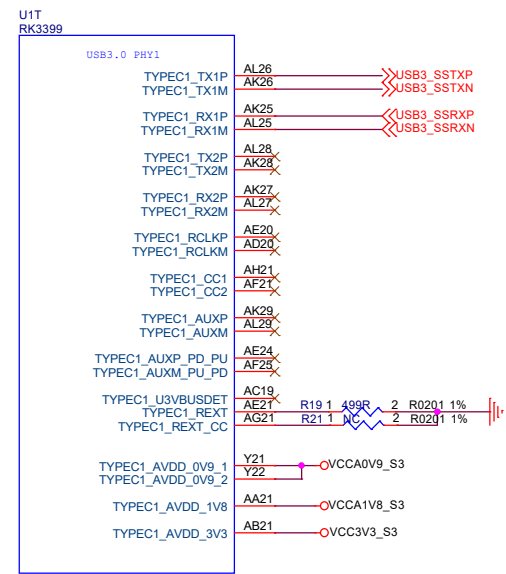
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 6;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间 距遵循3W 原则

USB3.0



USB3.0 design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between TX and RX < 1.6 ns;
- 3.Max trace length < 6 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 90ohm+/-10%;
6. 与其他信号间 距遵循3W 原则

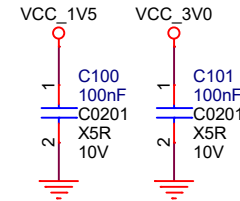
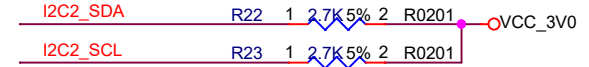
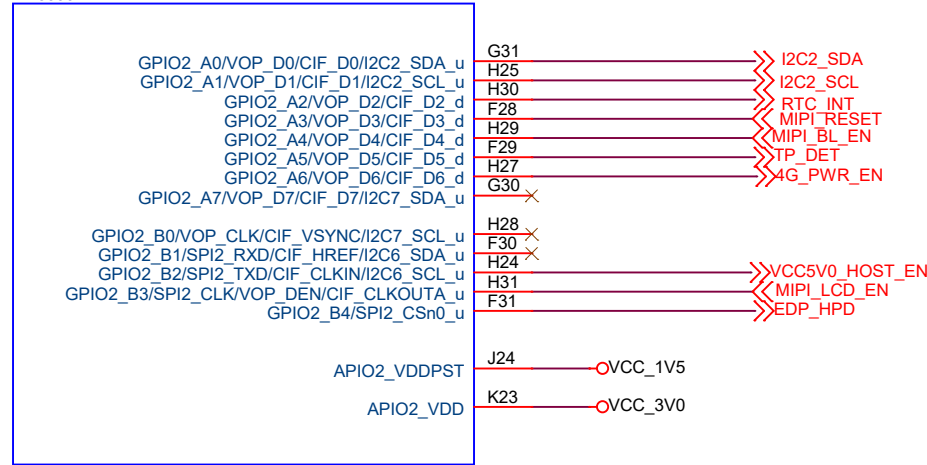


DP design rule:

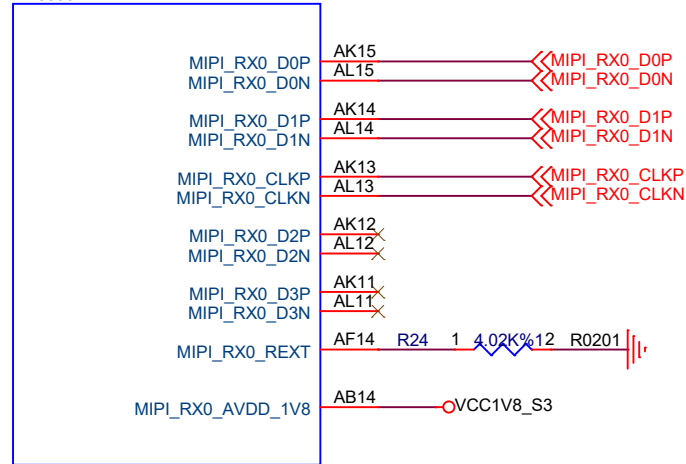
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
5. 与其他信号间 距遵循3W 原则

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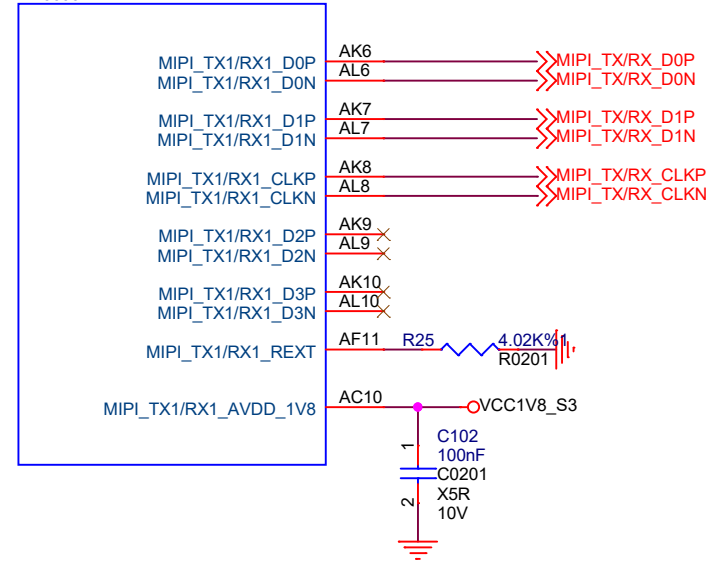
U1L
RK3399



U1R
RK3399

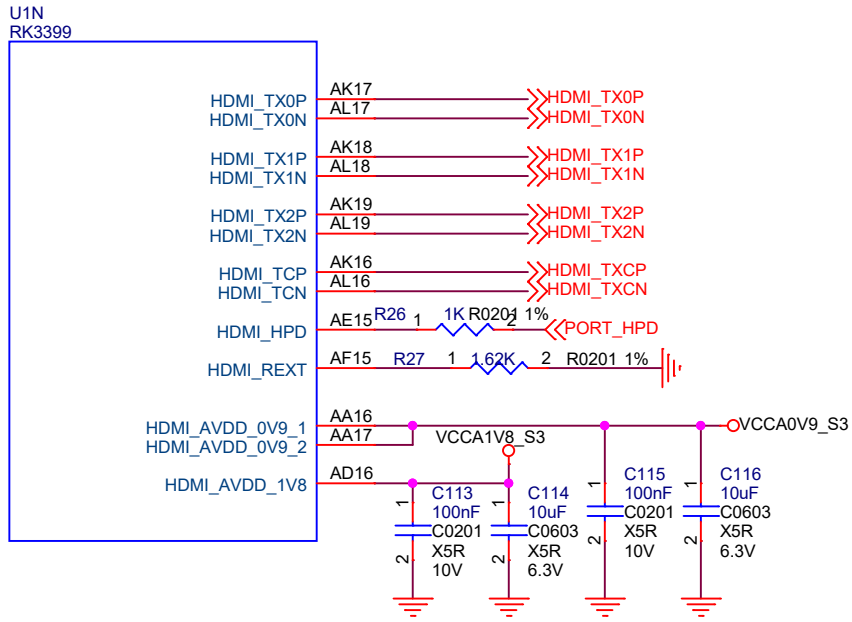


U1P
RK3399



Dual
MIPI
Right

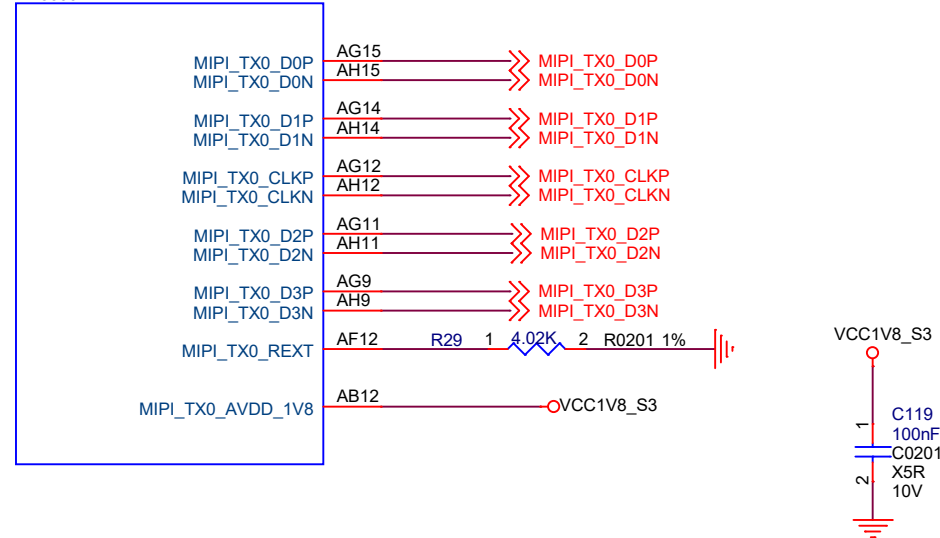
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A4	RK3399 MIPI/GPIO2		1.0		
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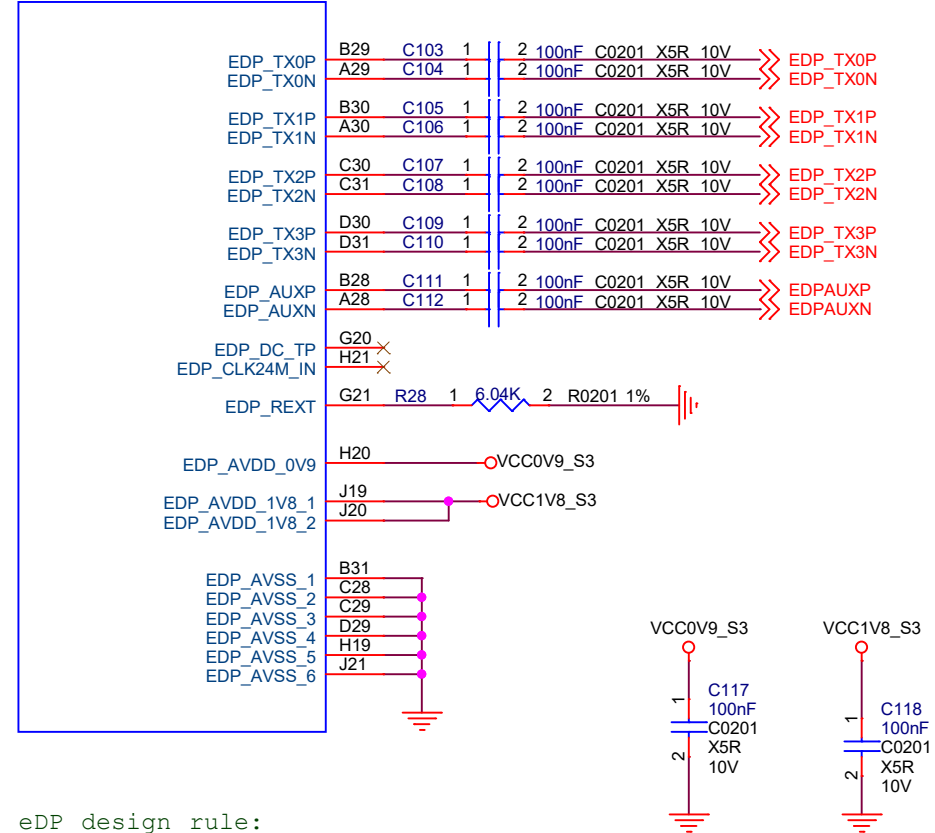
HDMI design rule:

1. Max intra-pair skew < 4 ps;
2. Max length skew between clk and data < 80 ps;
3. Max trace length < 9.8 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循3W原则

U1Q RK3399



U1M RK3399



eDP design rule:

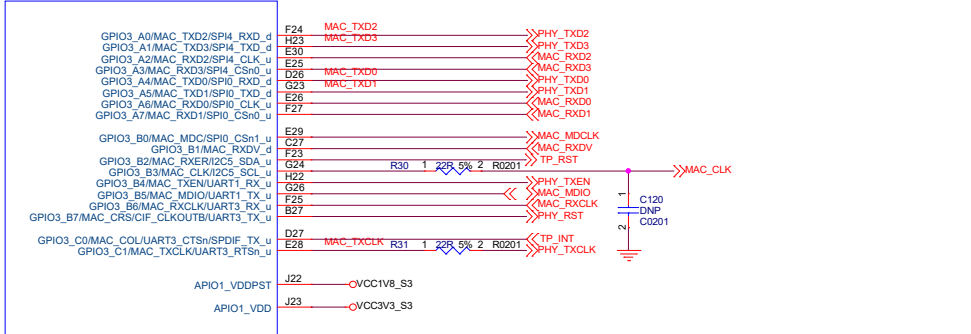
1. Max intra-pair skew < 4 ps;
2. Max trace length < 6 inches;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. 与其他信号间距遵循3W原则

MIPI design rule:

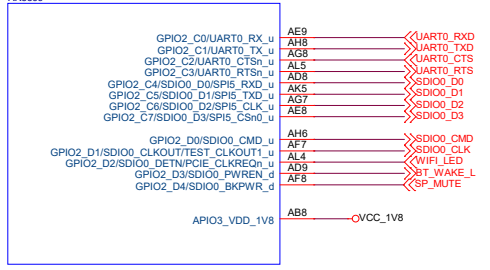
1. Max intra-pair skew < 4 ps;
2. Max length skew between clk and data < 7ps;
3. Max trace length < 7.2 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循3W原则

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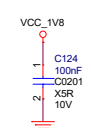
U1I Note:RK3399 part I is 3.3V only



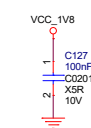
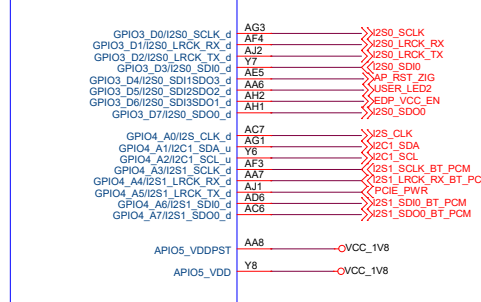
U1G Note:RK3399 part G is 1.8V only



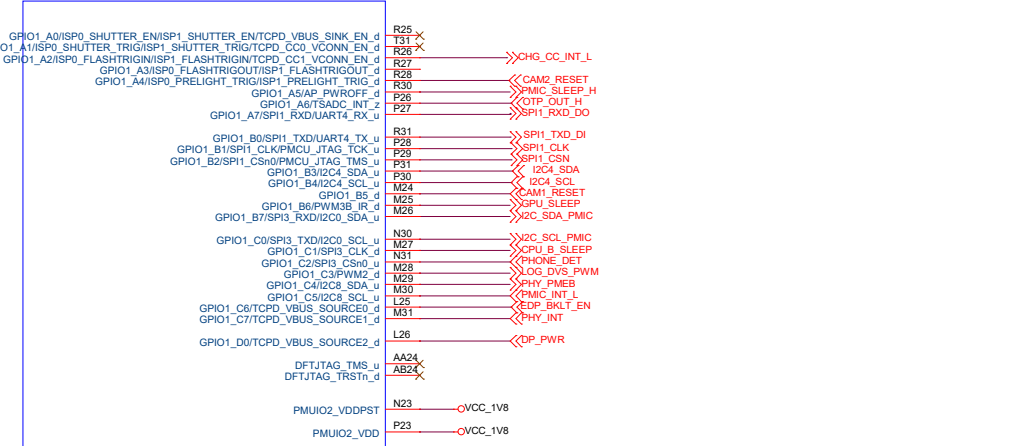
SDIO design rule:
 1. Data[0:3], cmd 数据组, 并行传输, 组内等长要求为 +/-1 0mil;
 2. clk 需单独包地处理, 与 data 的间距 < 20mil;
 4. Max trace length < 3.93 inches;
 5. Trace impedance 50ohm +/- 10%;
 6. 与其他信号间 间距遵循 3W 原则



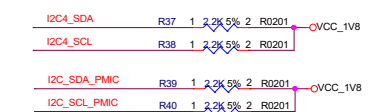
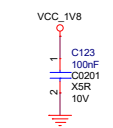
U1J Note:RK3399 part J is 1.8V/3.0V mode



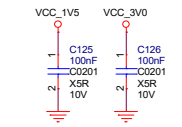
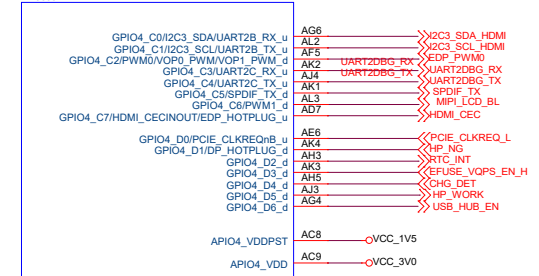
U1E Note:RK3399 part E is 1.8V/3.0V mode



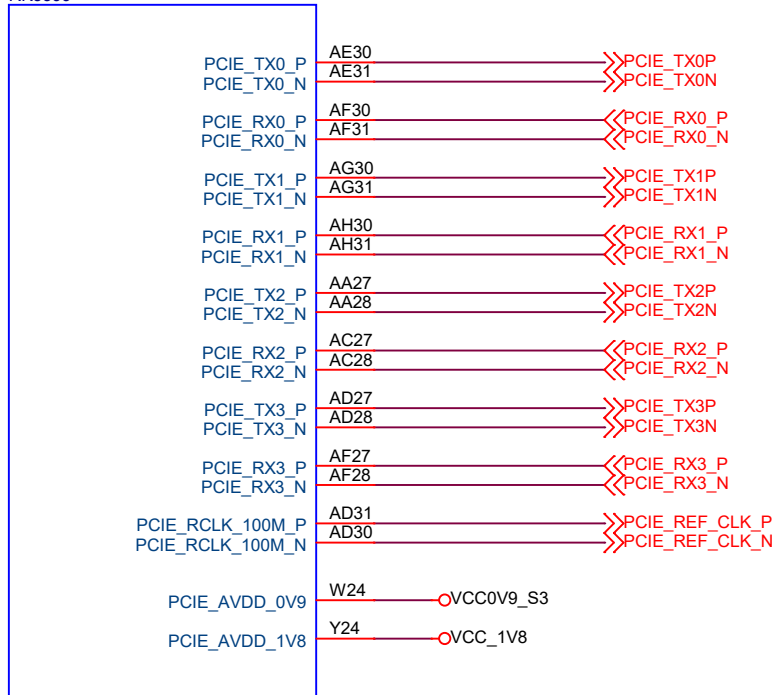
1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V, VDDIO=3.3V
other	3.0V mode: VDDPST=1.5V, VDDIO=3.0V 1.8V mode: VDDPST=1.8V, VDDIO=1.8V



U1K Note:RK3399 part J is 1.8V/3.0V mode

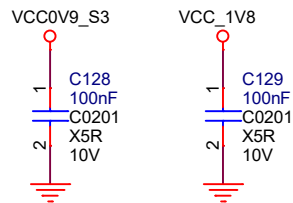


U10
RK3399



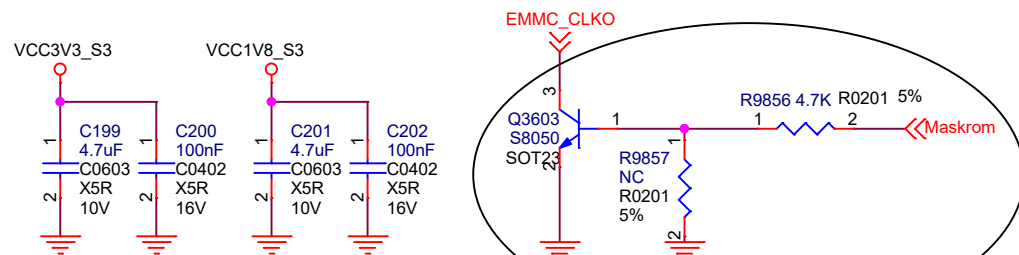
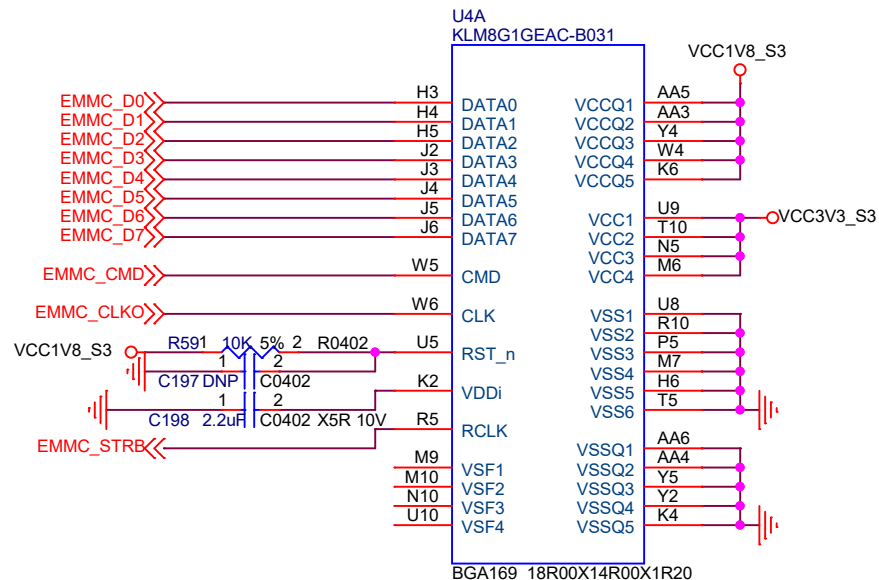
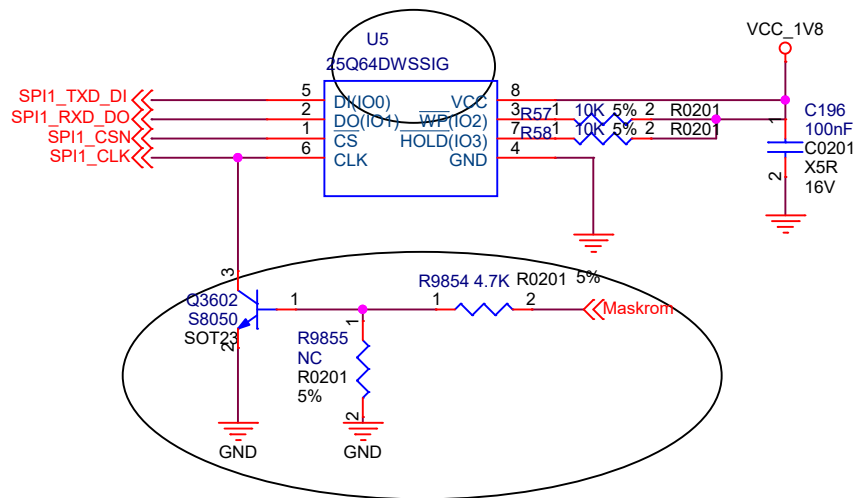
PCIE design rule:

1. Max intra-pair skew < 4ps;
2. Max inter-pair skew < 1.6 ns;
3. Max trace length < 14 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. 与其他信号间距遵循3W原则



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eMMC FLASH



Note: All the Power filter capacitors should be placed close to the power pins of eMMC

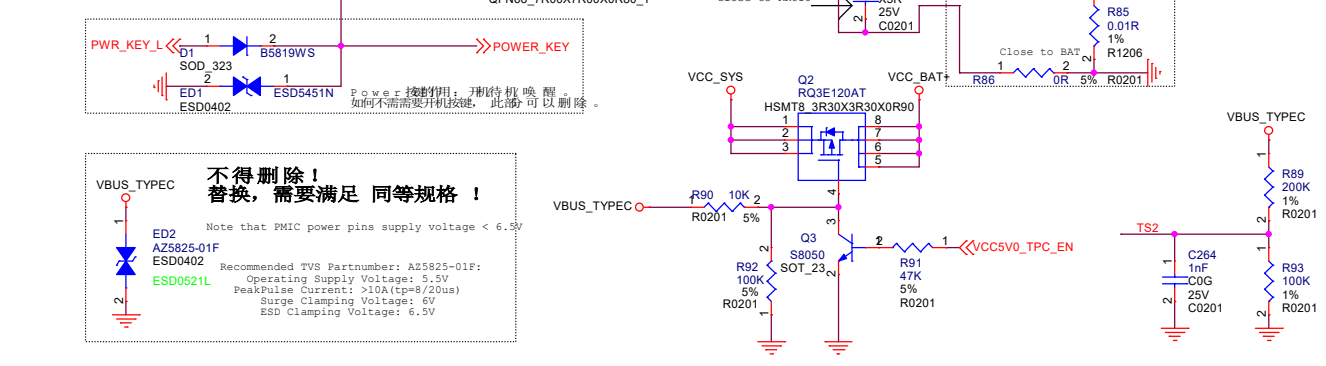
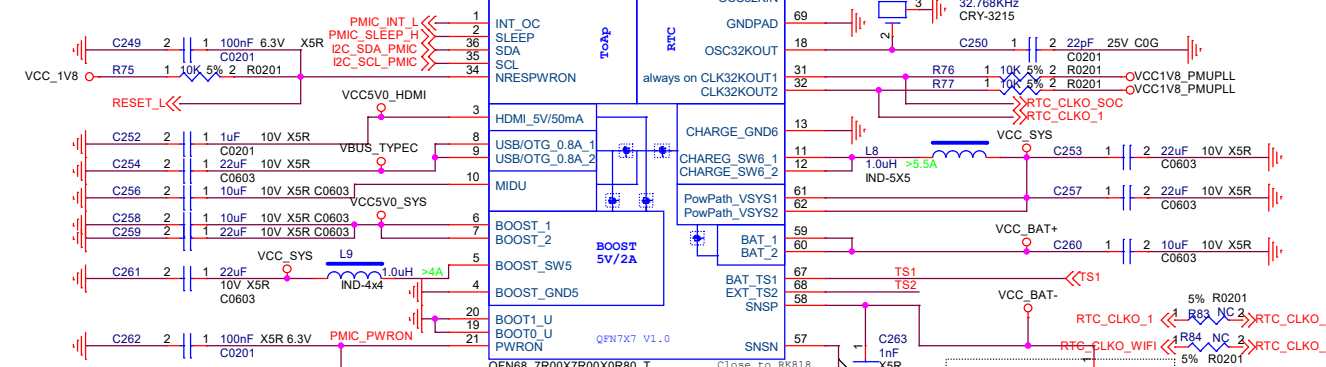
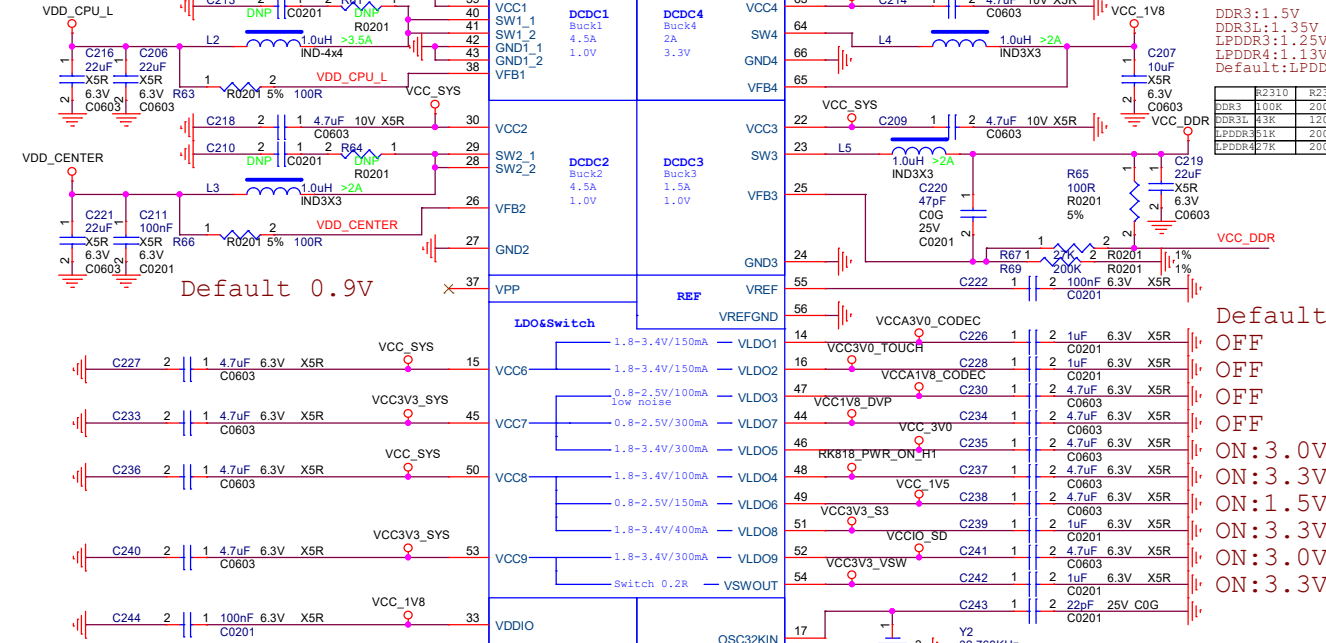
Note:
Reserve TestPoint for firmware update.
If EMMC_CLKO=0V at power-on reset,
then system will enter into Maskrom mode.

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A4	Memory-eMMC/SPI				1.0
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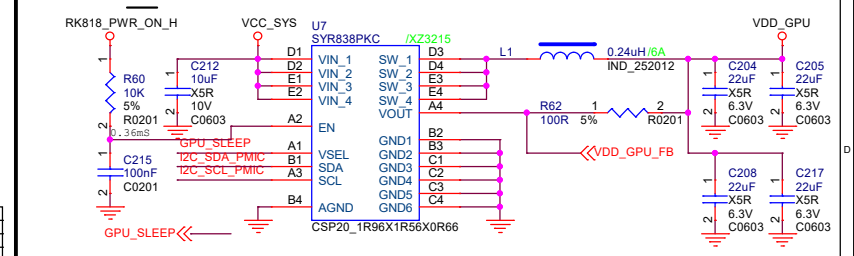
PMIC RK818-3

Default 0.9V

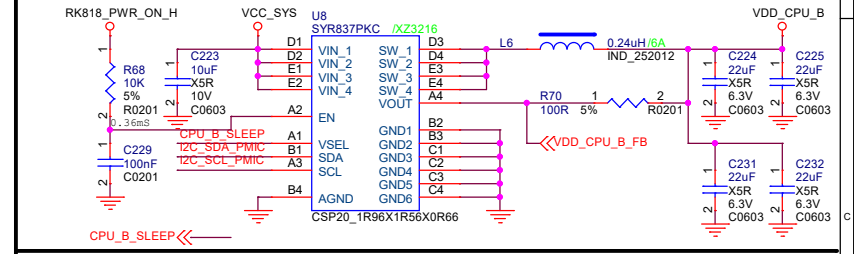
Default 1.8V



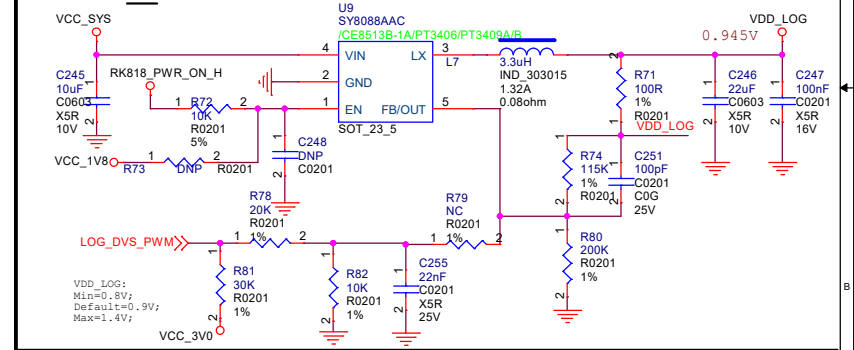
VDD_GPU



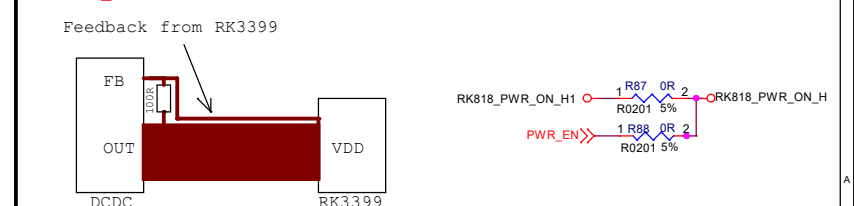
VDD_CPU_B



VDD_LOG

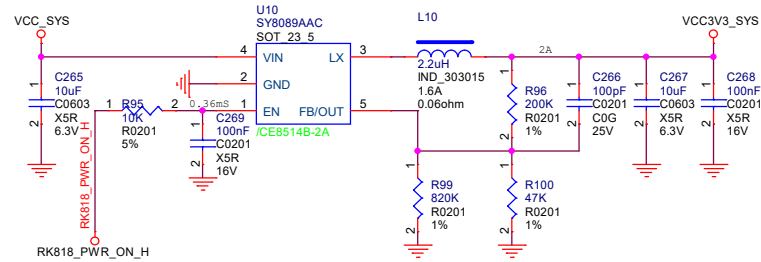


- 如下电源反馈信号的走线，需满足如下方式：
1. VDD_CPU_L
 2. VDD_CENTER
 3. VCC_DDR
 4. VDD_CPU_B
 5. VDD_GPU
 6. VDD_LOG

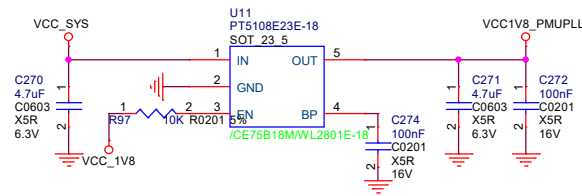


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A3	Power1-RK818-3	1.0	
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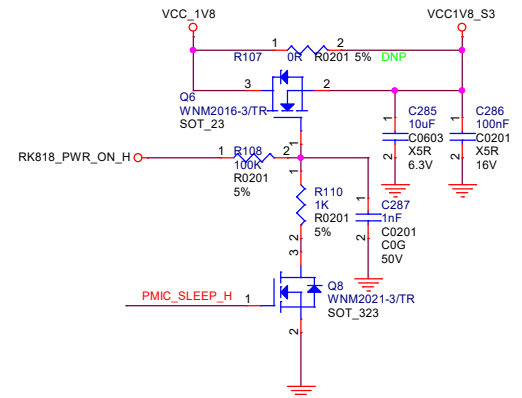
VCC3V3_SYS



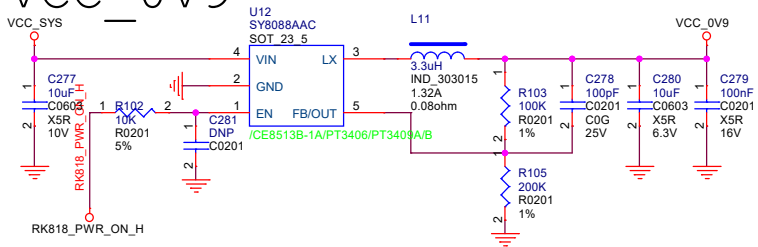
VCC1V8_PMUPLL



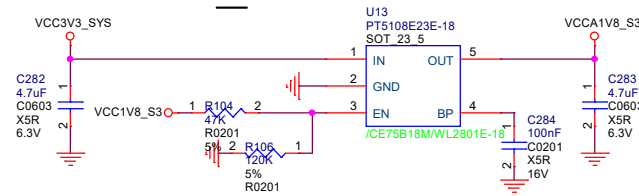
VCC1V8_S3



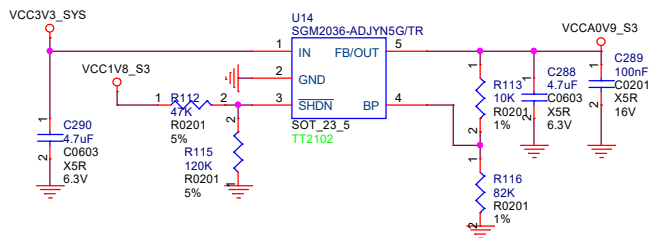
VCC_0V9



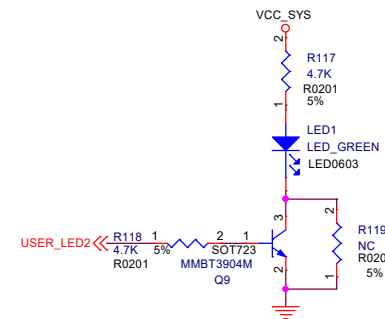
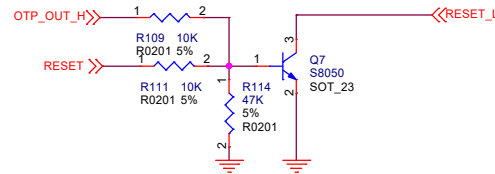
VCCA1V8_S3



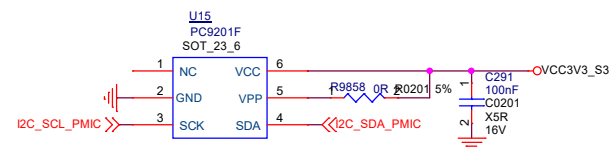
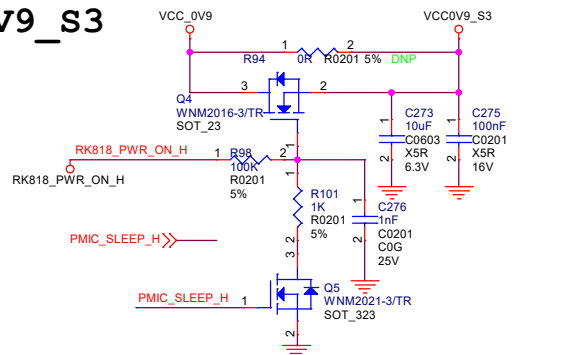
VCCA0V9_S3



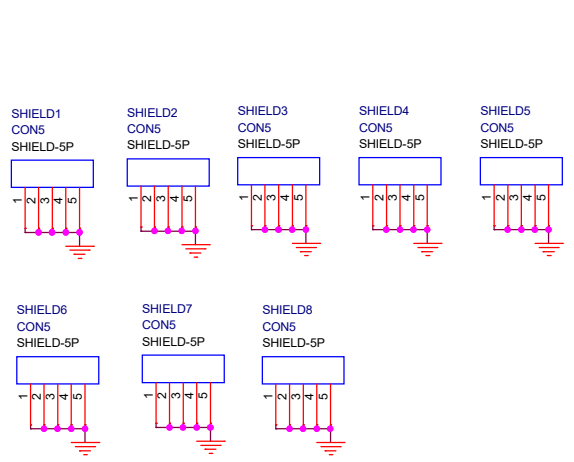
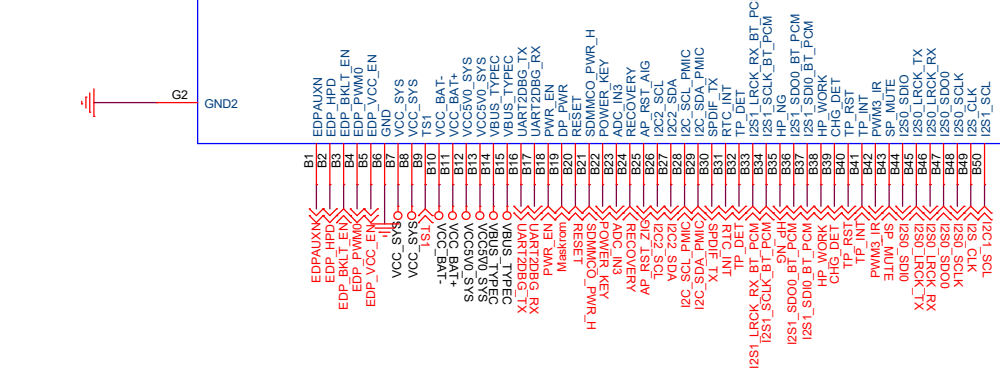
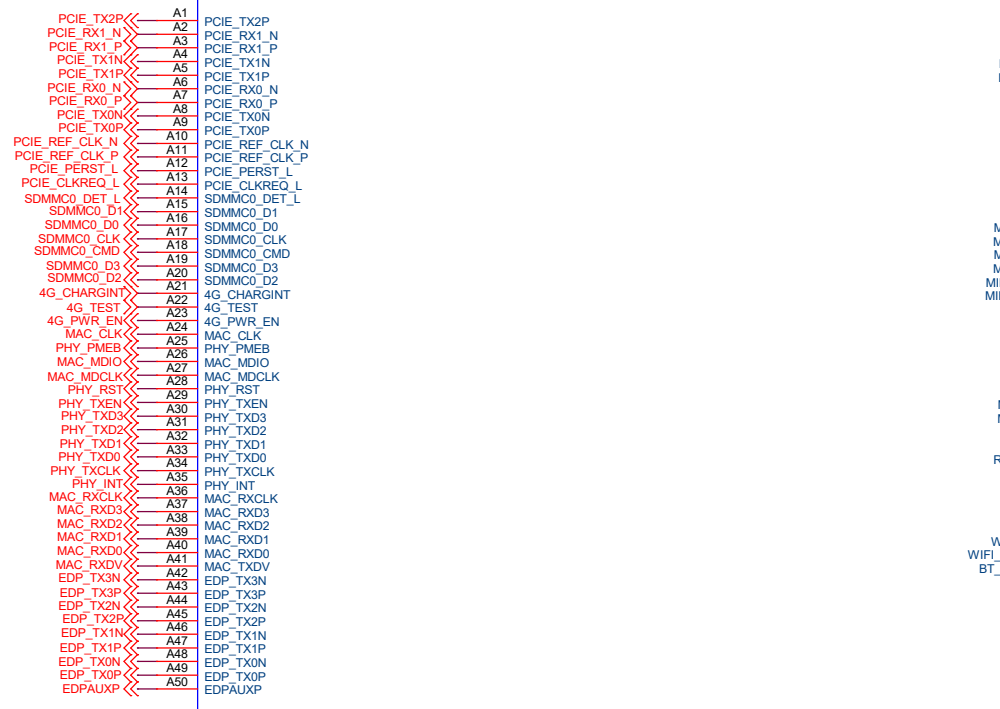
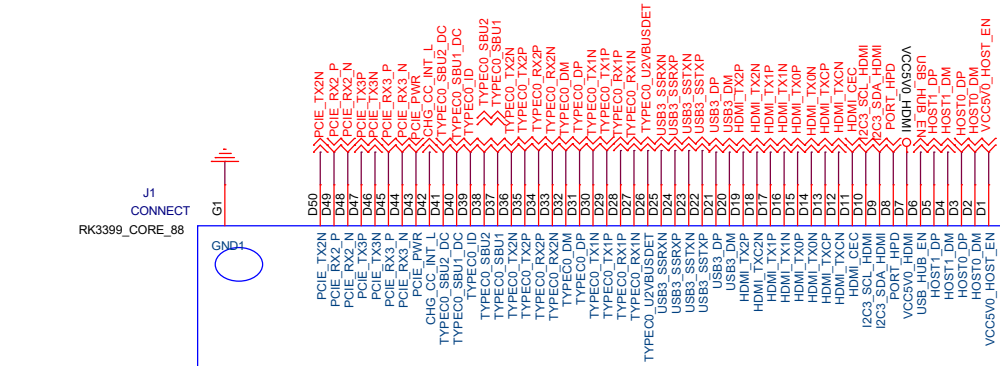
Over-temperature Protection



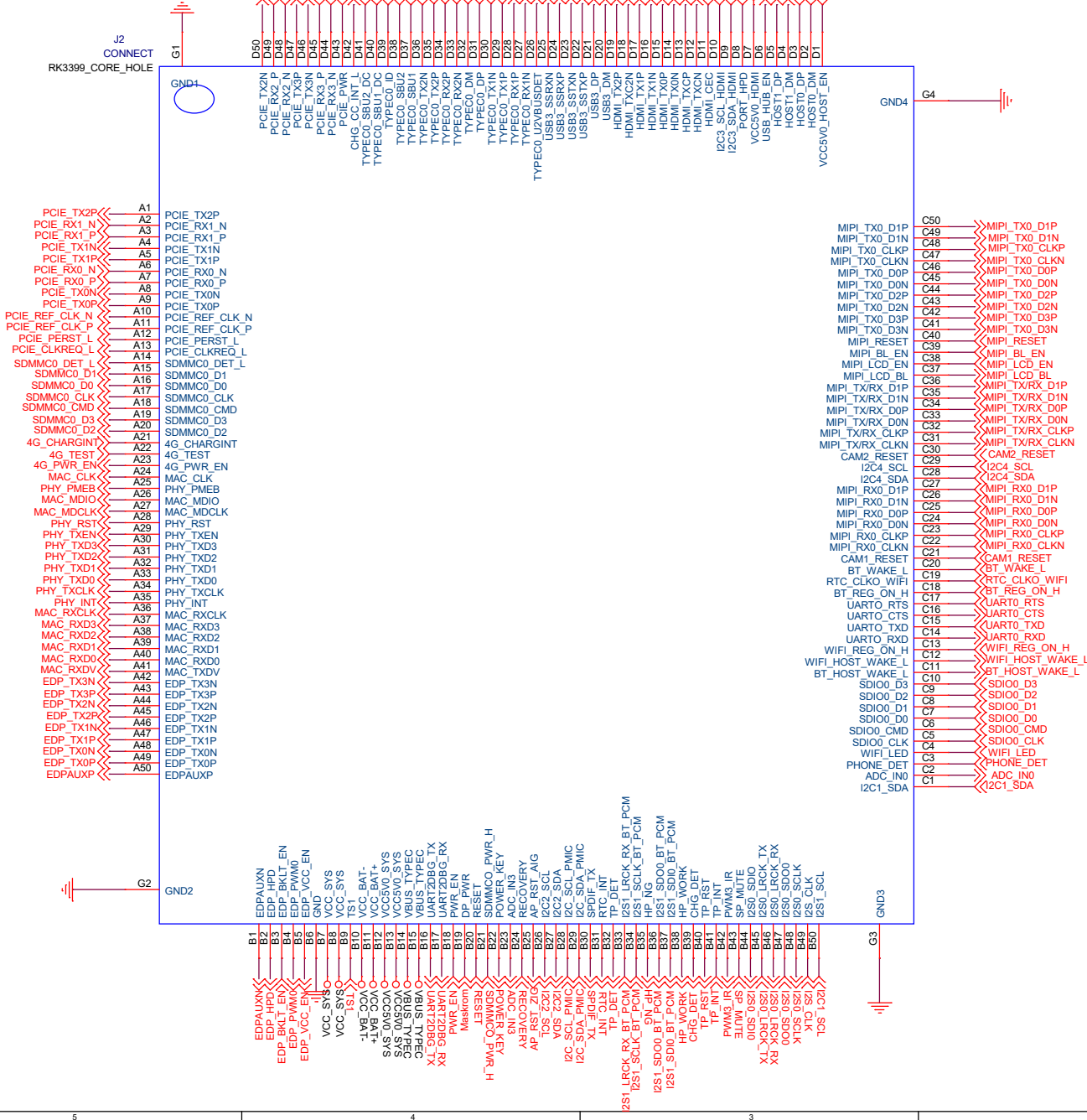
VCC0V9_S3



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