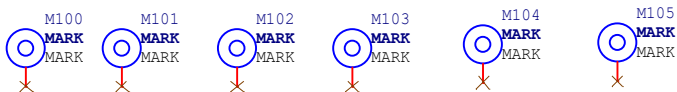
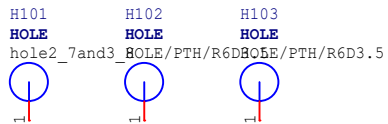
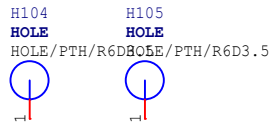


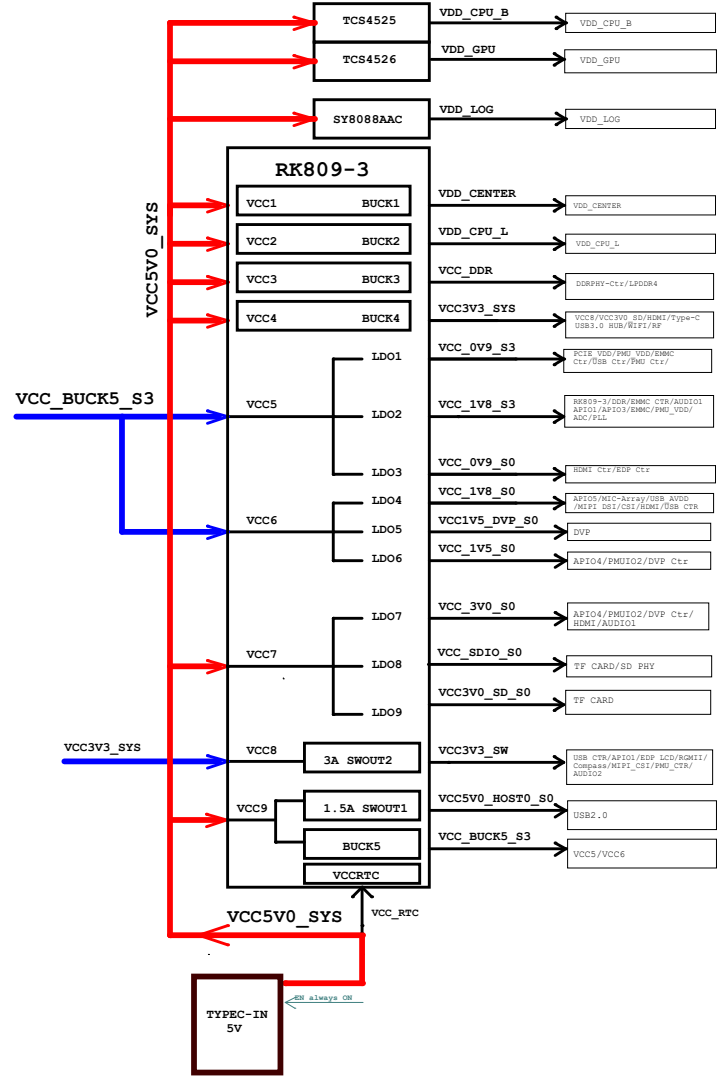
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- 02.Power Diagram and Sequence-2
- 03.I2C Map and MIPI Map
- 04.IO Power Domain Map
- 05.RK3399 Power/GND
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- 27.DP to HDMI



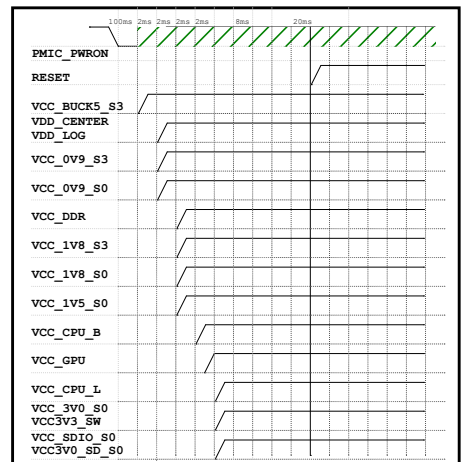
Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 01.Cover Page	1.2
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RK3399 POWER DIAGRAM



RK809-3 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC5V0_SYS	BB785D(AA)	0	5V		ON	ON	
VCC_BUCK5_S3	BUCK5(2.5A)	1	3.3V		ON	ON	
VDD_LOG	REG10(F0E8/1A)	2	0.9V		ON	ON	
VDD_CENTER	BUCK1(2.5A)	2	0.9V		ON	OFF	
VCC_CPU_B	LDO1(400mA)	2	0.9V		ON	OFF	
VCC_0V9_S3	LDO3(400mA)	2	0.9V		ON	ON	
VCC_DDR	BUCK3(1.5A)	3	1.11V		ON	ON	
VCC_1V8_S3	LDO4(400mA)	3	1.8V		ON	ON	
VCC_1V8_S0	LDO4(400mA)	3	1.8V		ON	OFF	
VCC_1V5_S0	LDO4(400mA)	3	1.5V		ON	OFF	
VCC_CPU_L	REG10(F0E8/1A)	3B	0.9V		ON	OFF	6A
VDD_CPU_B	REG10(F0E8/1A)	3A	0.9V		ON	OFF	6A
VCC_CPU_L	BUCK2(2.5A)	4	0.9V		ON	OFF	
VCC_3V0_S0	LDO7(400mA)	5	3.0V		ON	OFF	
VCC_3V3_SW	SWO2(1.5A)	5	3.3V		ON	OFF	
VCC5V0_SYS	BUCK1(1.5A)	5	3.3V		ON	OFF	
VCC_SDIO_S0	LDO8(400mA)	5	3.3V		ON	OFF	
VCC5V0_HOST0_S0	LDO8(400mA)	5	3.3V		ON	OFF	
VCC1V5_DVP_S0	LDO5(400mA)	5	1.5V		OFF	OFF	
VCC3V0_HOST0_S0	SWO2(1.5A)		3V		OFF	OFF	



I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK809	0x1b	PMIC	100kHz, 400KHz
					Silergy SYR837PKC	0x40	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
					Silergy SYR838PKC	0x41	DC-DC BUCK	100kHz, 400KHz, 3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8				
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	RESERVE					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_HDMI I2C_SCL_HDMI	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_TYPEC I2C_SCL_TYPEC	VCC_1V8				
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	N/A					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					



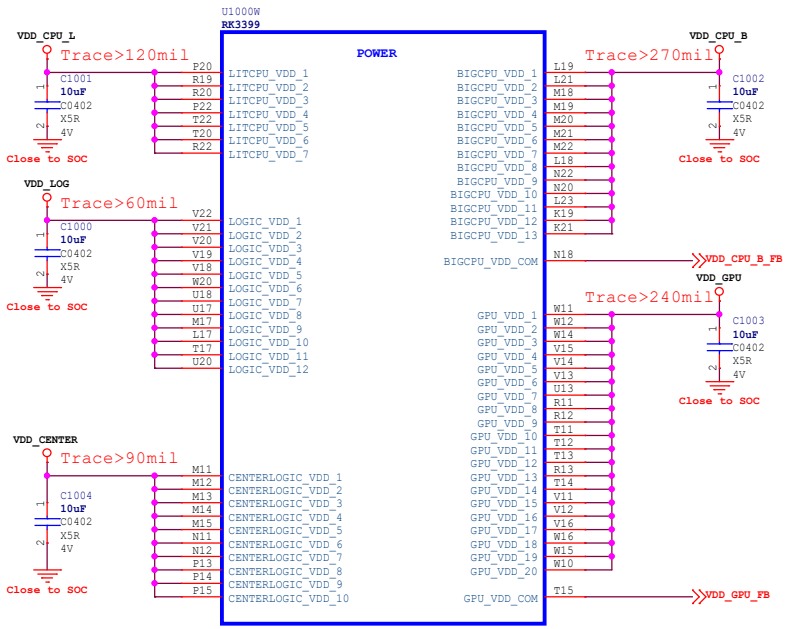
Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 03.I2C Map and MIPI Map	1.2
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IO Power Domain Map

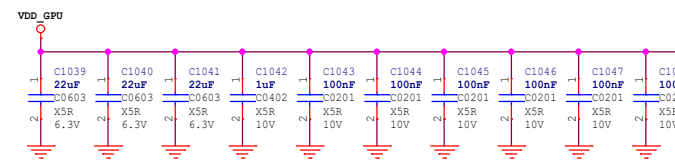
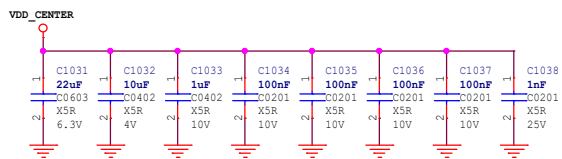
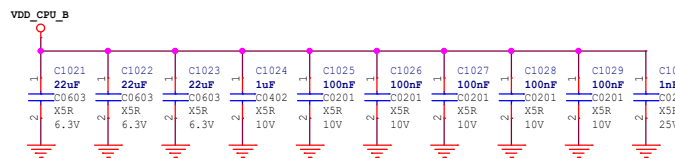
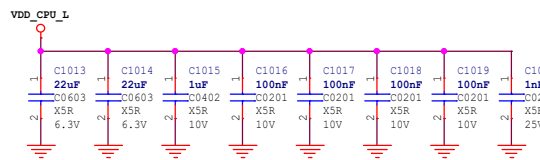
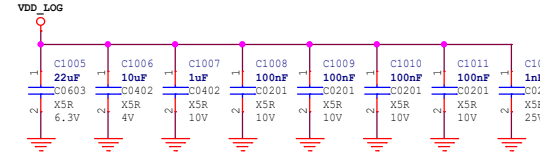
IO Domain	Pin No.	Support of IO Voltage			Default Actual assigned IO Domain Voltage			Notes
		1.8V	3.0V	3.3V	Net of IO Supply	Power Source	Default Voltage	
PMUIO1	GPIO0abcd	✓	✗	✗	VCCA_1V8	RK809-Ido2	1.8V	
PMUIO2	GPIO1abcd	✓	✓	✗	VCC_1V8	RK809-Ido2	1.8V	
APIO1	GPIO3abc	✗	✗	✓	VCC_1V8 VCC3V3_LAN	RK809_BUCK4	1.8V 3.3V	
APIO2	GPIO2ab	✓	✓	✗	VCC_1V8	RK809-Ido7	3v	
APIO3	GPIO2cd	✓	✗	✗	VCC_1V8	RK809-Ido2	1.8V	
APIO4	GPIO4cd	✓	✓	✗	VCC_1V5 VCC_3V0	RK809-Ido7	1.5V 3.0V	
APIO5	GPIO4a	✓	✓	✗	VCC_1V8	RK809-Ido4	1.8V	
SDMMC0	GPIO4b	✓	✓	✗	VCCIO_SD	RK809-Ido8	1.8/3.0V auto	



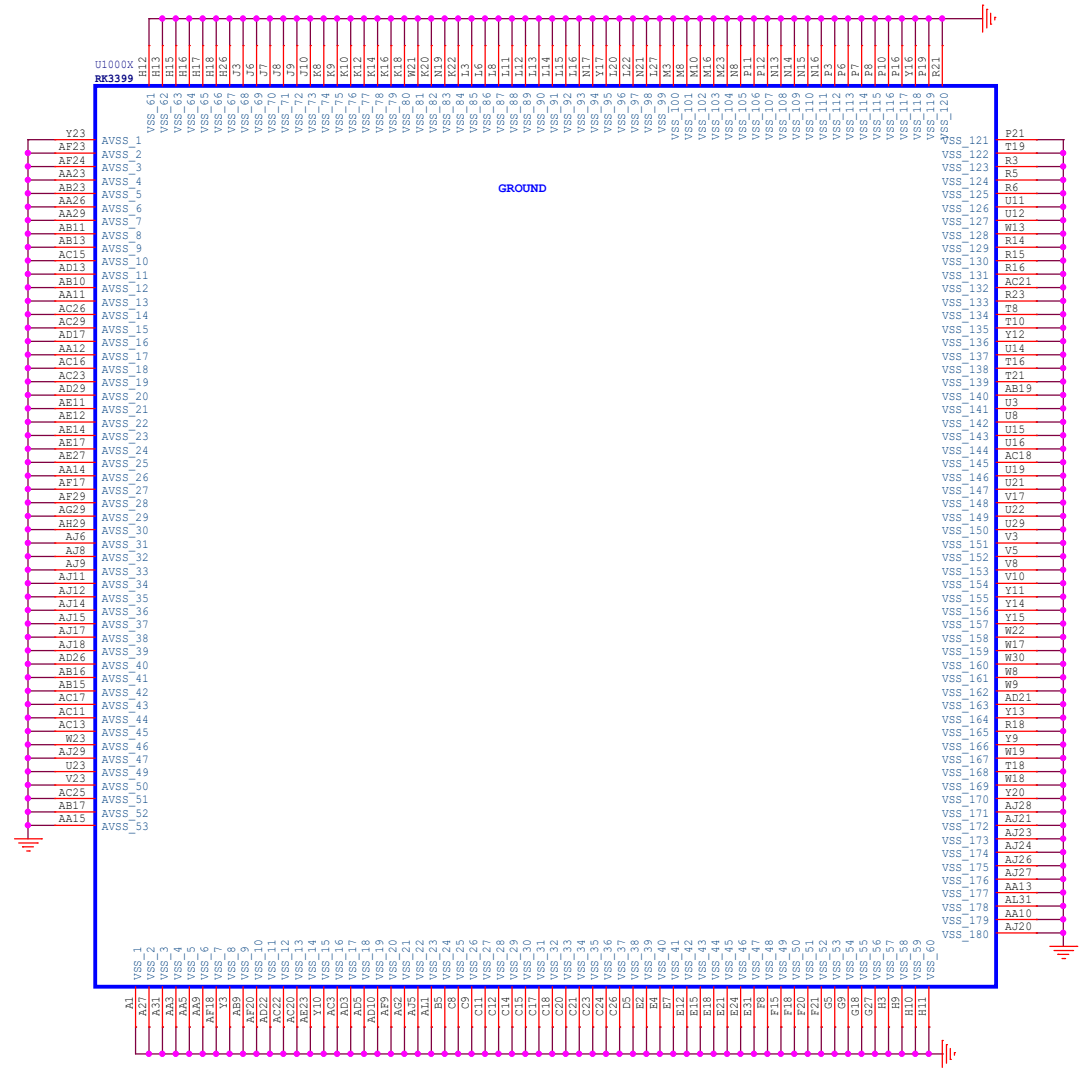
Power



Place:All the Power filter capacitors should be placed close to the power pins of RK3399

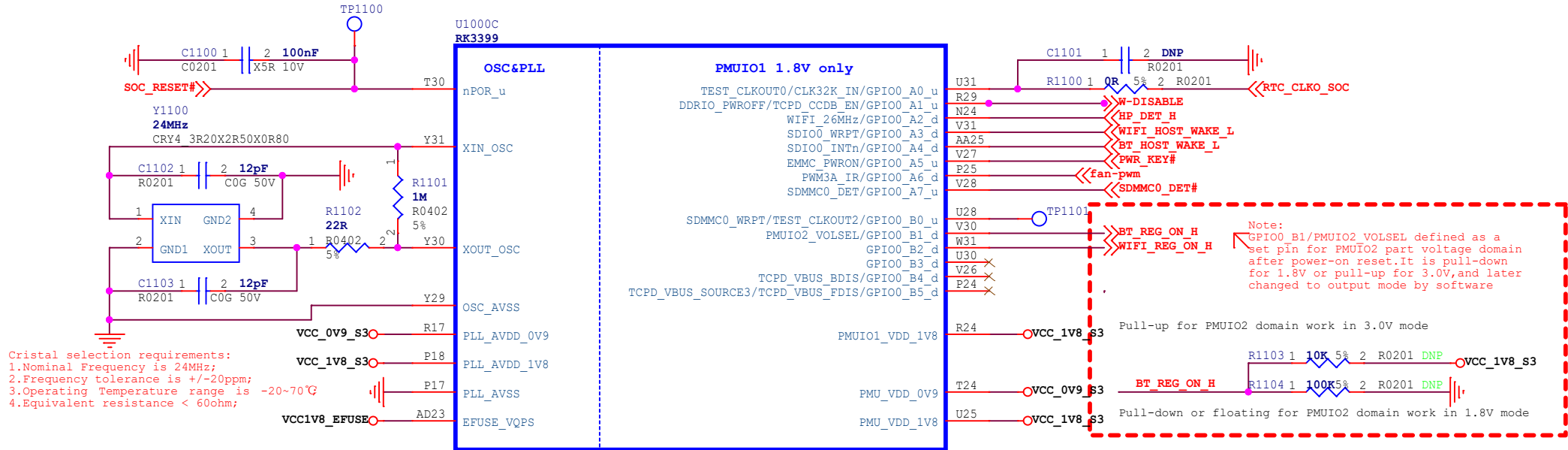


Ground

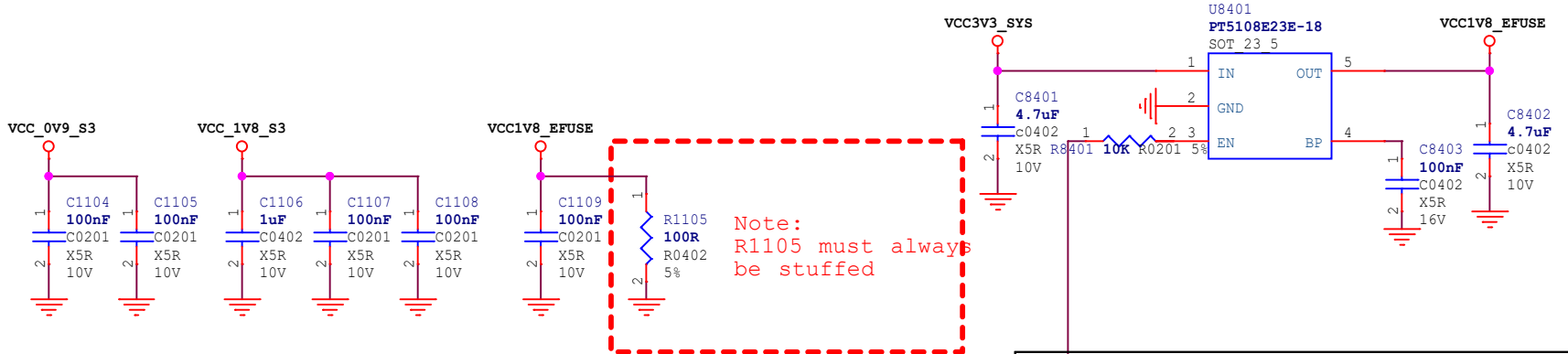


Size	Title: ROCK PI 4C Plus	REV
A3	Page Name: 05.RK3399 Power/GND	1.2
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OSC/PLL/PMUIO1



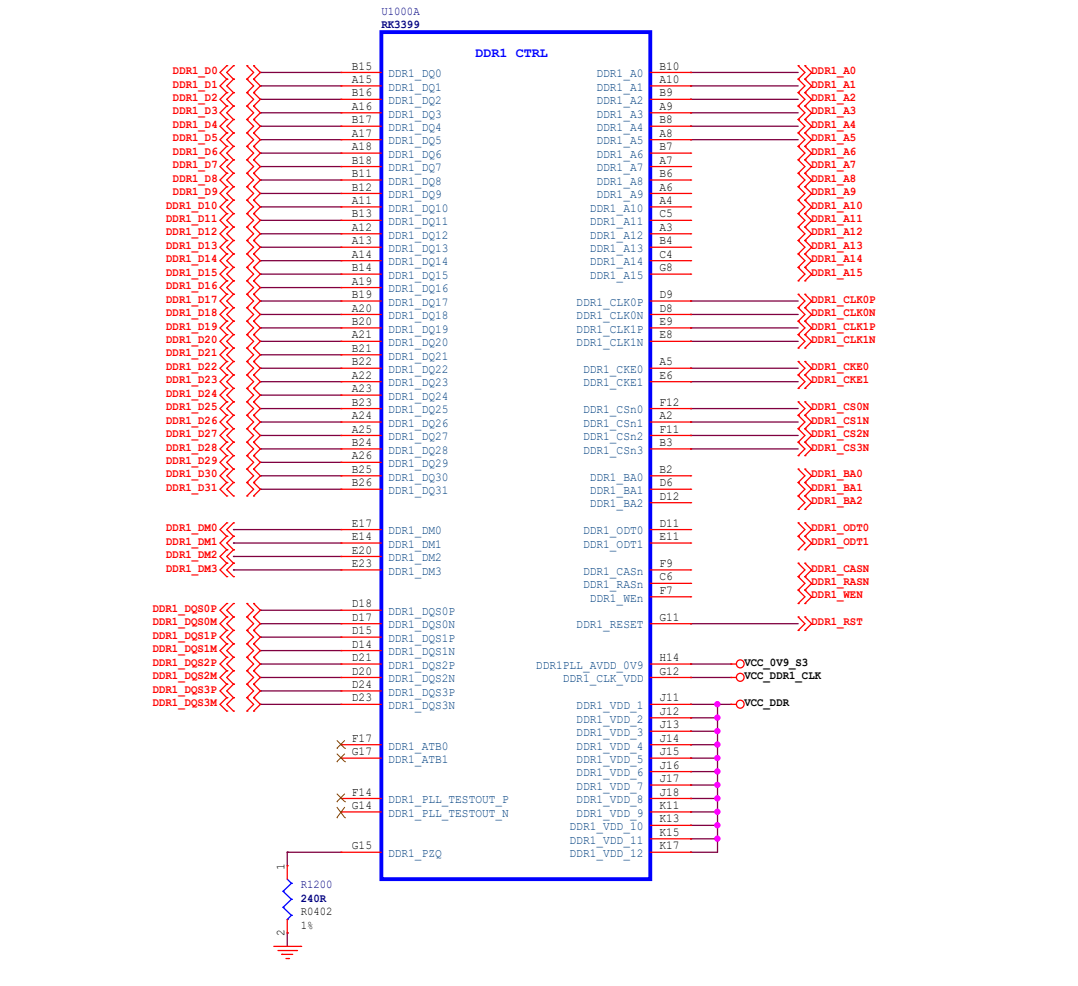
Crystal selection requirements:
 1. Nominal Frequency is 24MHz;
 2. Frequency tolerance is +/-20ppm;
 3. Operating Temperature range is -20~70°C
 4. Equivalent resistance < 60ohm;



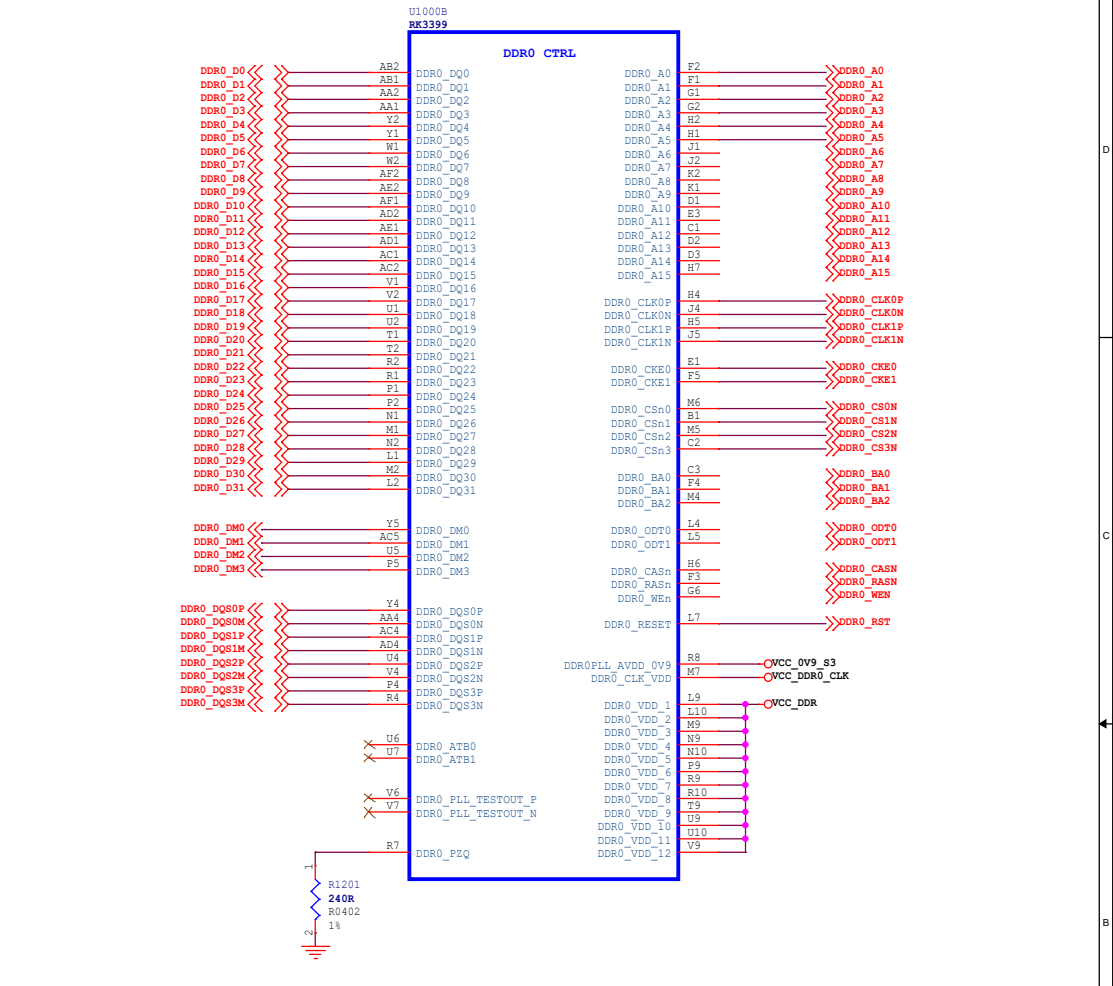
Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
 所有电源去耦电容必须靠近3399电源管脚放置。

Size	Title:	ROCK PI 4C Plus	REV
A4	Page Name:	06.RK3399 PMU Controller	1.2
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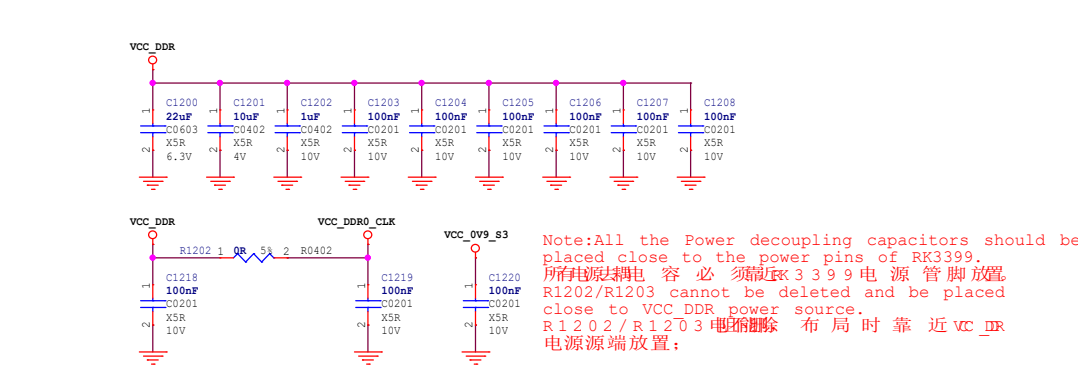
DDR1 Controller



DDR0 Controller

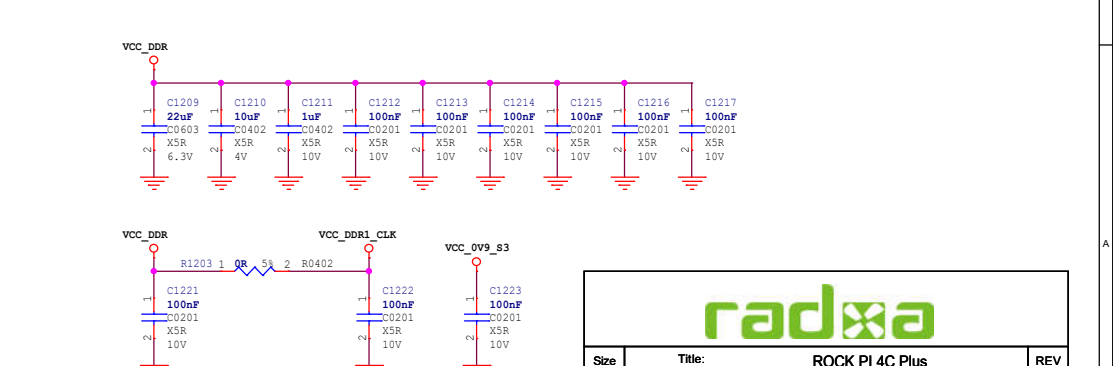


DDR1 Power Decoupling



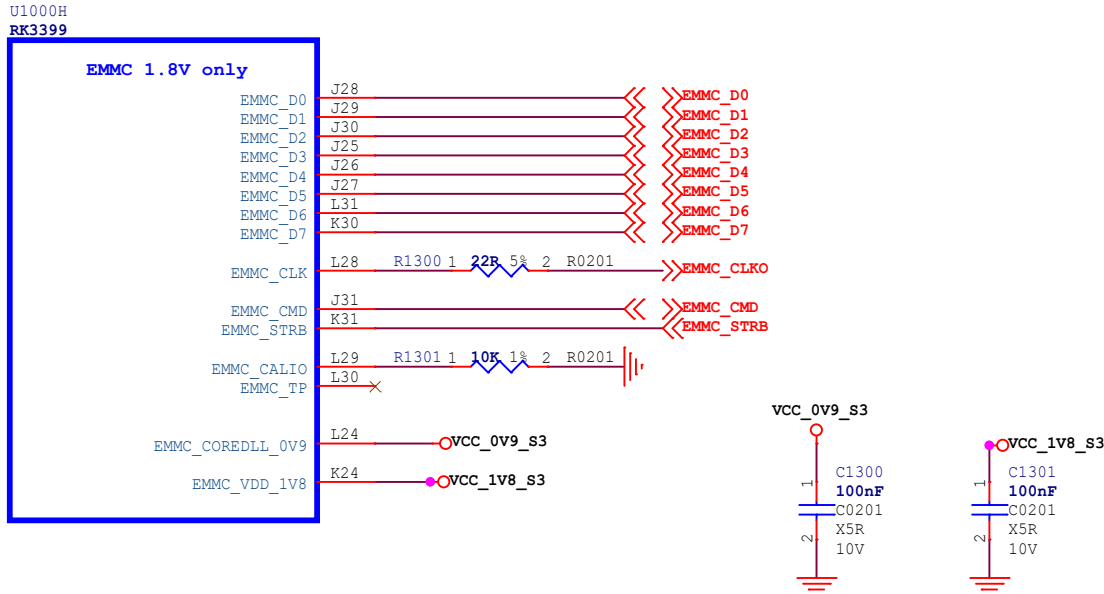
Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
 所有电源去耦电容必须靠近3399电源管脚放置。
 R1202/R1203 cannot be deleted and be placed close to VCC DDR power source.
 R1202/R1203 电路删除 布局时靠近 VCC_DDR 电源源端放置:

DDR0 Power Decoupling



Size	Title: ROCK PI 4C Plus	REV
A3	Page Name: 07.RK3399 DRAM Controller	1.2
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eMMC Controller



Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
所有电源去耦电容必须靠近3399电源管脚放置。

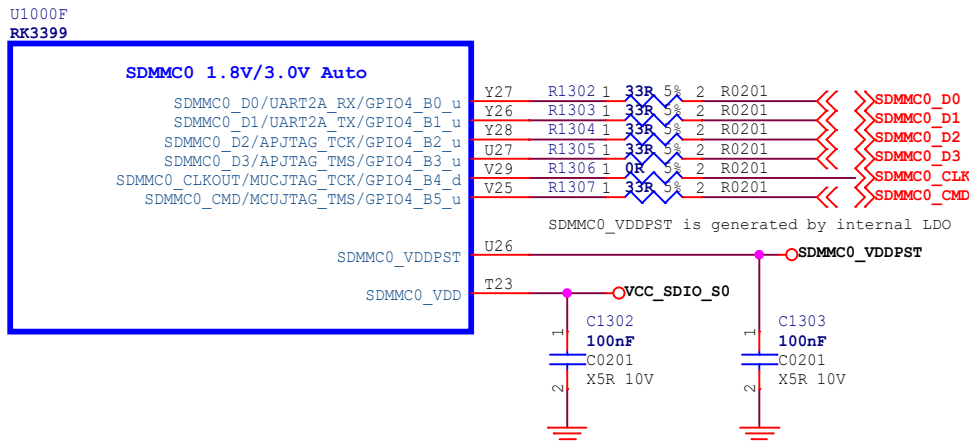
EMMC design rules:

1. Data[0:7], CMD and Strobe lines routing parallel as a group, and be isolated with other signals by GND line, the skew between group <30ps;
2. Clk should be isolated with other signals by GND line; The skew between data signals <20ps;
3. Max trace length < 3.93inches;
4. Trace impedance 50ohm+/-10%;
5. The distance between other signals follows the 3W rule;
6. R1300 should be place close to RK3399;

EMMC 信号设计规则

1. Data[0:7]、CMD和Strobe整体并行走线并包地隔离，组内偏移小于20ps；
2. CLK单独走线与数据信号的偏移小于20ps；
3. 线长小于3.93英寸；
4. 阻抗控制在50ohm+-10%；
5. 信号与其他信号的可距遵循3W原则；
6. R1300靠近RK3399P0201；

SDMMC Controller



Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
所有电源去耦电容必须靠近3399电源管脚放置。

SDMMC design rules:

1. Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signals by GND line, the skew between group <30ps;
2. Clk should be isolated with other signals by GND line; The skew between data signals <20ps;
3. Max trace length < 3.93inches;
4. Trace impedance 50ohm+/-10%;
5. The distance between other signals follows the 3W rule;

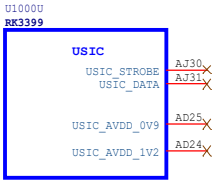
SDMMC 信号设计规则

1. Data[0:3]和CMD整体并行走线并包地隔离，组内偏移小于30ps；
2. CLK单独走线与数据信号的偏移小于20ps；
3. 线长小于3.93英寸；
4. 阻抗控制在50ohm+-10%；
5. 信号与其他信号的可距遵循3W原则；

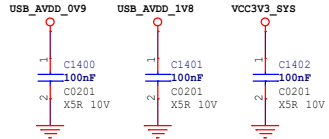
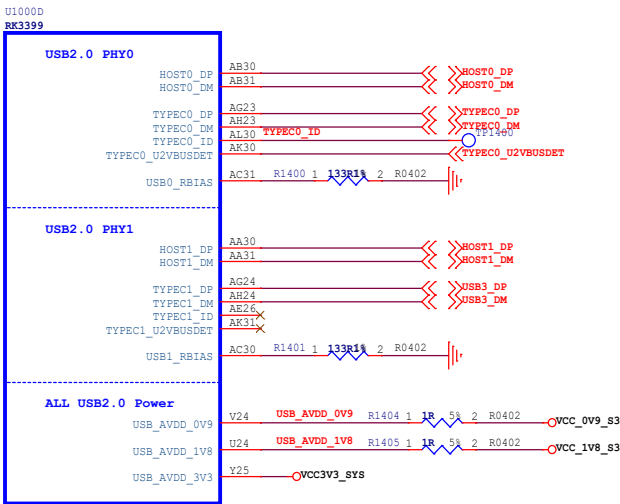


Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 08.RK3399 FLASH/MMC Controller	1.2
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USIC Controller



USB2.0 Controller

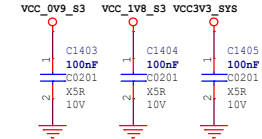
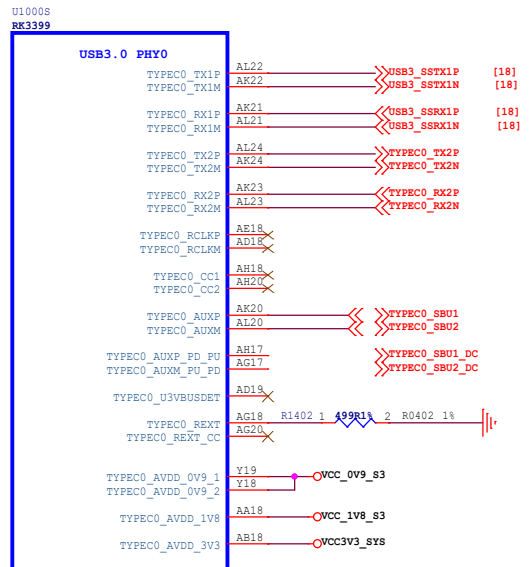


Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
所有电源去耦电容必须靠近RK3399电源管脚放置。

- USB2.0 design rules:
1. Max intra-pair skew < 4ps;
 2. Max trace length < 6inchs;
 3. Max allowed via < 6;
 4. Trace impedance 90ohm+/-10%;
 5. The trace spacing with other signals follows the 3W rule;

- USB2.0 信号设计规则:
1. 差分对内偏移小于4ps;
 2. 差分对线长小于6英寸;
 3. 差分对线过孔数量少于6个;
 4. 阻抗控制在90ohm+/-10%;
 5. 差分对与其他信号的间距遵循3W原则;

USB3.0 PHY0 Controller

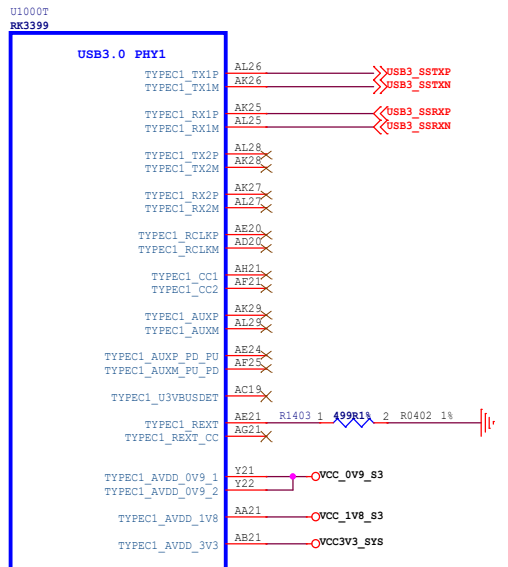


Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
所有电源去耦电容必须靠近RK3399电源管脚放置。

- USB3.0 design rules:
1. Max intra-pair skew < 4ps;
 2. Max length skew between TX and RX < 1.6ns;
 3. Max trace length < 6inchs;
 4. Max allowed via < 4;
 5. Trace impedance 90ohm+/-10%;
 6. The trace spacing with other signals follows the 3W rule;

- USB3.0 信号设计规则:
1. 差分对内偏移小于4ps;
 2. TX与RX的组间偏移小于1.6ns;
 3. 差分对线长小于6英寸;
 4. 差分对线过孔数量少于4个;
 5. 阻抗控制在90ohm+/-10%;
 6. 差分对与其他信号的间距遵循3W原则;

USB3.0 PHY1 Controller



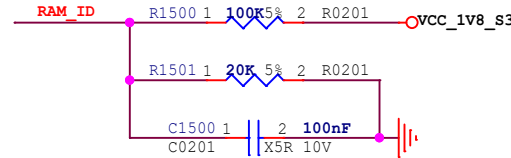
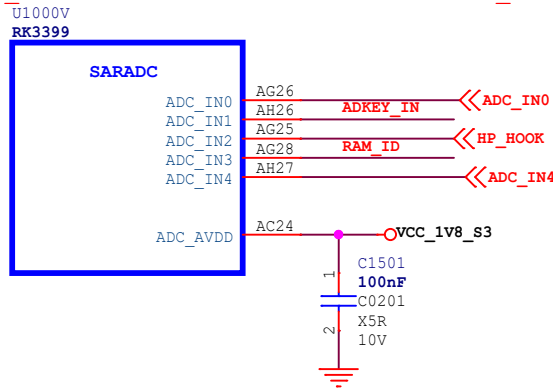
- DP design rules:
1. Max intra-pair skew < 4ps;
 2. Max trace length < 6inchs;
 3. Max allowed via < 4;
 4. Trace impedance 90ohm+/-10%;
 5. The distance between other signals follows the 3W rule;

radxa		
Size:	Title: ROCK PI 4C Plus	REV
A3	Page Name: 09.RK3399 USB/USIC Controller	1.2
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SARADC

Note:

Reserve ADC_IN2 for firmware update. If ADC2_KEY_IN=0V at power-on reset, then system will enter into Recovery/MiniLoader mode.
 预留 ADC_IN2 用于固件升级。如果上电复位情况下 ADC2_KEY_IN 处于低电平，系统会进入 Recovery/MiniLoader 模式。



SARADC design rules:

1. The trace spacing with other signals follows the 3W rule;

SARADC 信号设计规则:

1. 差分对与其他信号的间距遵循 3W 原则;

Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399.
 所有电源去耦电容必须靠近 RK3399 电源管脚放置。

Note:

- If ADC2_KEY_IN=0V at power-on reset, then system will enter into Recovery/MiniLoader mode.
- R1503, SW1500, ED1500 can be deleted if no need at Mass Production

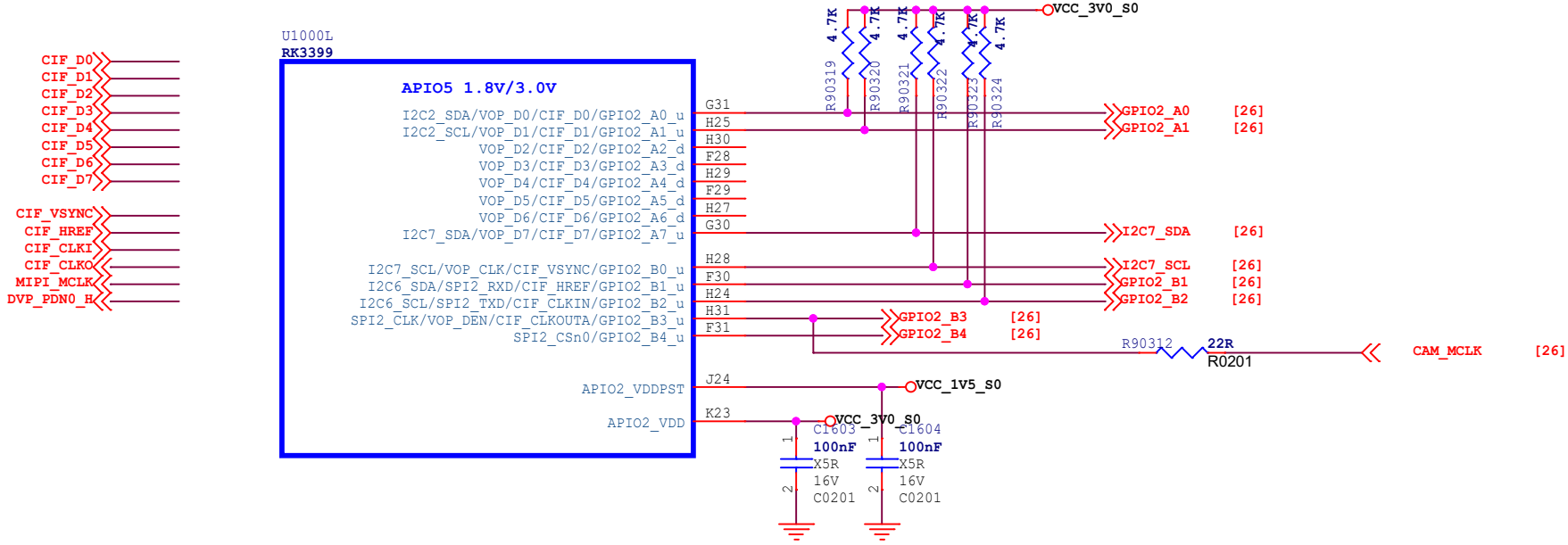
BOM ID

Item	Rup	Rdown		VOL	VERSION
LEVEL1	DNP	100K		0V	A
LEVEL2	100K	20K		0.3V	B
LEVEL3	100K	51K		0.6V	C
LEVEL4	100K	100K		0.9V	D
LEVEL5	100K	200K		1.2V	E
LEVEL6	100K	499K		1.5V	F
LEVEL7	100K	DNP		1.8V	G

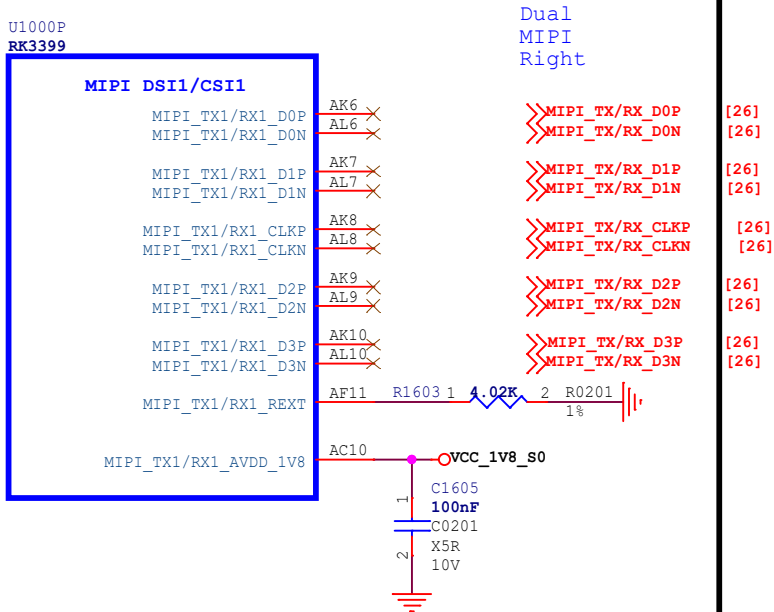


Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 10.RK3399 SAR-ADC/Key	1.2
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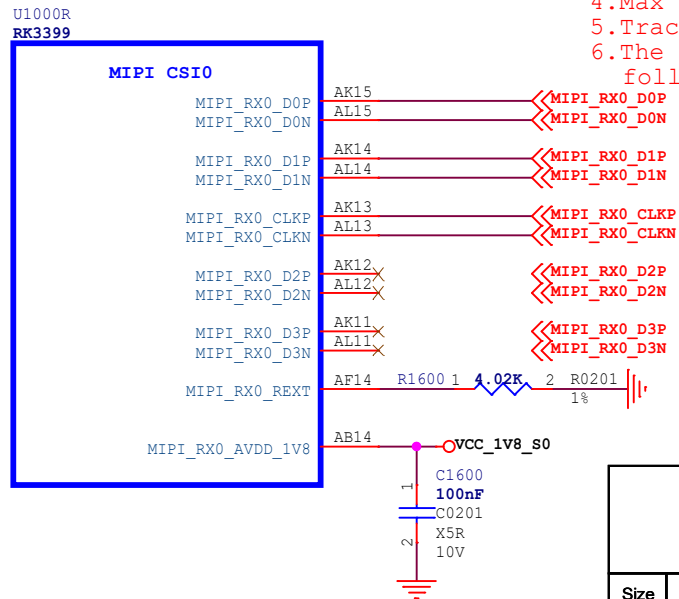
Video Input



MIPI DSI1/CSI1



MIPI CSI0



- MIPI design rules:
1. Max intra-pair skew < 4ps;
 2. Max length skew between clk and data < 7ps;
 3. Max trace length < 7.2inchs;
 4. Max allowed via < 4;
 5. Trace impedance 100ohm+/-10%;
 6. The distance between other signals follows the 3W rule;

Note: All the Power filter capacitors should be placed close to the power pins of RK3399

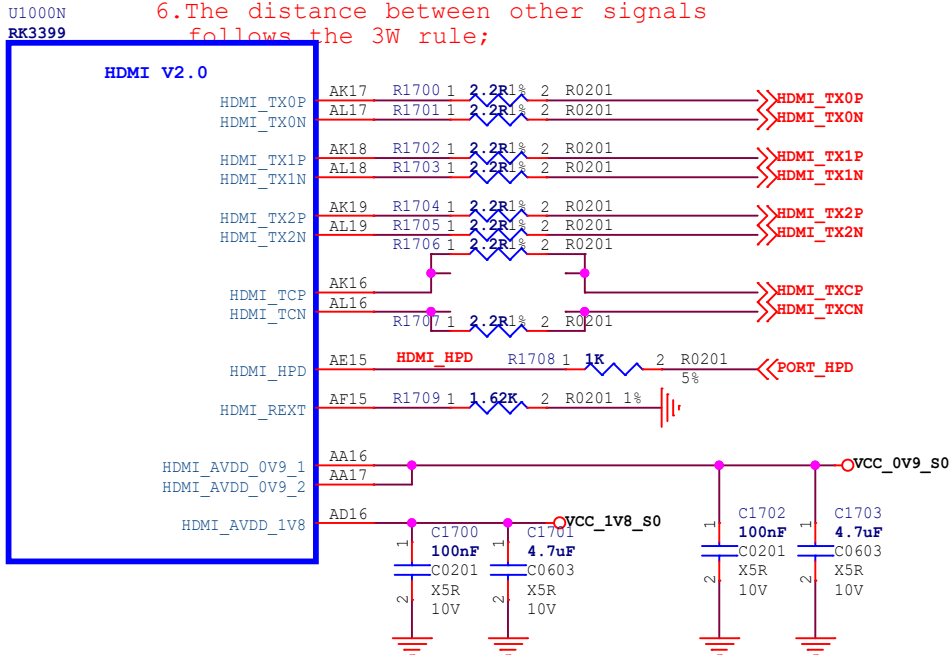


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	Page Name: 11.RK3399 VideoInput	1.2
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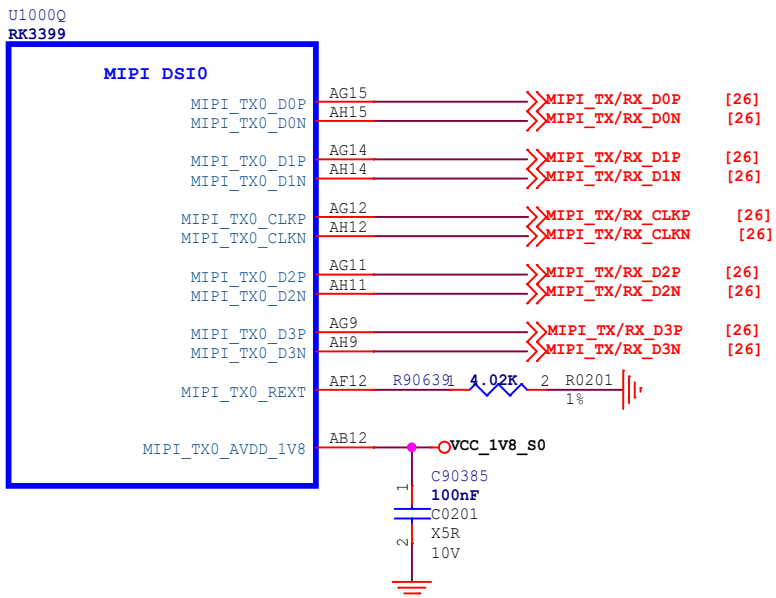
HDMI

HDMI design rules:

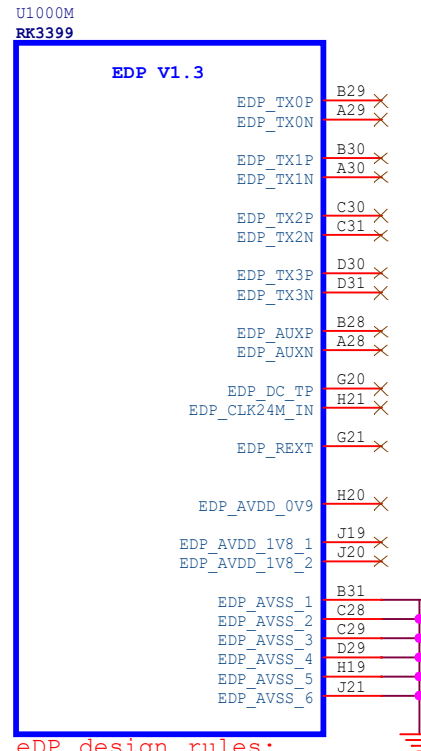
- 1.Max intra-pair skew < 4ps;
- 2.Max length skew between clk and data < 80ps;
- 3.Max trace length < 9.8inchs;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.The distance between other signals follows the 3W rule;



MIPI DSI0



EDP



EDP design rules:

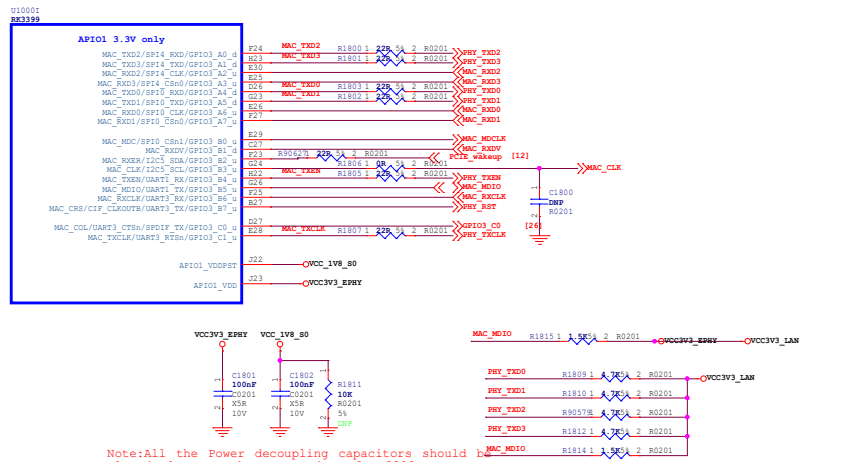
- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6inchs;
- 3.Max allowed via < 4;
- 4.Trace impedance 100ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

Note:All the Power decoupling capacitors should be placed close to the power pins of RK3399.
所有电源去耦电容必须靠近RK3399电源管脚放置。

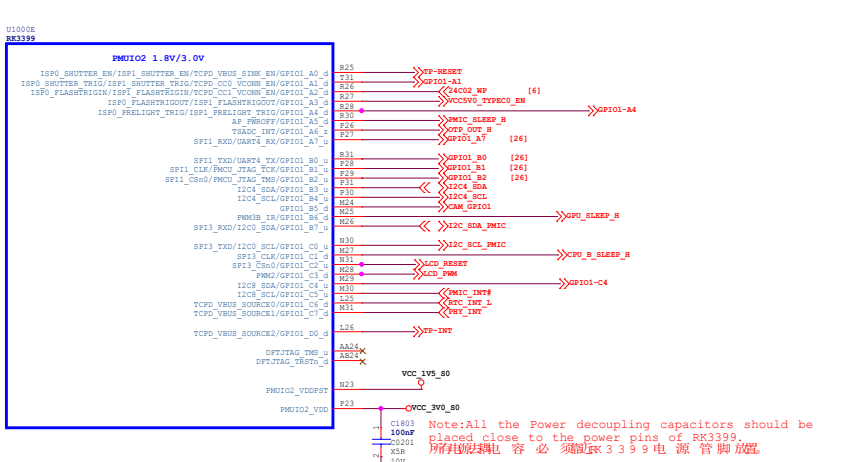


Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 12.RK3399 VideoOutput	1.2
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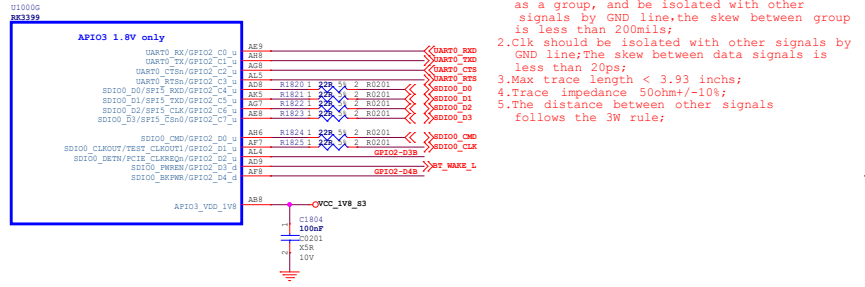
APIO1



PMUIO2



APIO3

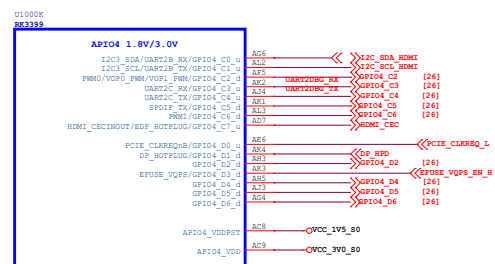


SDIO design rules:
 1.Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signals by GND line-the skew between group is less than 200mils;
 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
 3.Max trace length < 3.93 inches;
 4.Trace impedance 50ohm±10%;
 5.The distance between other signals follows the 3W rule;

1.8V Only	VDDPST=VDDIO=1.8V
3.3V Only	VDDPST=1.8V, VDDIO=3.3V
1.8V/3.0V mode	mode:VDDPST=1.5V, VDDIO=3.0V
3.0V mode	mode:VDDPST=1.8V, VDDIO=1.8V

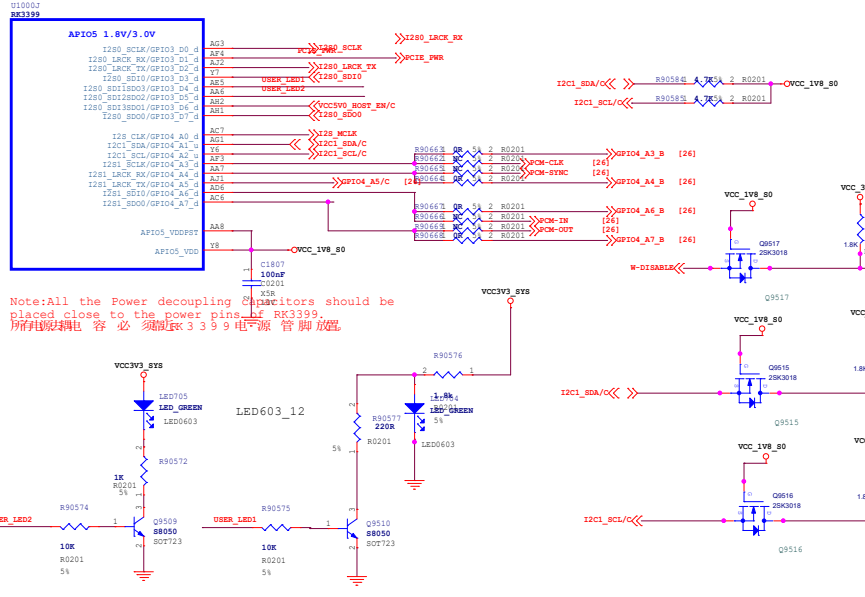
Note: All the part which support 1.8V and 3.0V mode, software config should match with hardware design.

APIO4

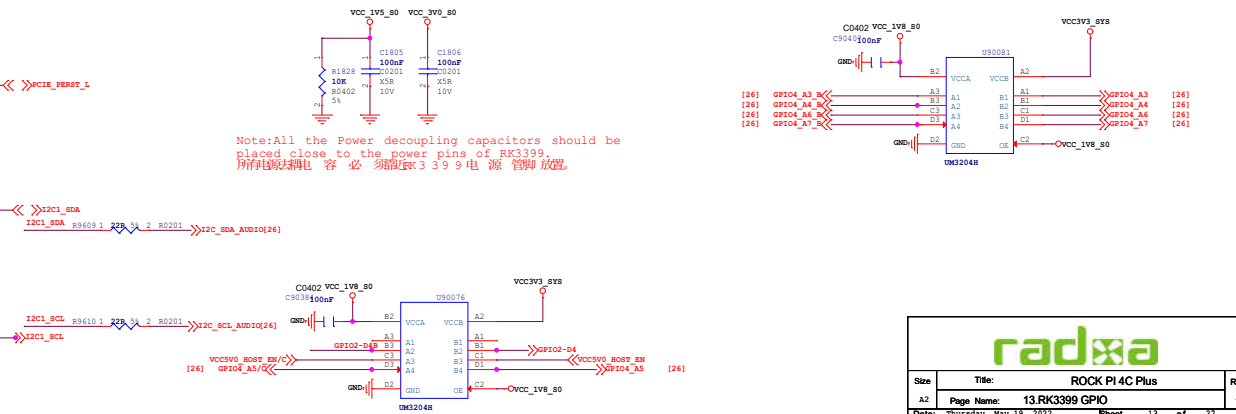


Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399. 所有电源滤波电容必须靠近3.3V电源管脚放置。

APIO5

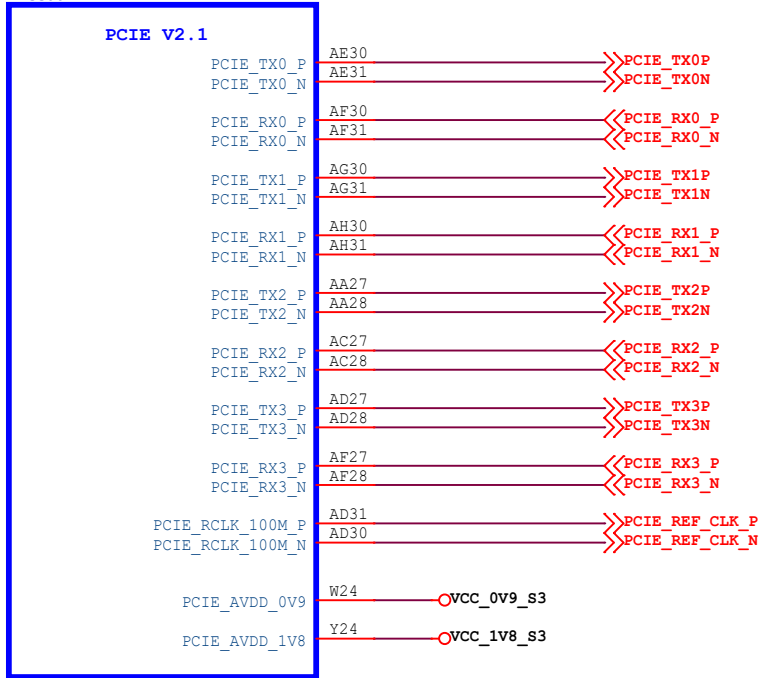


Note: All the Power decoupling capacitors should be placed close to the power pins of RK3399. 所有电源滤波电容必须靠近3.3V电源管脚放置。

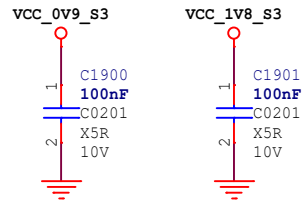


PCIE


U10000
RK3399



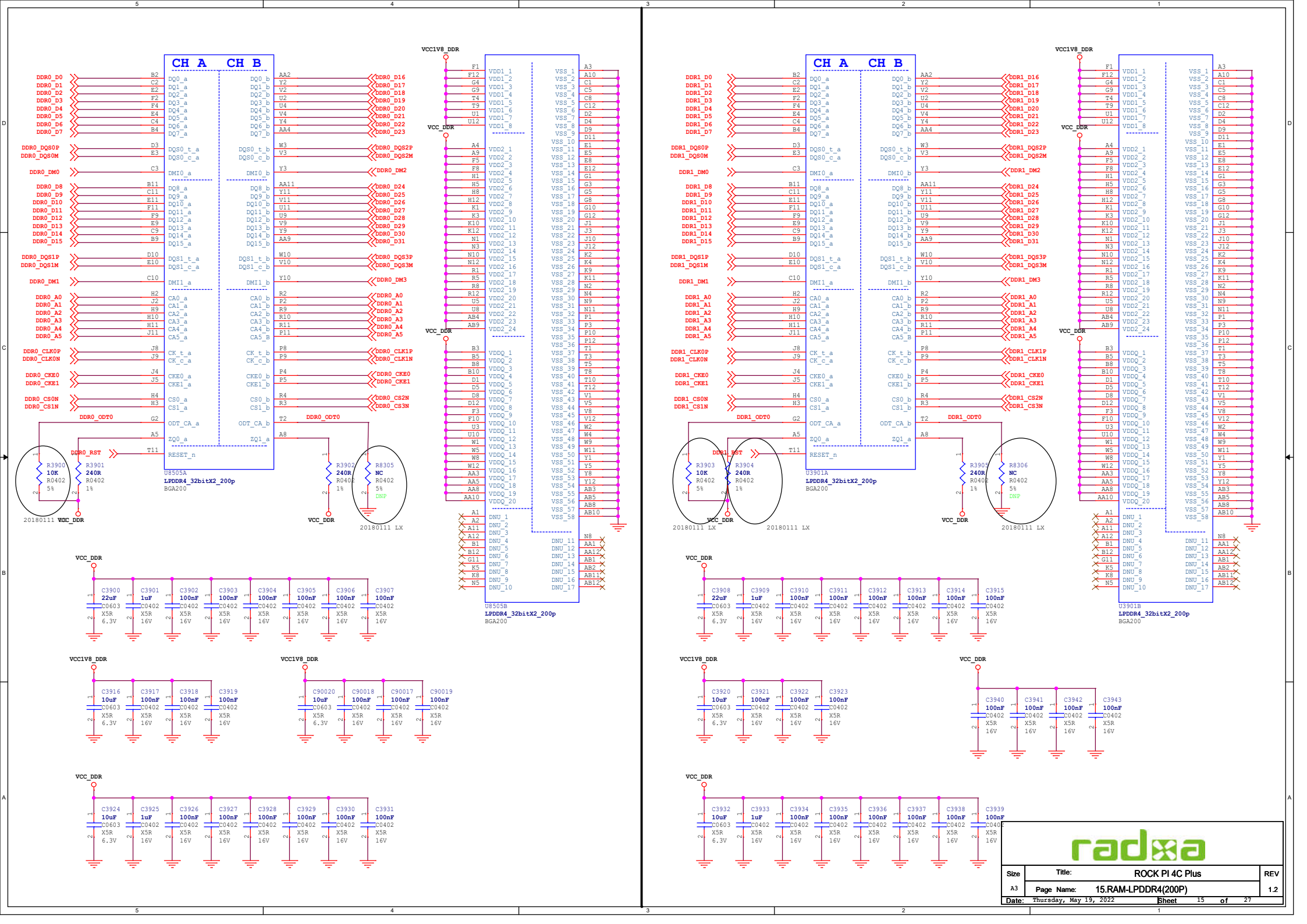
- PCIE design rules:
1. Max intra-pair skew < 4ps;
 2. Max inter-pair skew < 1.6ns;
 3. Max trace length < 14inches;
 4. Max allowed via < 4;
 5. Trace impedance 100ohm+/-10%;
 6. The distance between other signals follows the 3W rule;



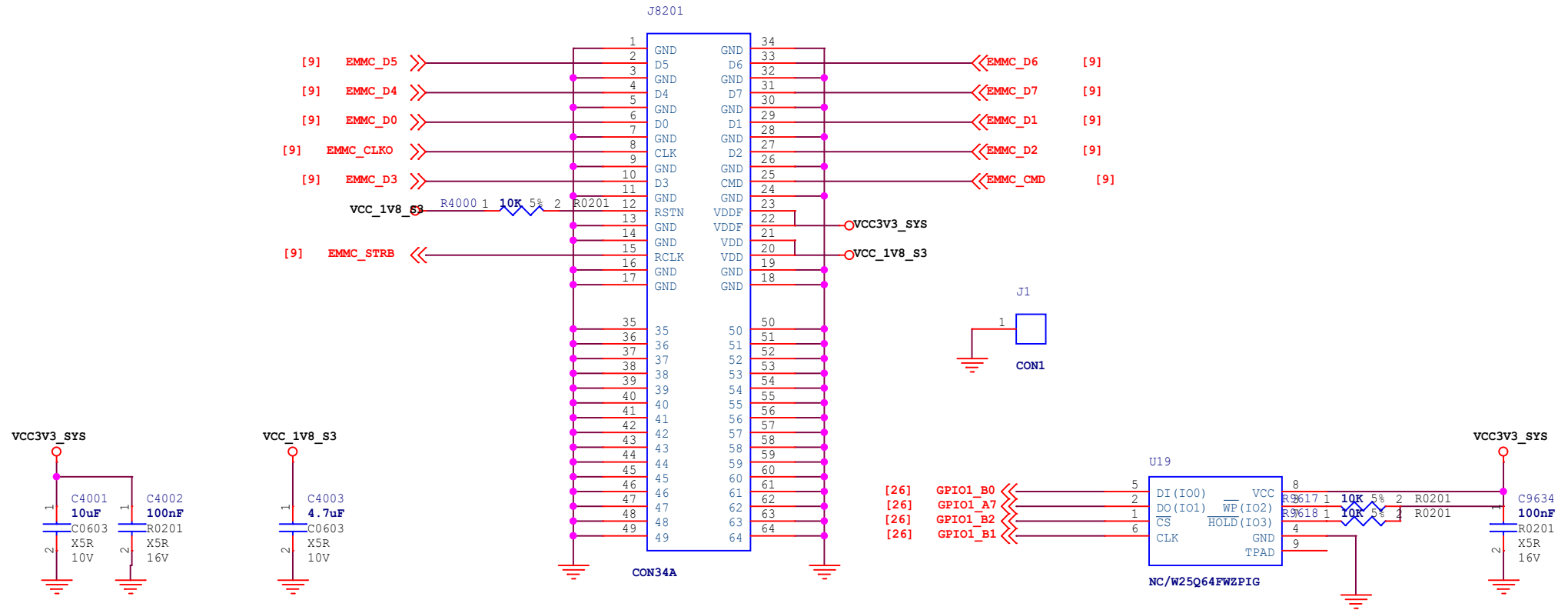
Note: All the Power filter capacitors should be placed close to the power pins of RK3399

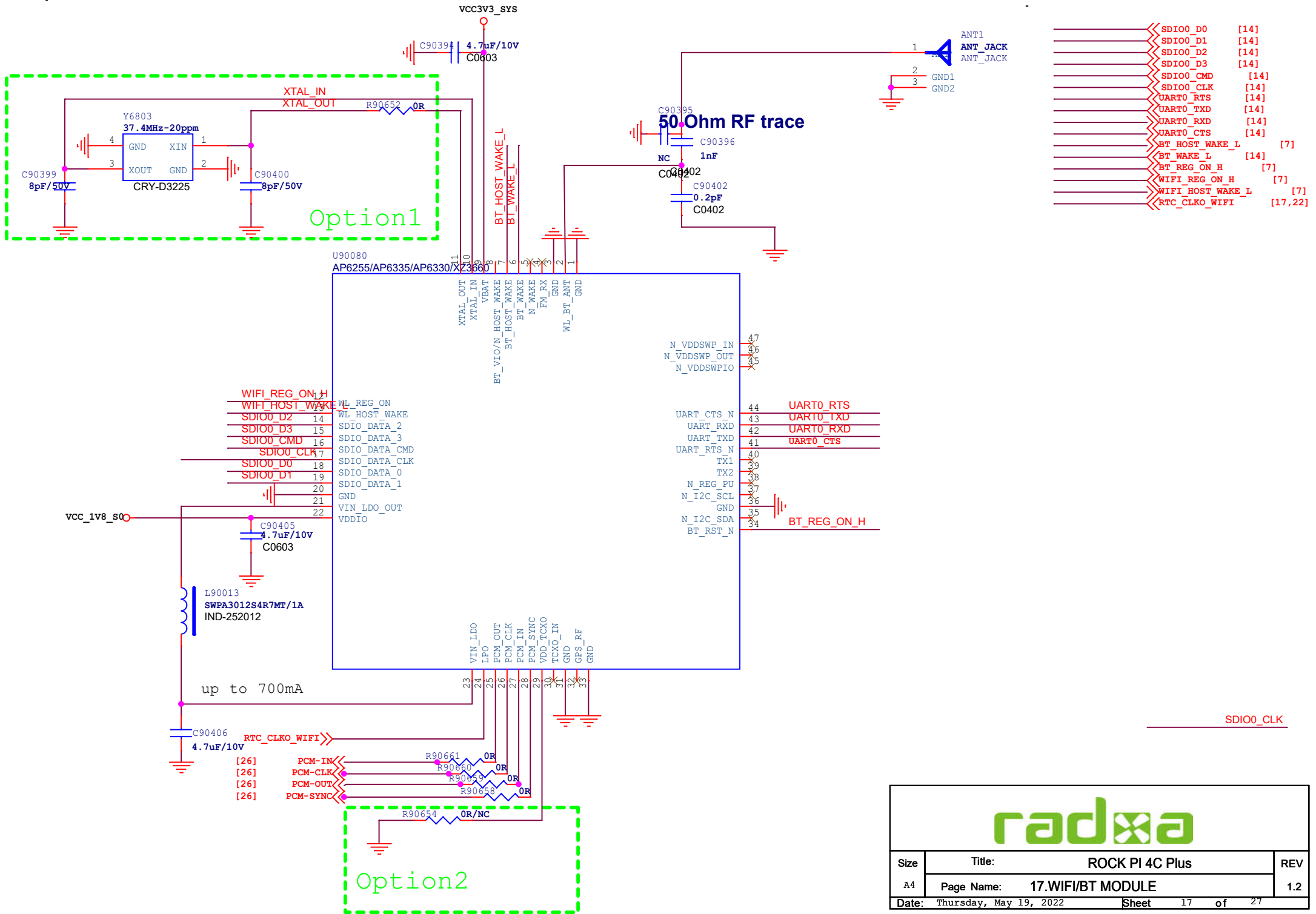


Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 14.RK3399 PCIE	1.2
Date: Thursday, May 19, 2022		Sheet 14 of 27




eMMC FLASH



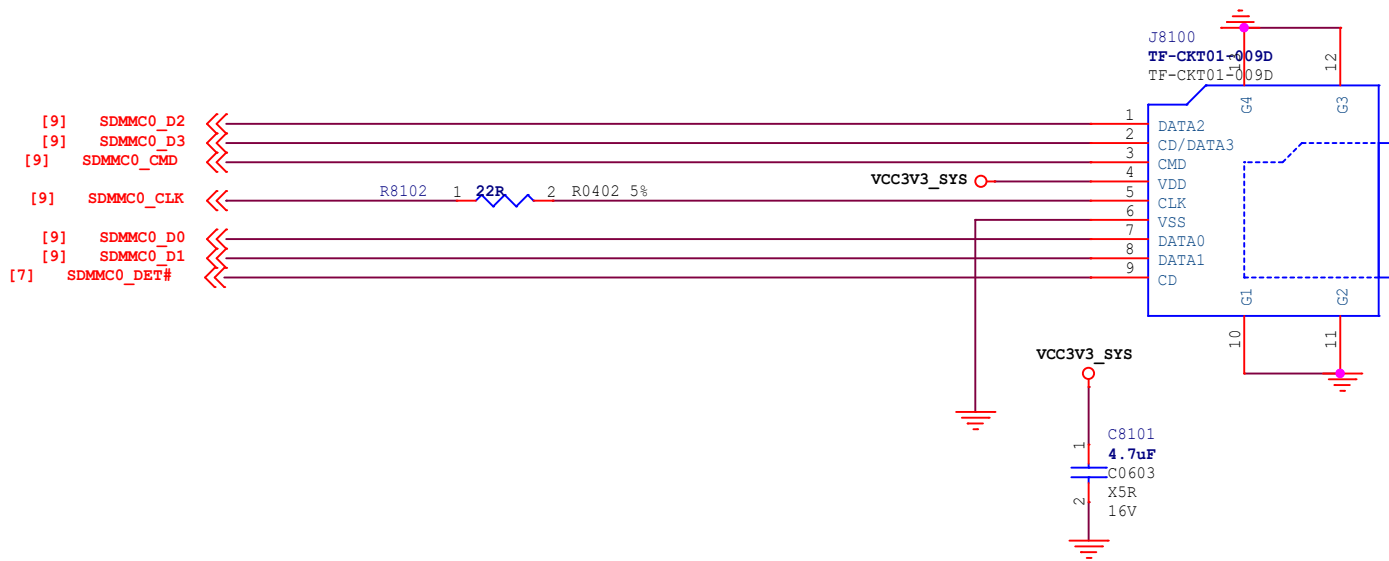


- SDIO0_D0 [14]
- SDIO0_D1 [14]
- SDIO0_D2 [14]
- SDIO0_D3 [14]
- SDIO0_CMD [14]
- SDIO0_CLK [14]
- UART0_RTS [14]
- UART0_TXD [14]
- UART0_RXD [14]
- UART0_CTS [14]
- BT_HOST_WAKE_L [7]
- BT_WAKE_L [14]
- BT_REG_ON_H [7]
- WIFI_REG_ON_H [7]
- WIFI_HOST_WAKE_L [7]
- RTC_CLKO_WIFI [17,22]



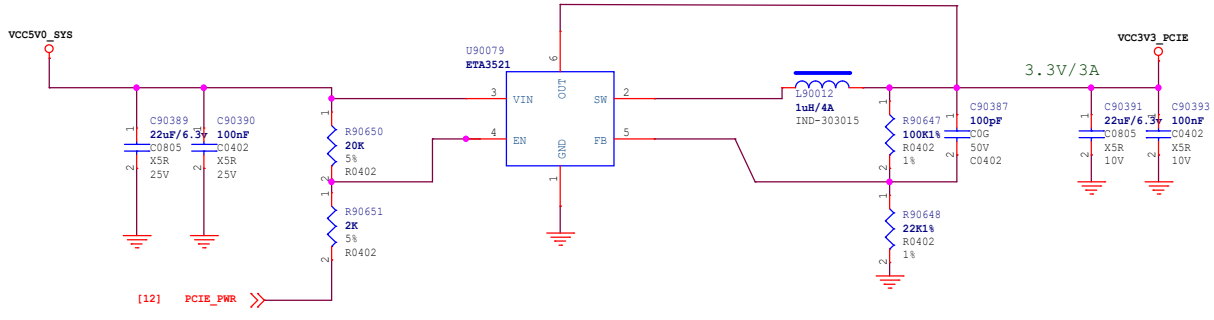
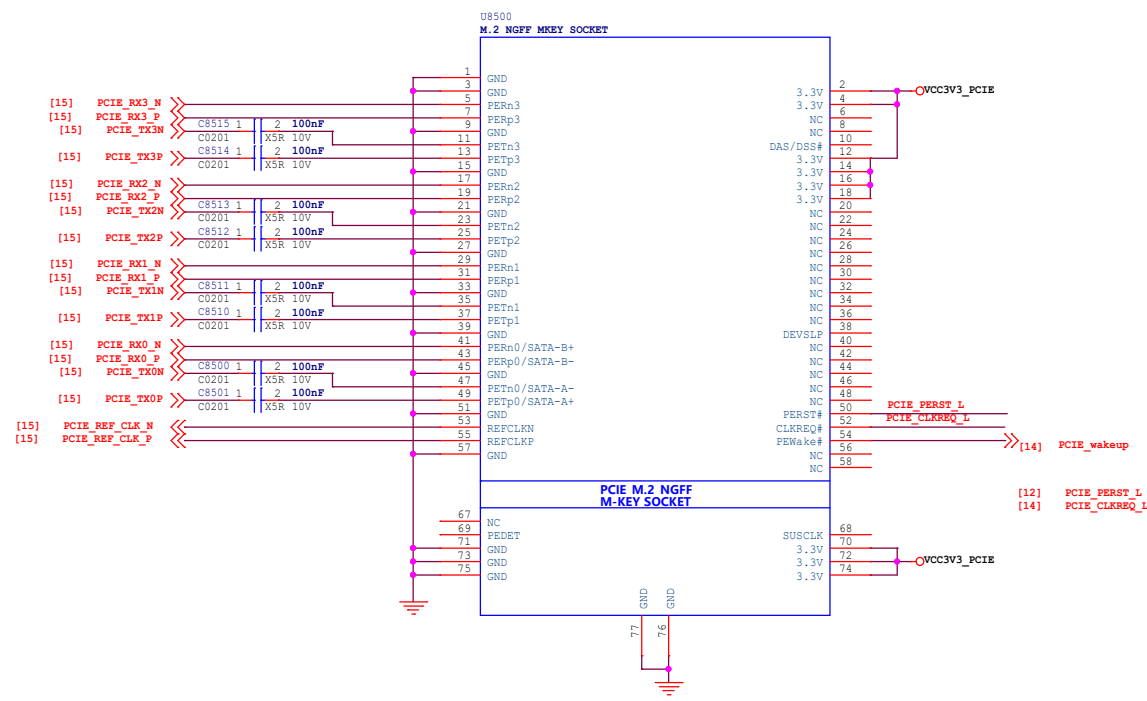
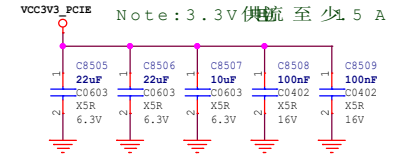
Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 17.WIFI/BT MODULE	1.2
Date: Thursday, May 19, 2022		Sheet 17 of 27

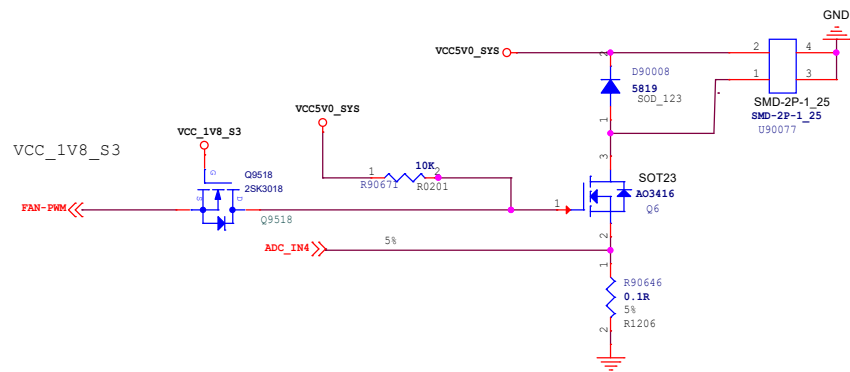
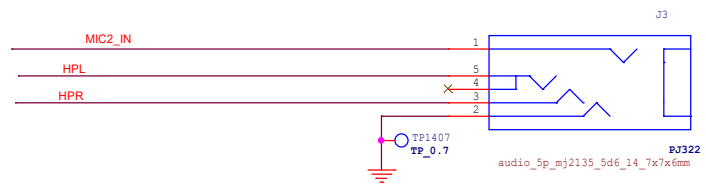
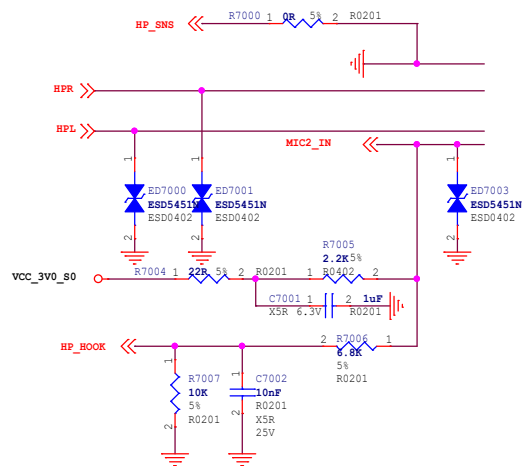
TF CARD

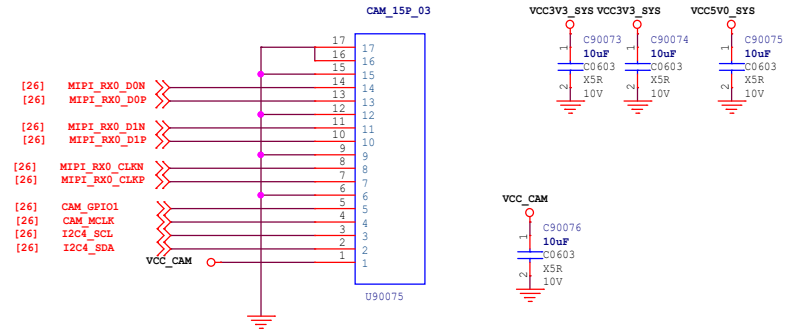
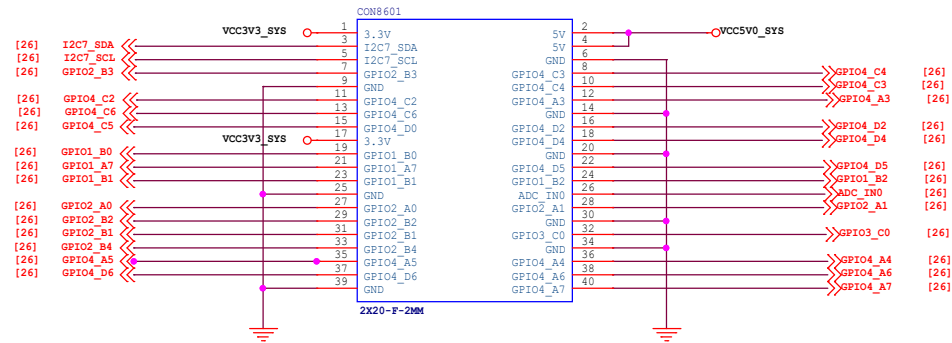
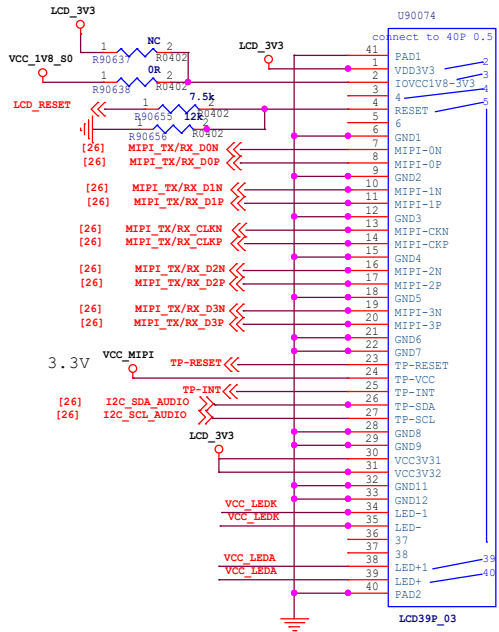


Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 18.TF Card	1.2
Date: Thursday, May 19, 2022		Sheet 18 of 27

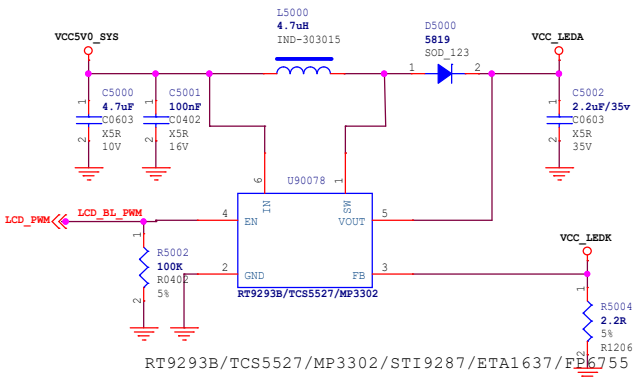
PCIe NGFF/M.2



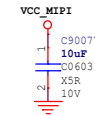




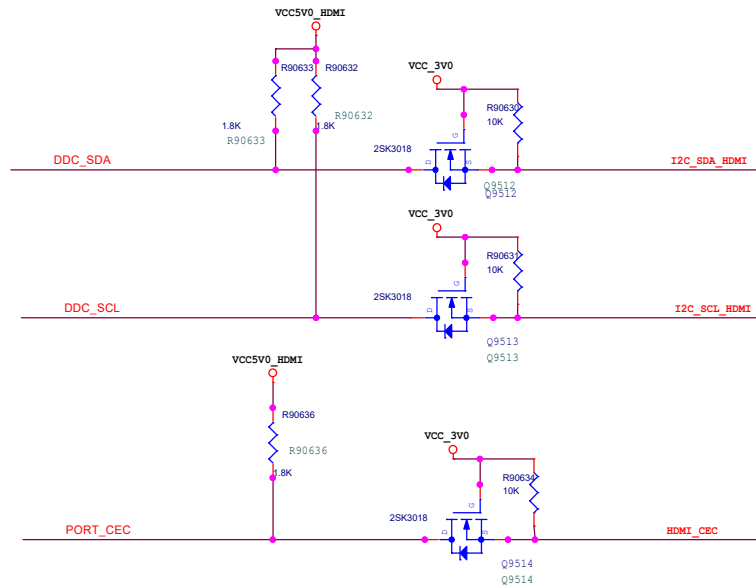
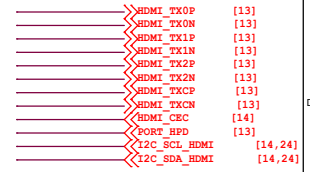
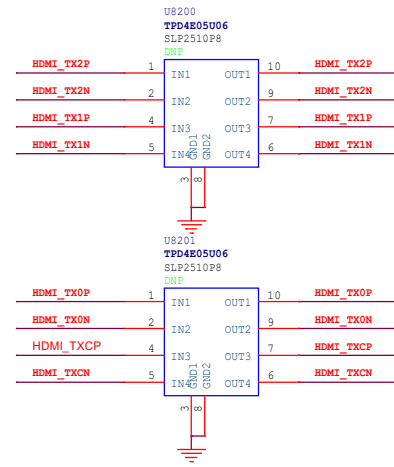
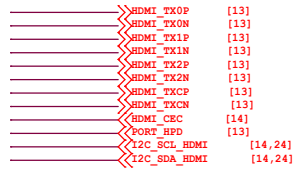
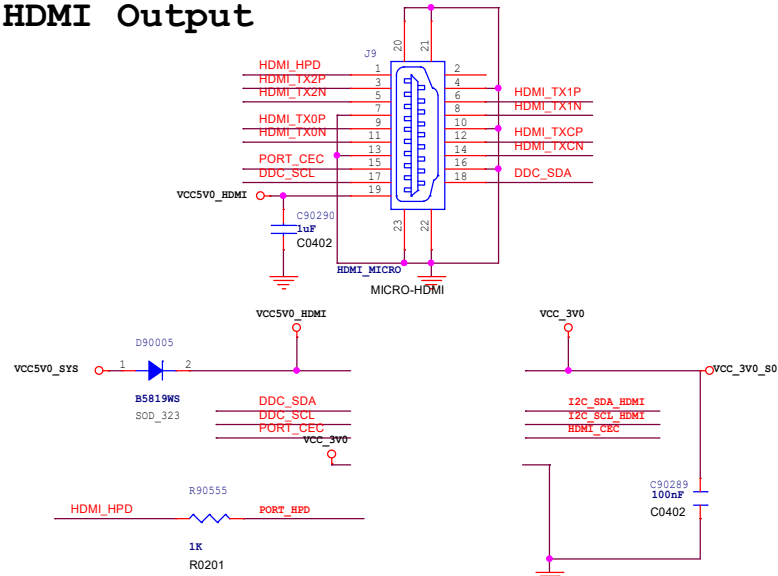
LCD



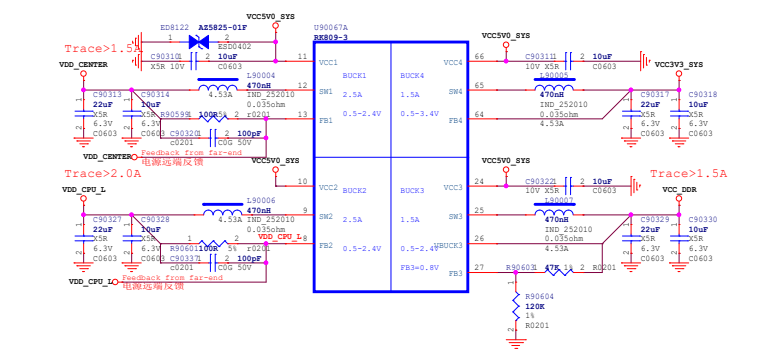
RT9293B: L5000=10UH
 MP3302: L5000=4.7UH
 ETZ1637: L5000=10UH R5004=NC
 RT9293B: L5000=6.8UH



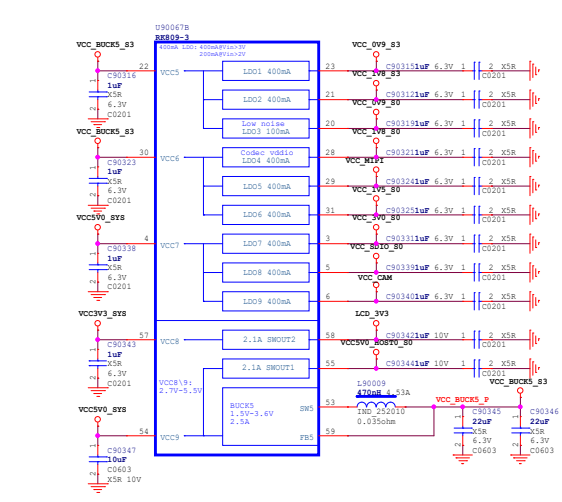
HDMI Output



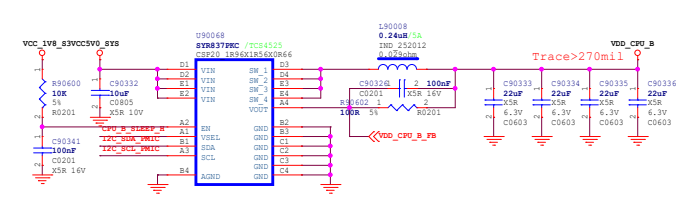
PMIC RK809-3 DCDC



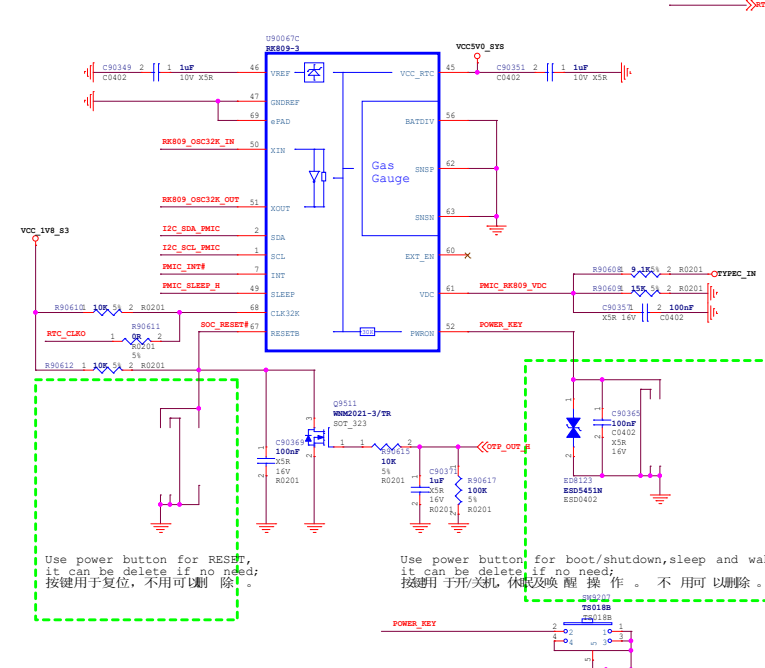
PMIC RK809-3 LDO



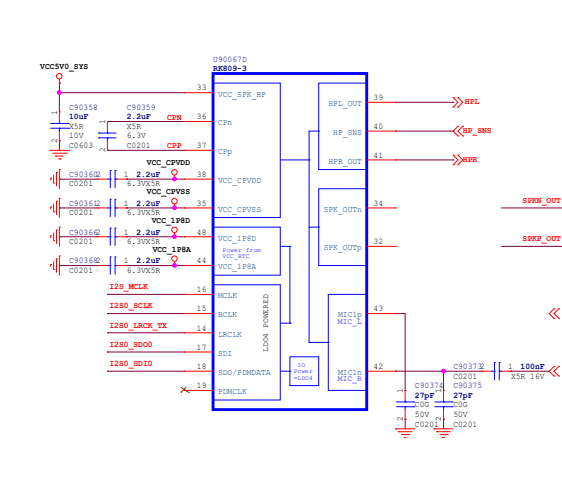
Power of VDD_CPU_B



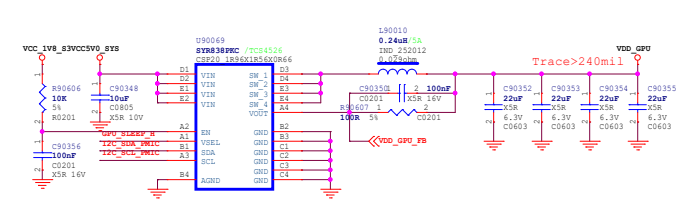
PMIC RK809-3 Management



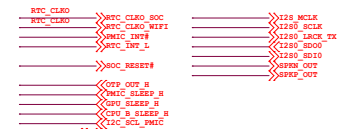
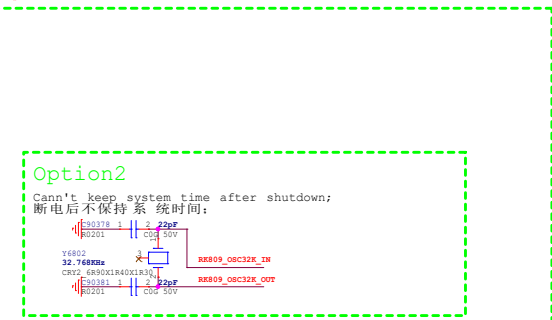
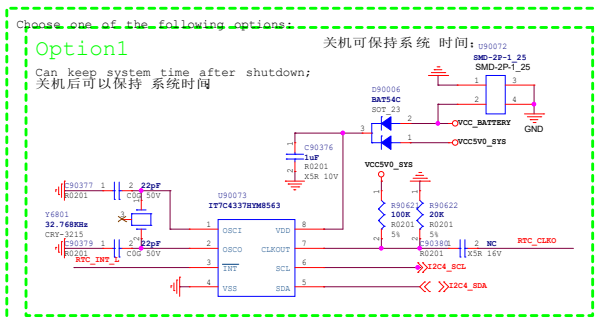
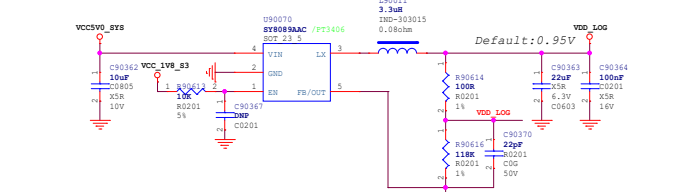
PMIC RK809-3 CODEC



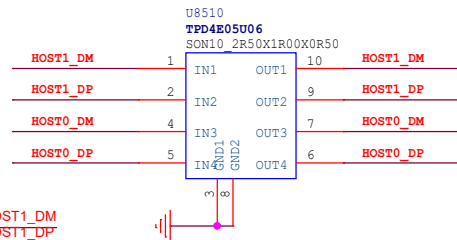
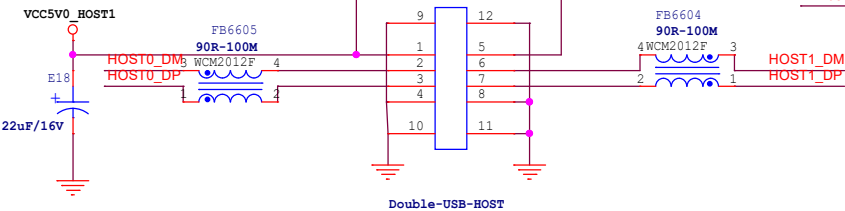
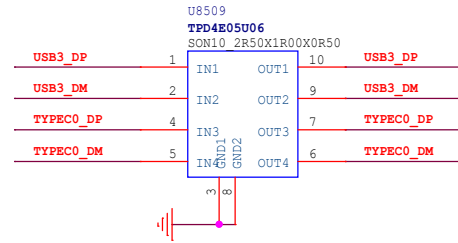
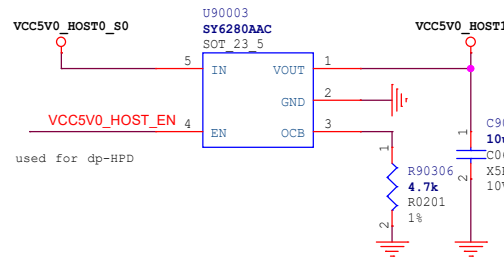
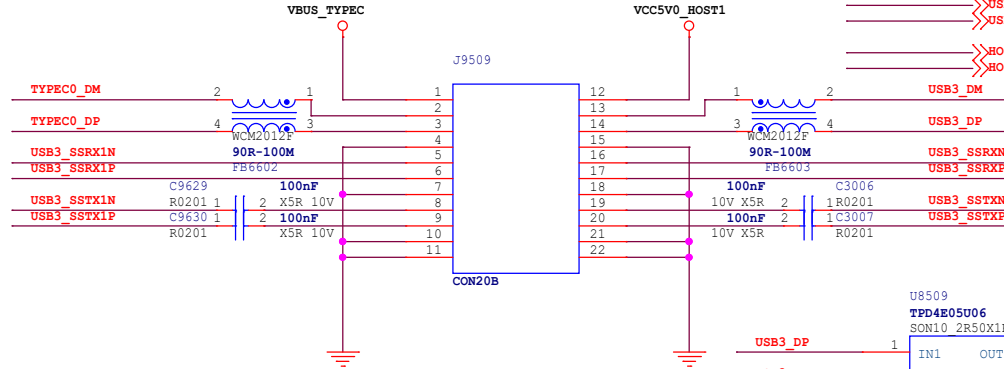
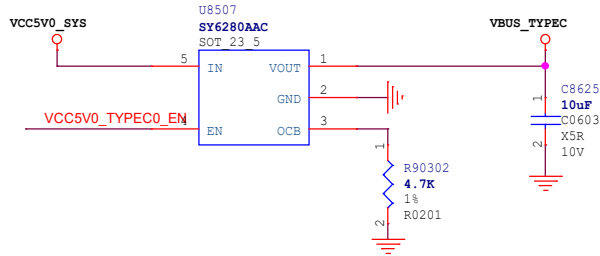
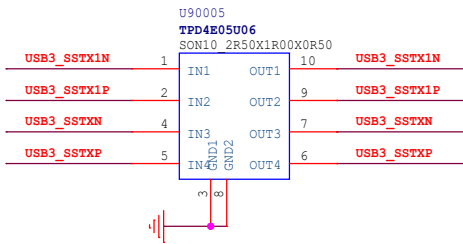
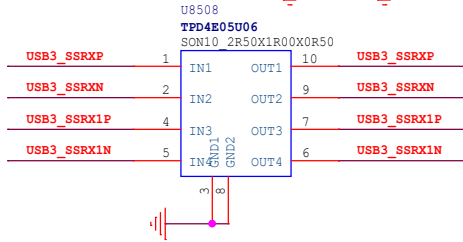
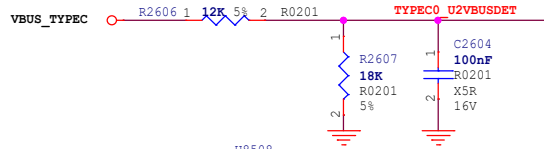
Power of VDD_GPU



Power of VDD_I2C



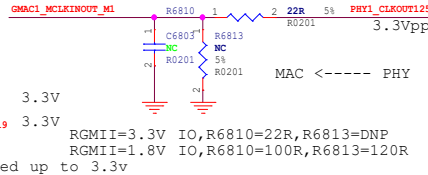
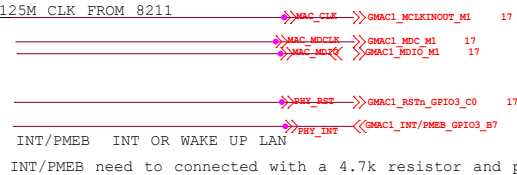
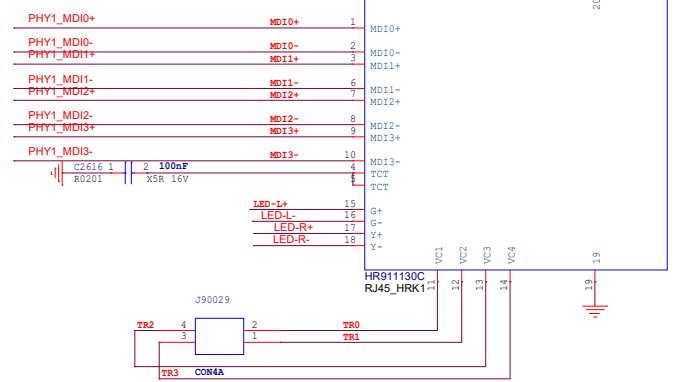
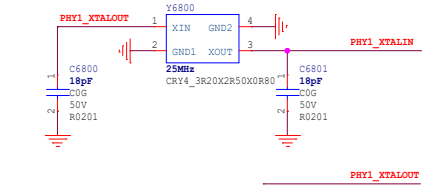
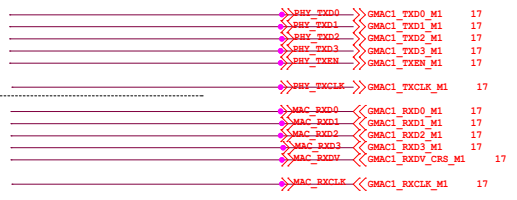
USB3.0 OTG port



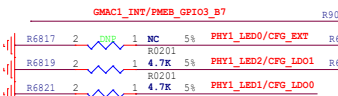
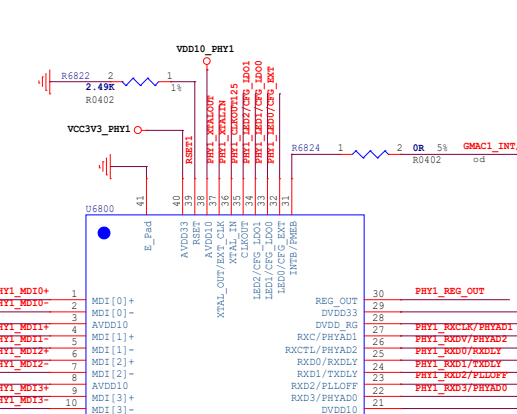
- >>>TYPECO_DP [10]
- >>>TYPECO_DM [10]
- >>>VCC5V0_TYPPEC0_EM [14]
- >>>TYPECO_U2VBUSDET [10]
- >>>USB3_SSTX1P [18]
- >>>USB3_SSTXIN [18]
- >>>USB3_SSRX1P [18]
- >>>USB3_SSRXIN [18]
- >>>HOST0_DP [10]
- >>>HOST0_DM [10]
- >>>VCC5V0_HOST_EN [14]
- >>>USB3_DP [10]
- >>>USB3_DM [10]
- >>>USB3_SSTXP [10]
- >>>USB3_SSTXN [10]
- >>>USB3_SSRXP [10]
- >>>USB3_SSRXN [10]
- >>>HOST1_DP [26]
- >>>HOST1_DM [26]



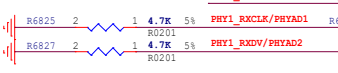
Size	Title: ROCK PI 4C Plus	REV
	Page Name: 24.USB3.0 OTG Port	1.2
Date: Thursday, May 19, 2022	Sheet	24 of 27



RGMIIO=3.3V IO, R6810=22R, R6813=DNP
 RGMII=1.8V IO, R6810=100R, R6813=120R



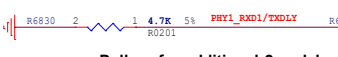
VCC_PHY10 Voltage Config



PHY Address Config



Pull-up for additional 2ns delay to RXC for data latching

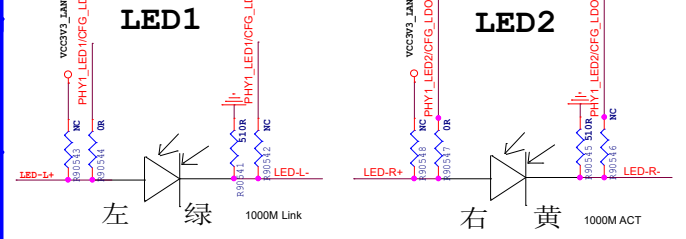


Pull-up for additional 2ns delay to TXC for data latching

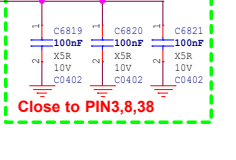
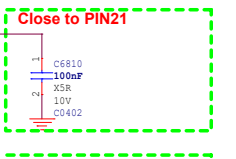
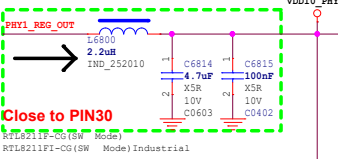
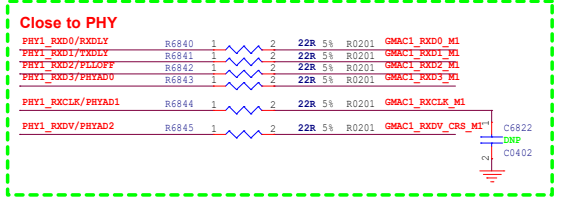
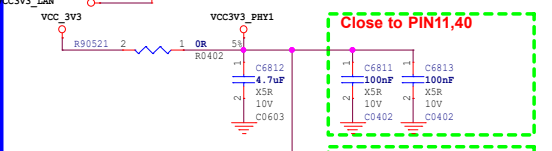
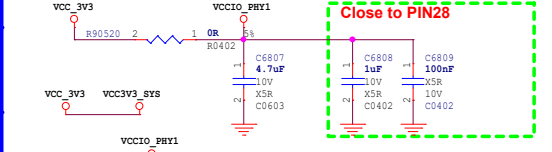


Pull-up to disable PLL @ ALDPS mode

RGMIIO Power Source	CFG_EXT	CFG_LDO1(1:0)
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 0.8V	1'b0	2'b10

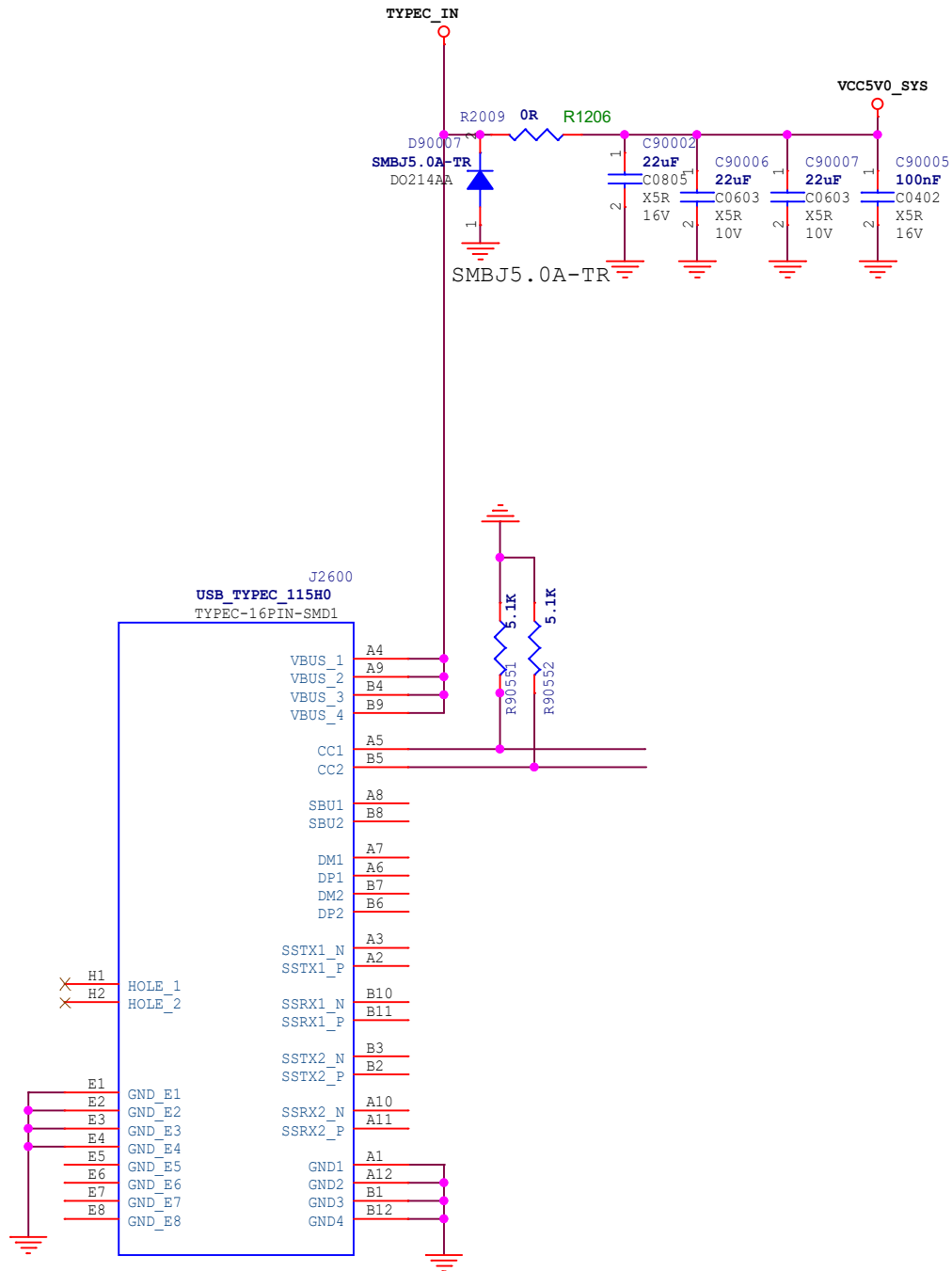



8211F default definitions : LED1 100M LINK AND ACTIVE
 LED2 1000M LINK AND ACTIVE



Rockchip Confidential

DC IN&SYSTEM Power



		
Size	Title: ROCK PI 4C Plus	REV
A4	Page Name: 26.Power TYPEC IN	1.2
Date: Thursday, May 19, 2022	Sheet	26 of 27

