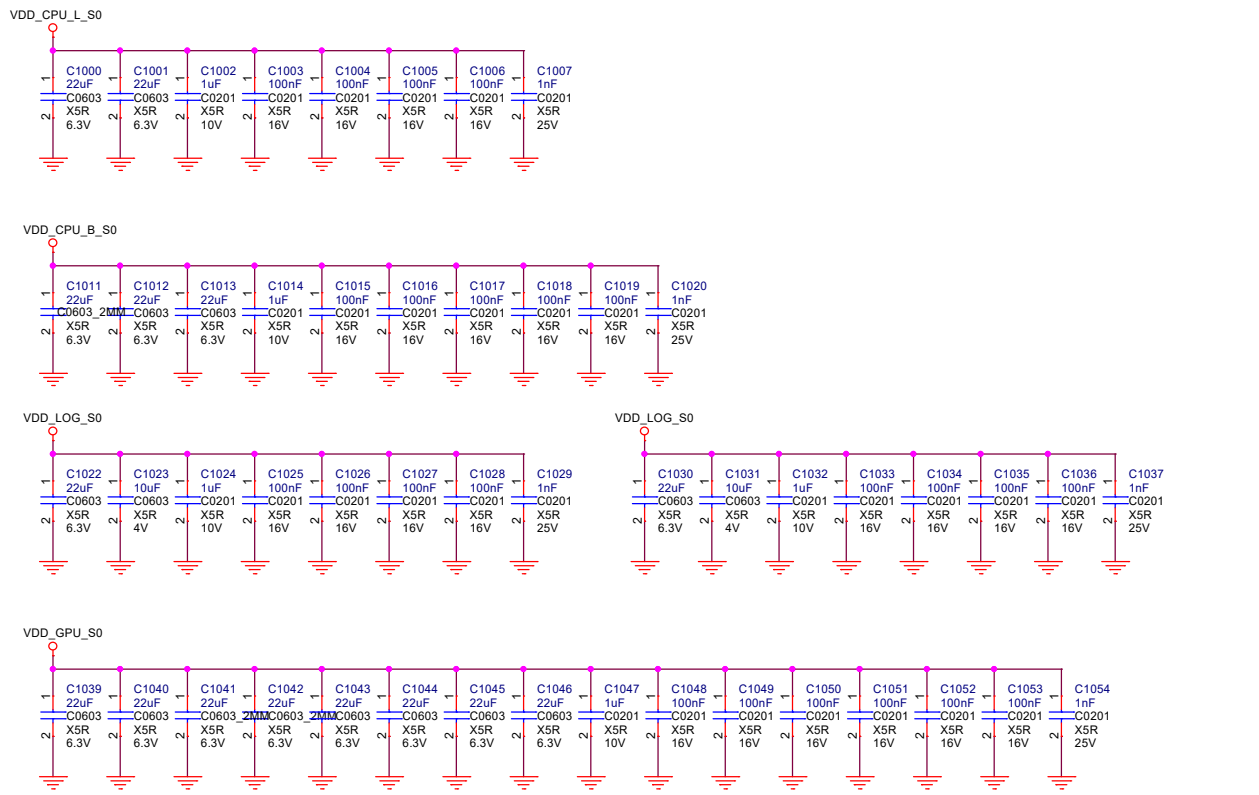
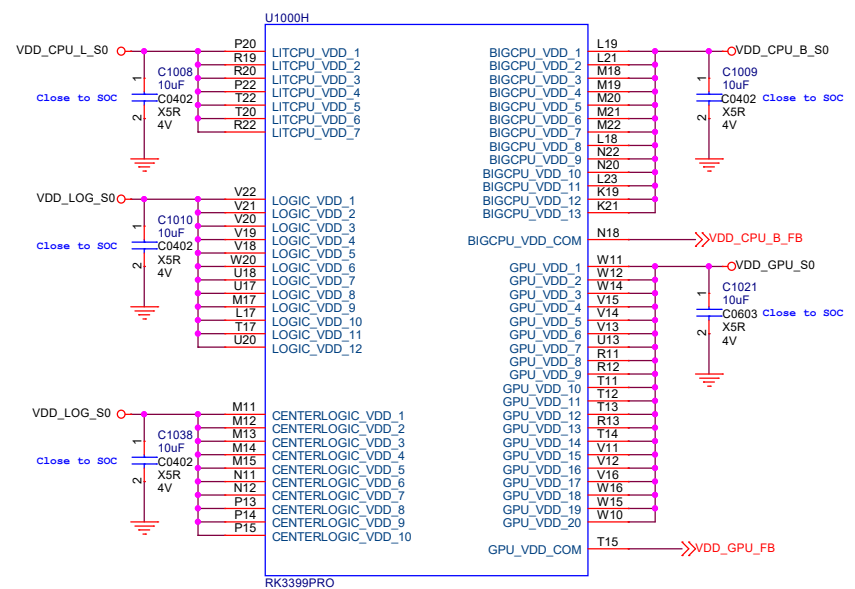
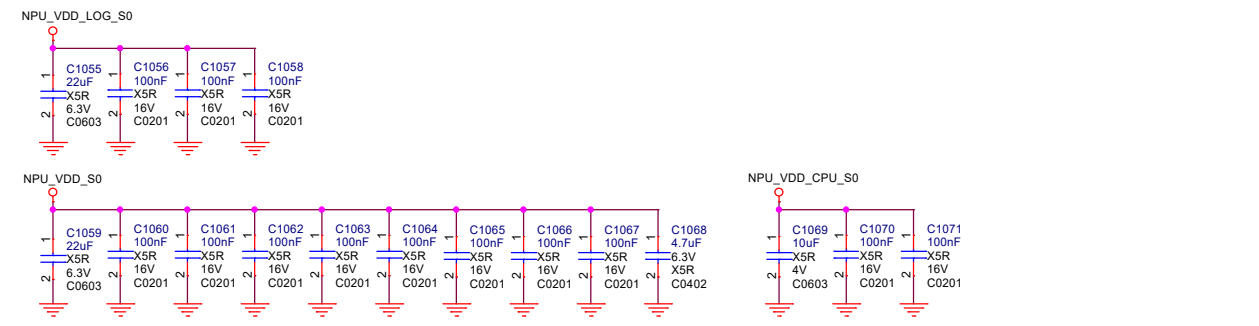
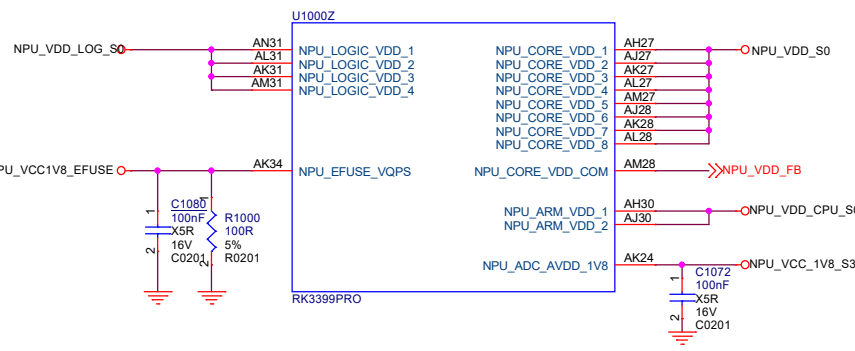


Power

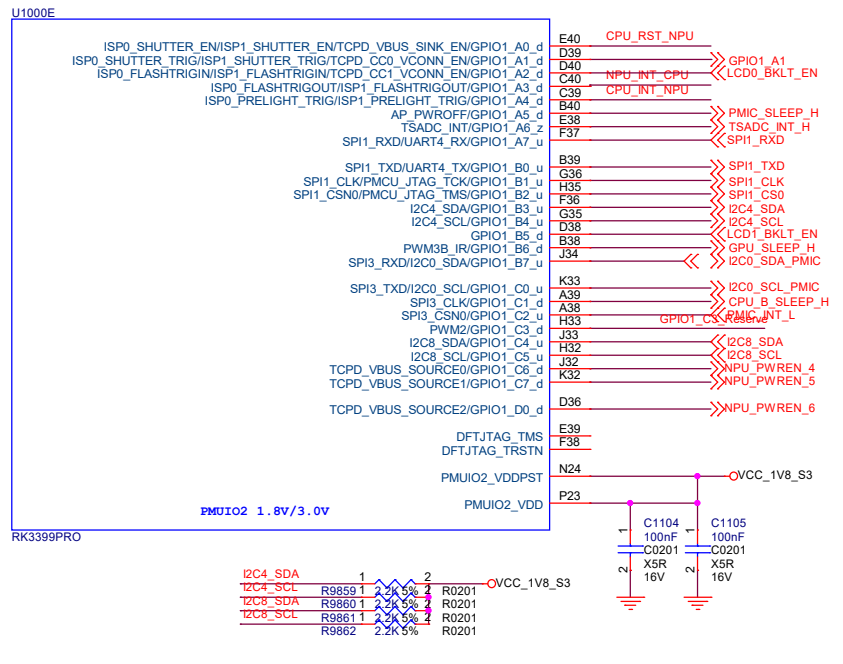
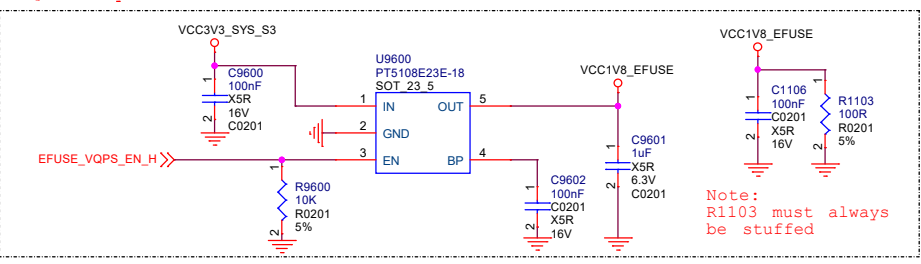
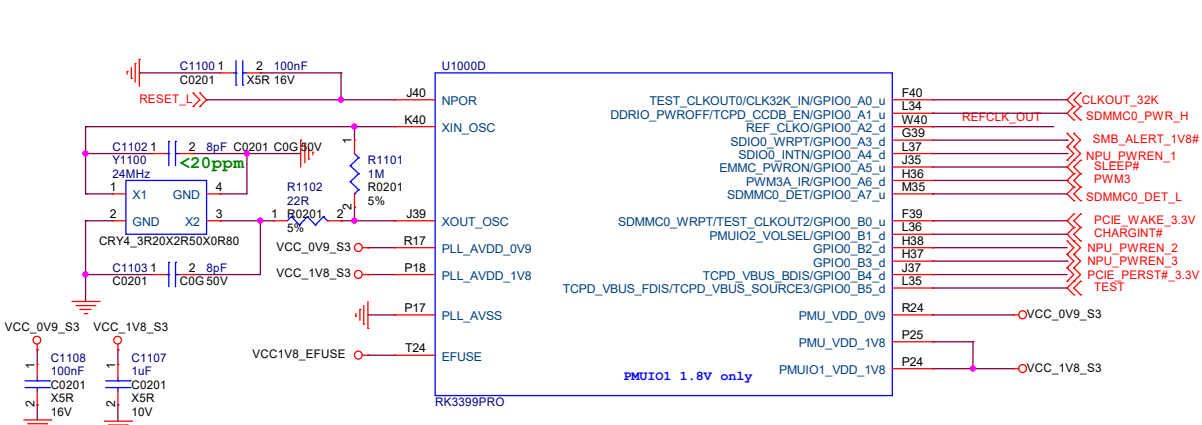


NPU Power

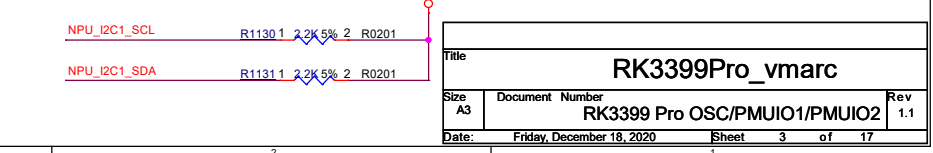
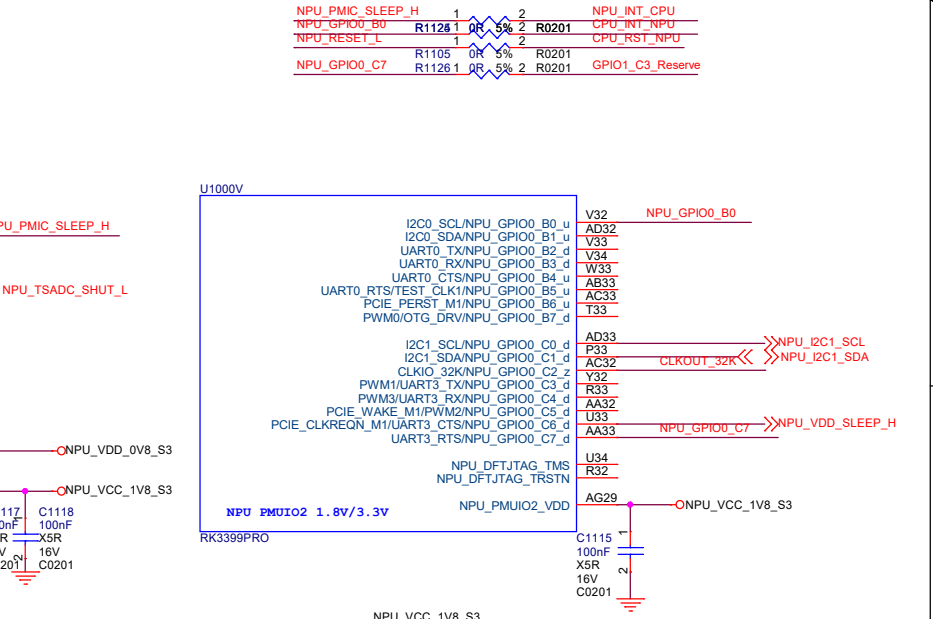
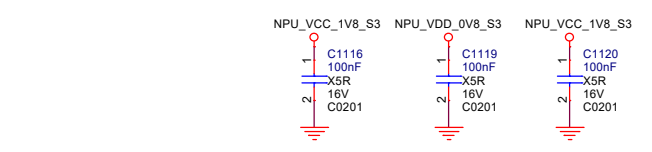
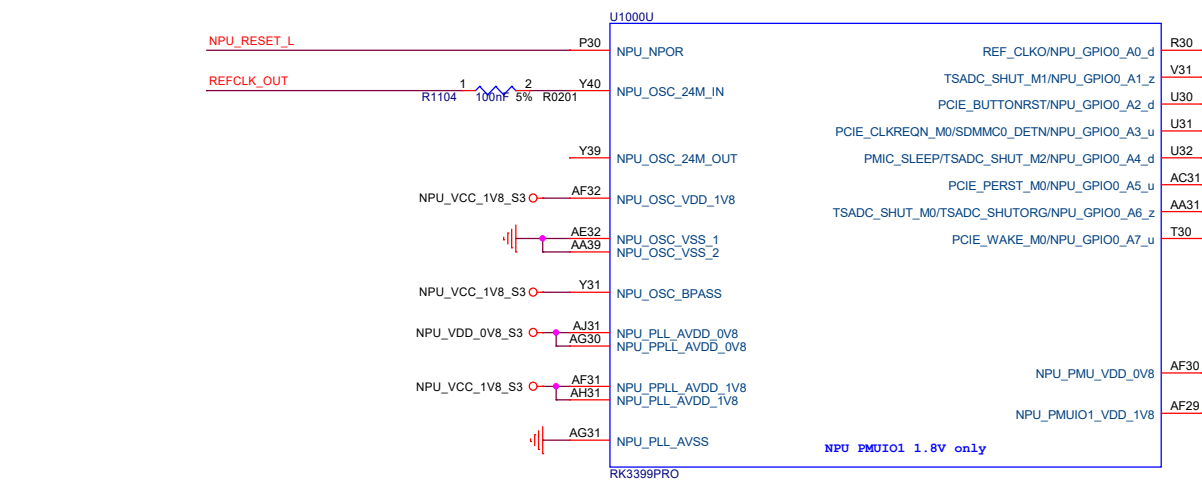


Title			RK3399Pro_vmarc		
Size	Document Number	Rev			
A3	RK3399 Pro Power	1.1			
Date:	Monday, May 31, 2021	Sheet	2	of	17

PMUIO1/PMUIO2

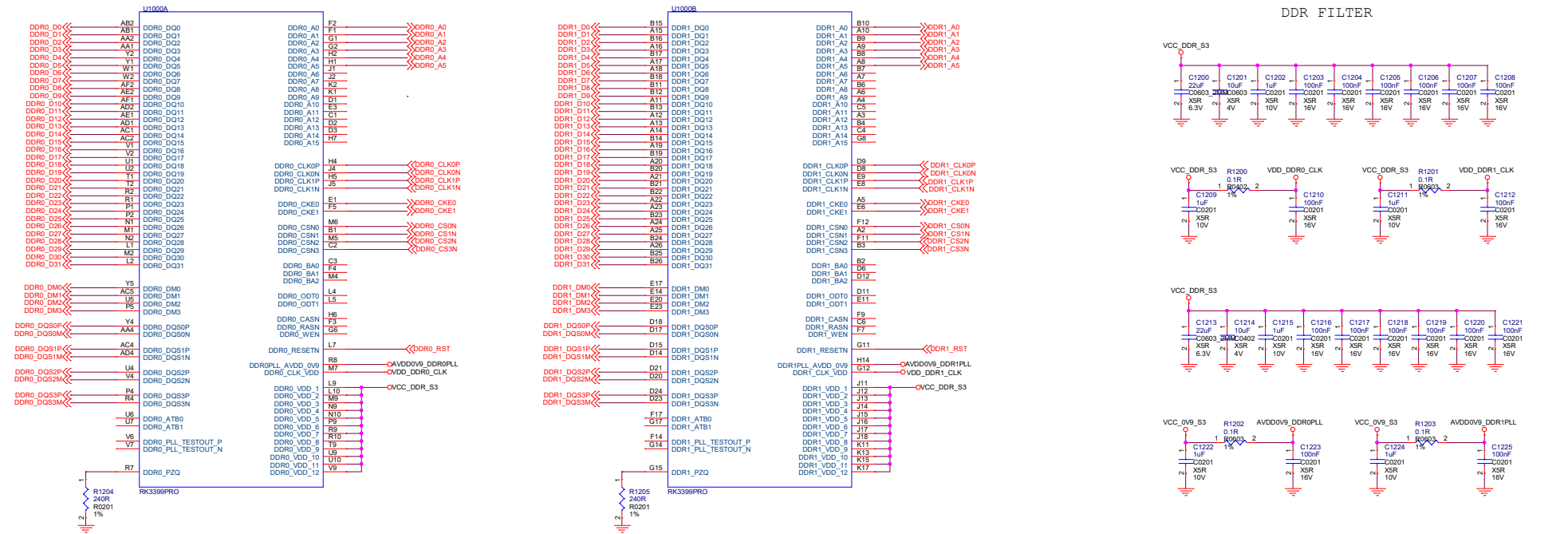


NPU PMUIO1/PMUIO2

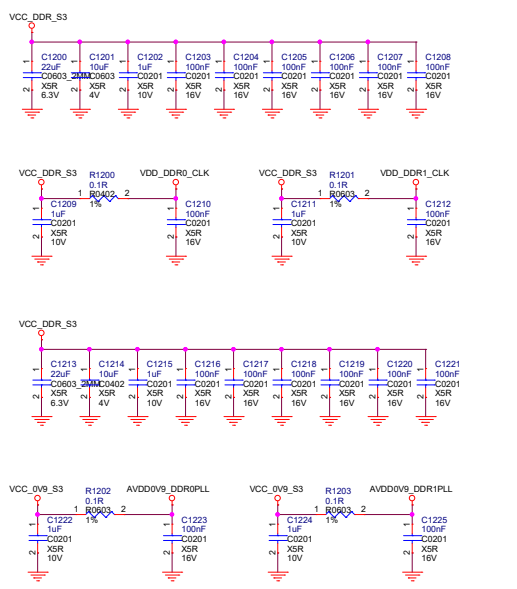


Title			
RK3399Pro_vmarc			
Size	Document Number	Rev	
A3	RK3399 Pro OSC/PMUIO1/PMUIO2	1.1	
Date:	Friday, December 18, 2020	Sheet	3 of 17

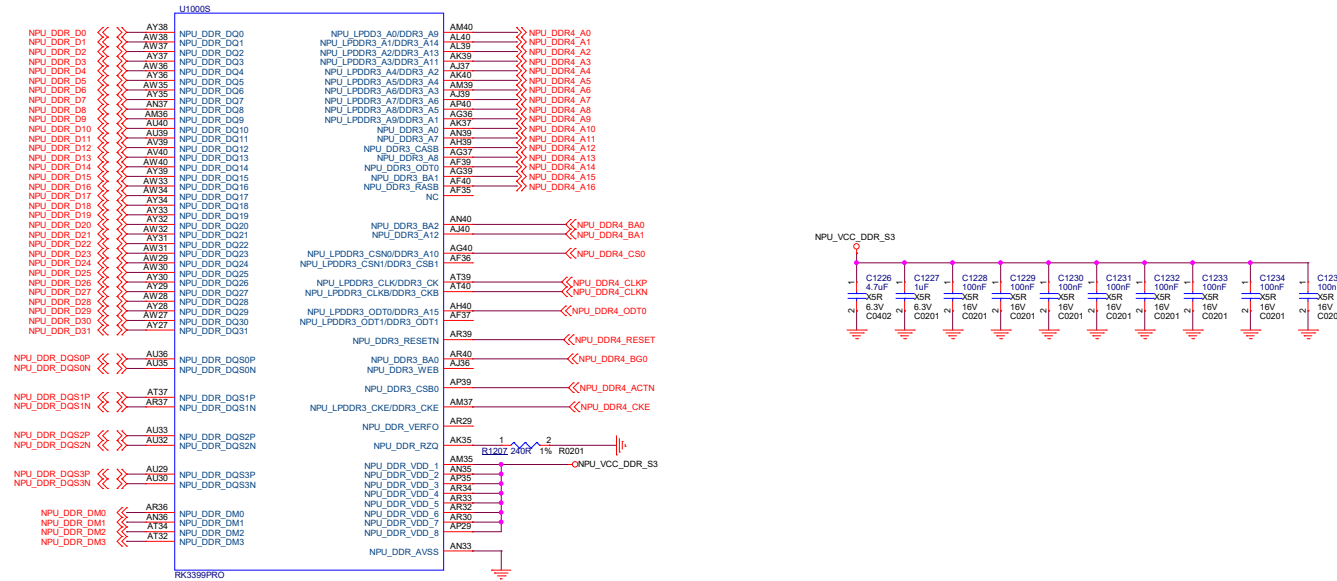
DDR Controller



DDR FILTER

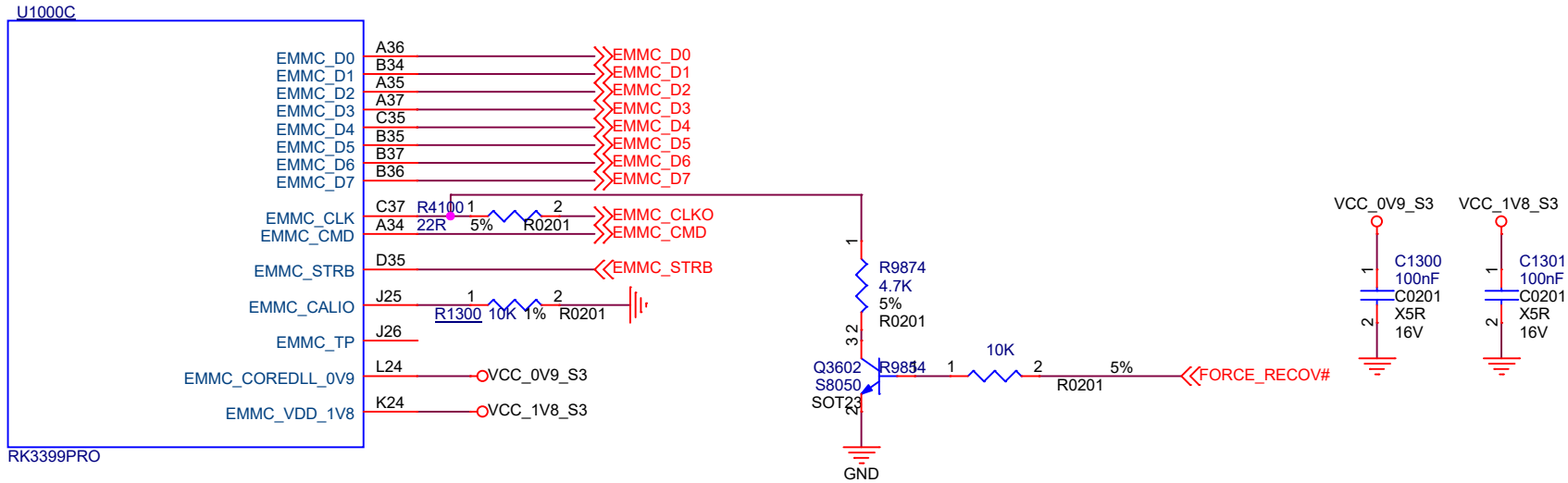


NPU DDR Controller

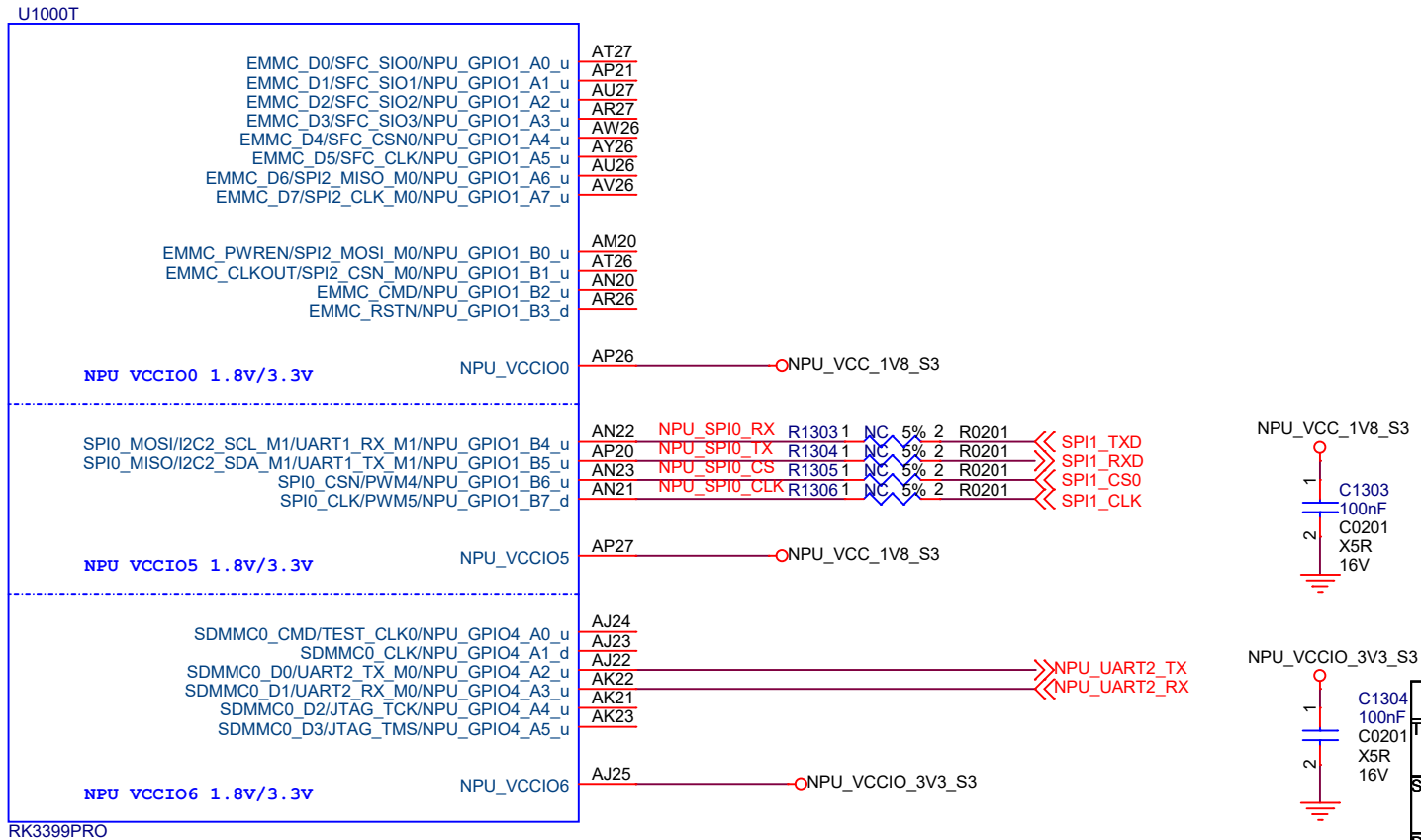


LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
A0	A0
A7	CASB
A0	ODT0
BA1	BA1
RASB	RASB
CSB0	CSB0
BA2	BA2
A12	A12
BA0	BA0
WEB	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN

EMMC Controller



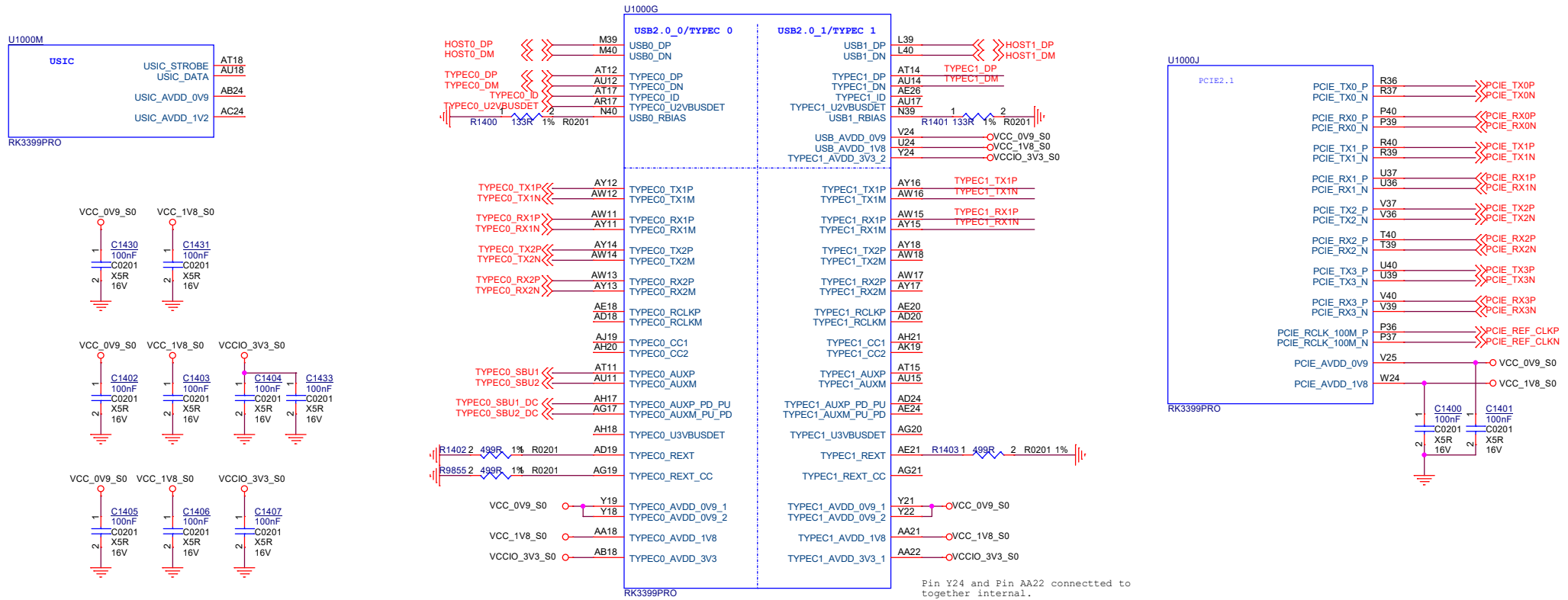
NPU EMMC Controller



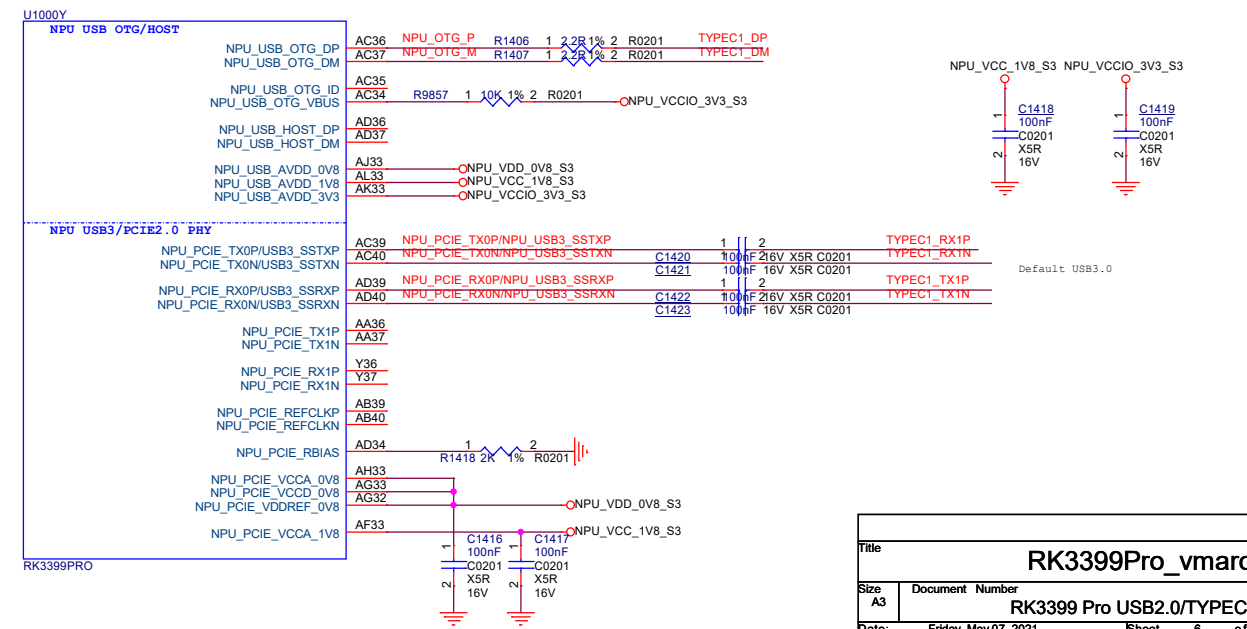
Title			RK3399Pro_vmarc		
Size	Document Number		Rev		
A4	RK3399 Pro EMMC/SPI		1.1		
Date:	Friday, May 07, 2021	Sheet	5	of	17

USB Controller

PCIe Controller



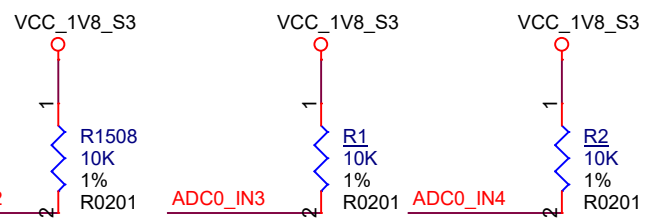
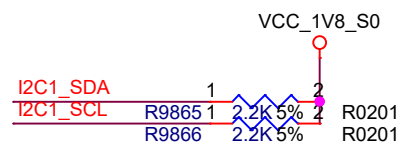
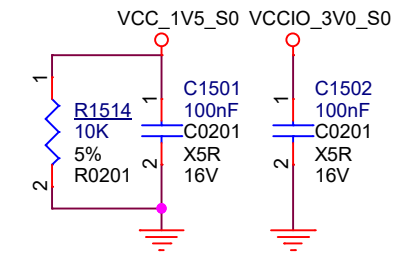
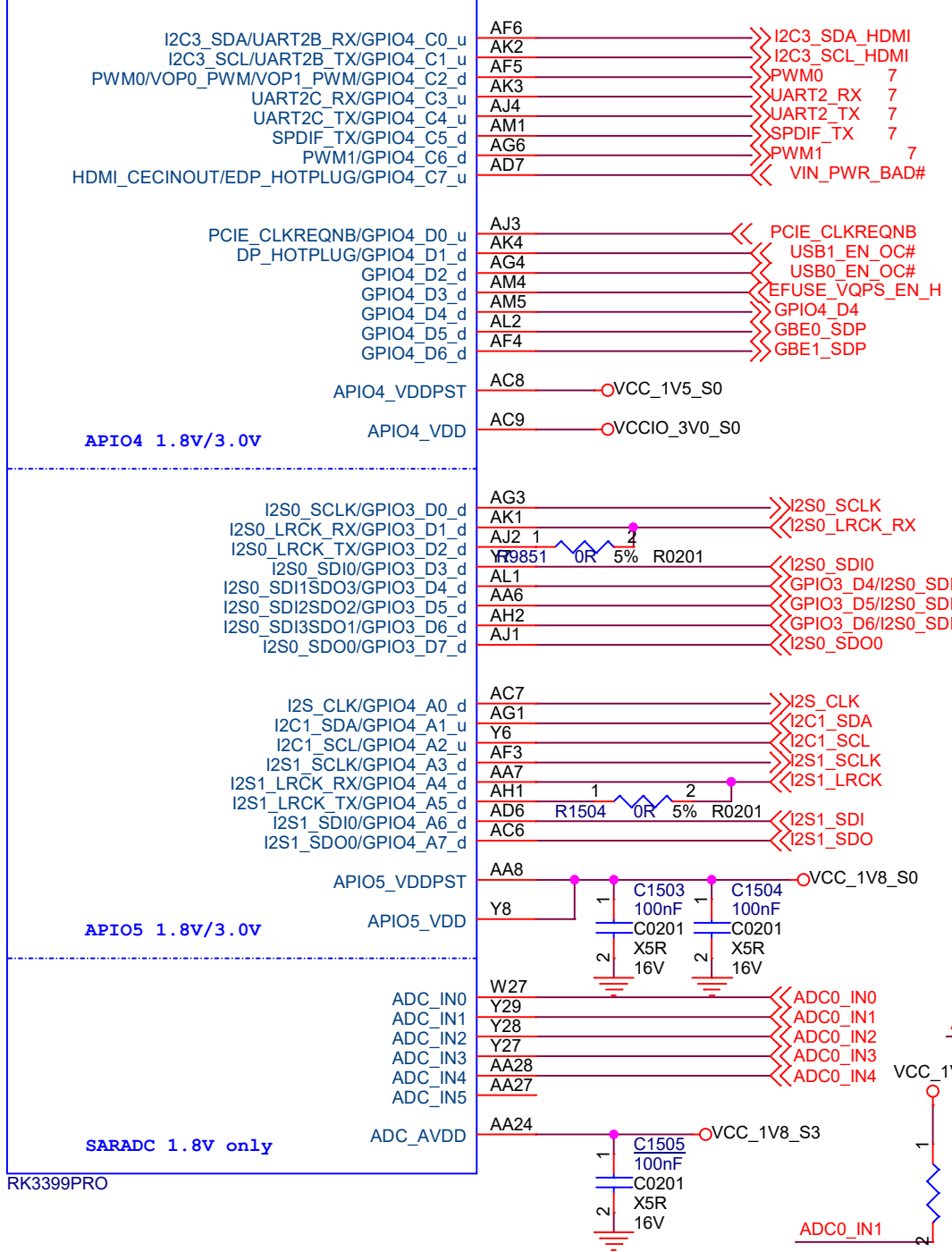
NPU PCIe/USB3.0 Controller



Title			
RK3399Pro_vmarc			
Size	Document Number	Rev	
A3	RK3399 Pro USB2.0/TYPEC/PCI E	1.1	
Date:	Friday, May 07, 2021	Sheet	6 of 17

GPIO/SARADC

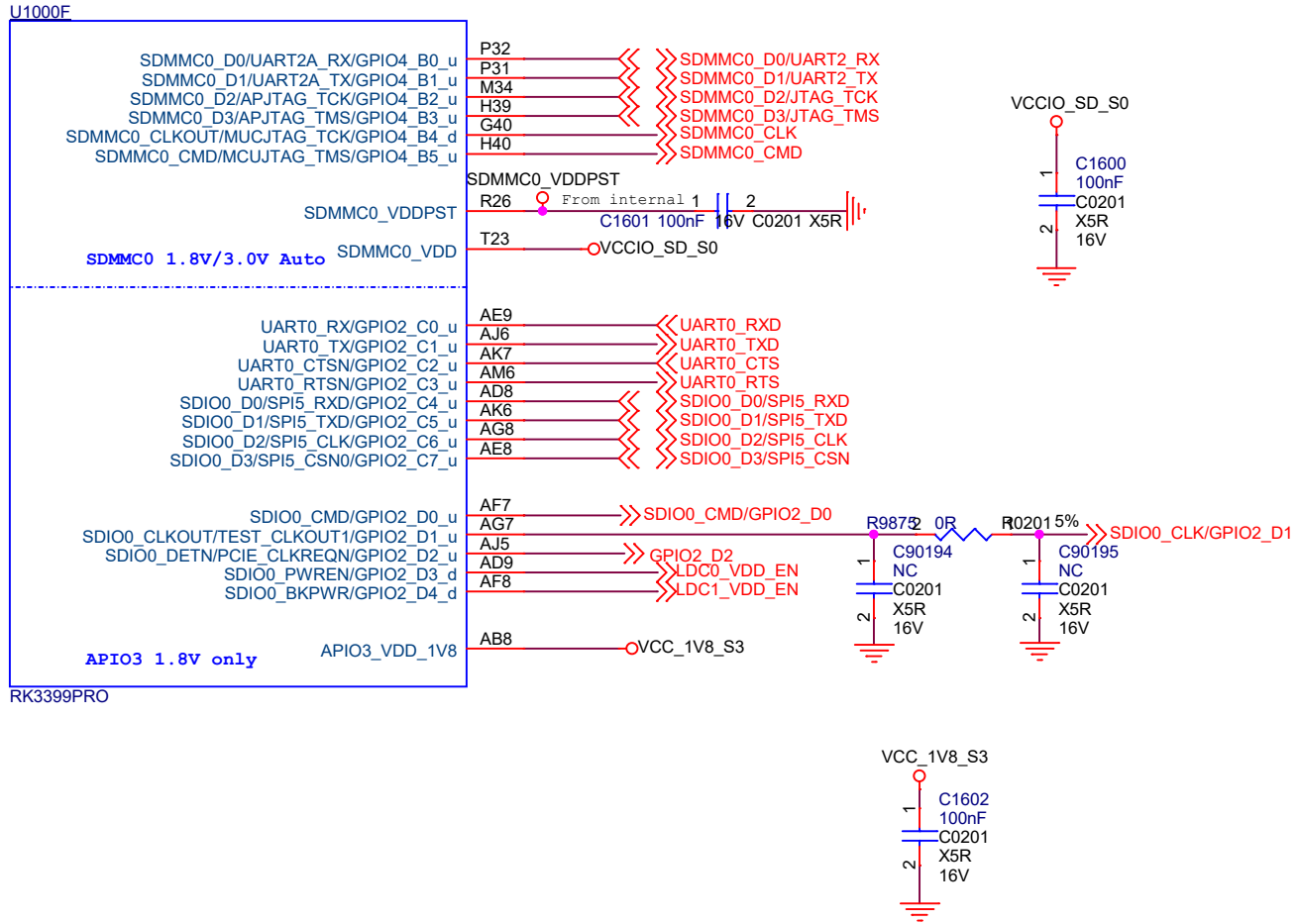
U1000N



Title		
RK3399Pro_vmarc		
Size	Document Number	Rev
A	RK3399 Pro SARADC/GPIO	1.1
Date:	Friday, May 07, 2021	Sheet 7 of 17

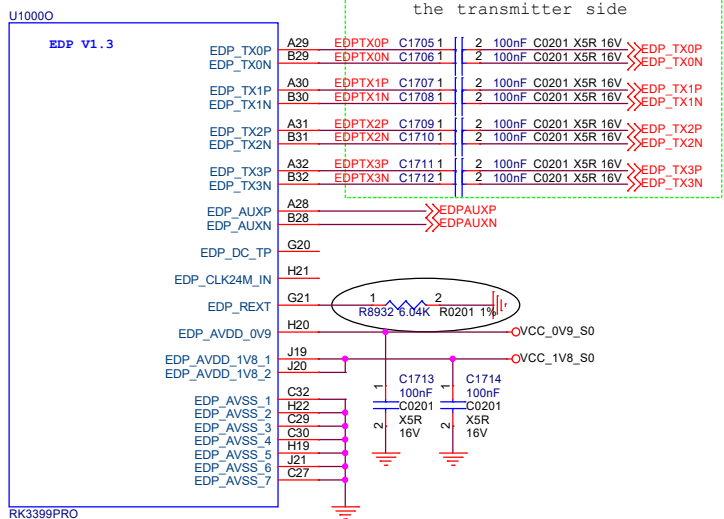
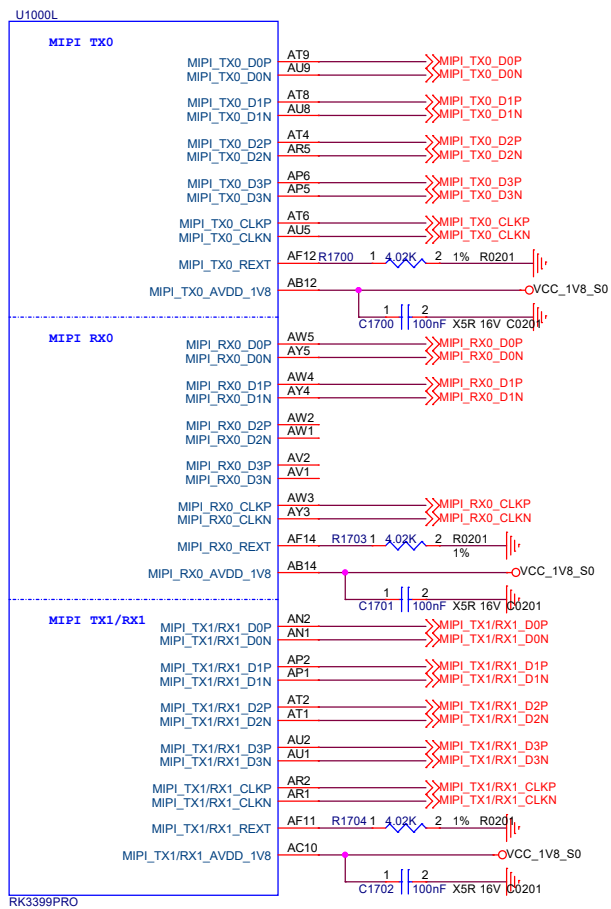
RK3399PRO

SDMMC0/SDIO0 Controller



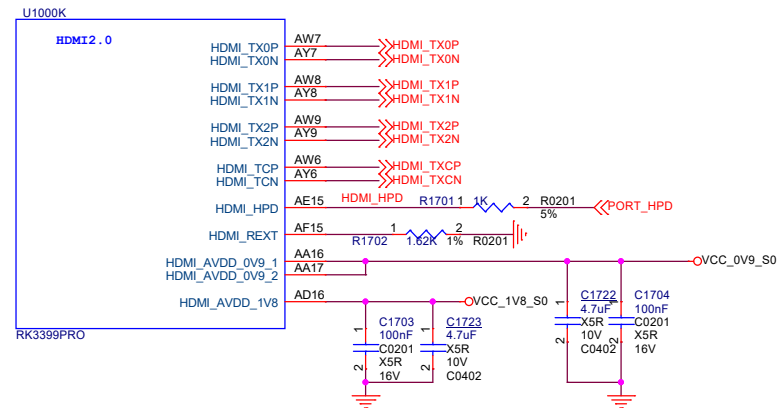
Title			RK3399Pro_vmarc		
Size	Document Number	Rev			
A4	RK3399 Pro SDMMC0/SDMMC1	1.1			
Date:	Friday, May 07, 2021	Sheet	8	of	17

MIPI CSI/DSI Controller

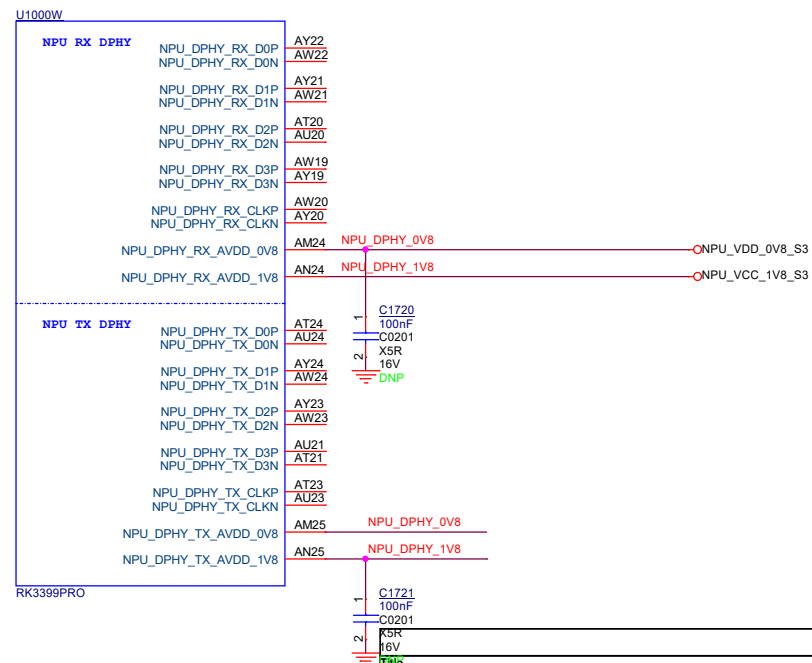


EDP Controller

HDMI Controller



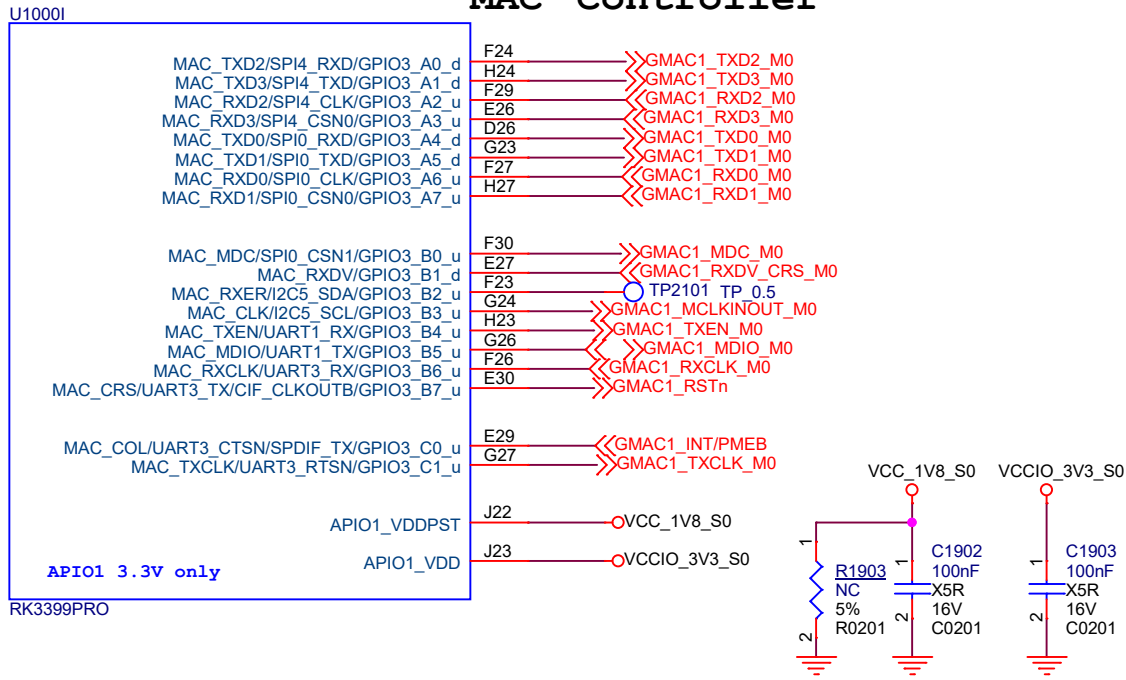
NPU MIPI DSI/CSI Controller



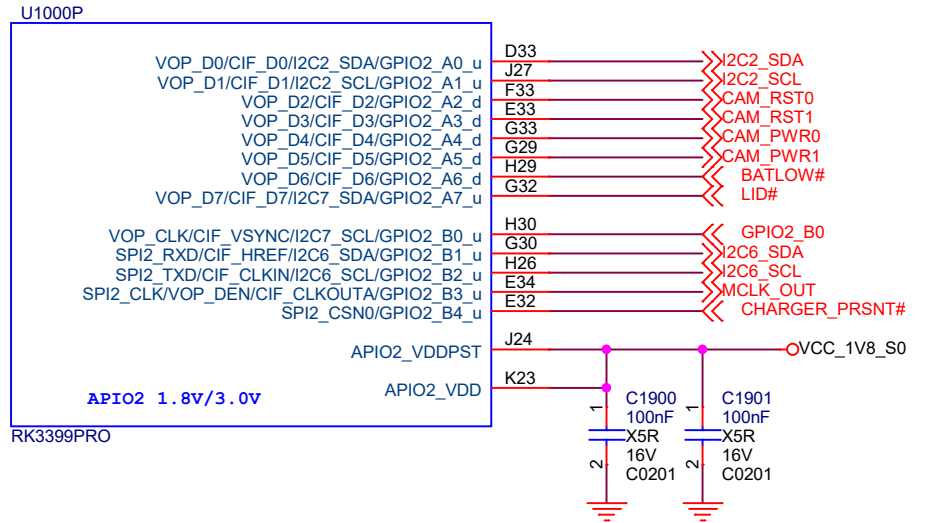
RK3399Pro_vmarc

Size	A3	Document Number	RK3399 Pro Display	Rev	1.1
Date:	Friday, May 07, 2021	Sheet	9	of	17

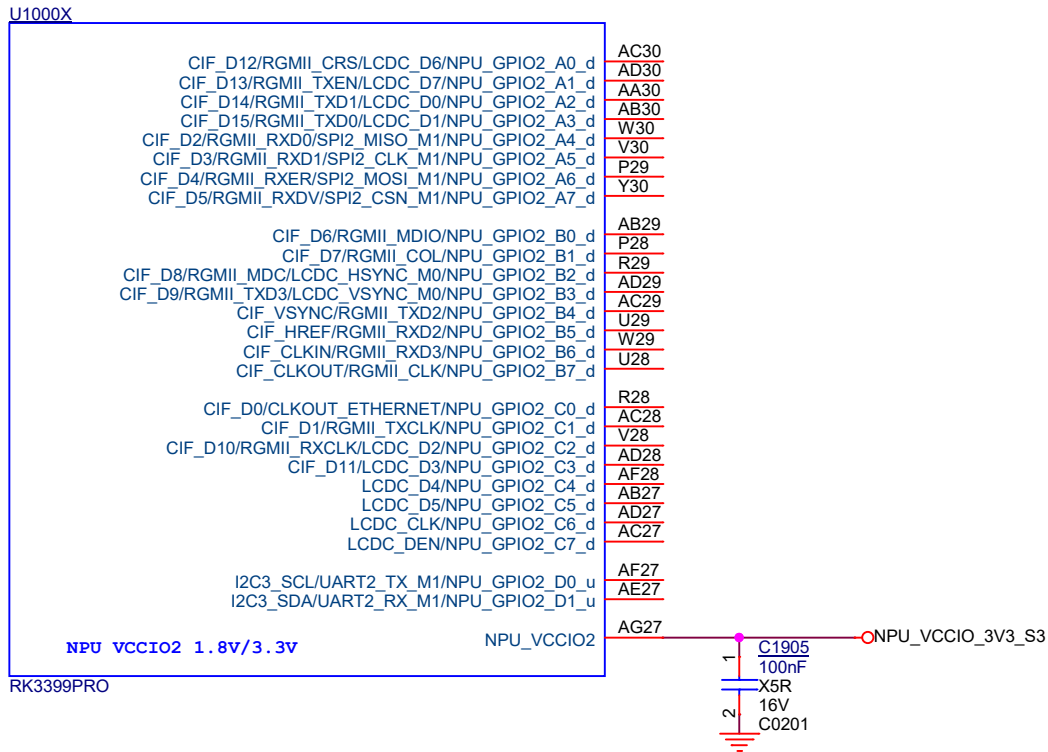
MAC Controller



VOP/CIF Controller

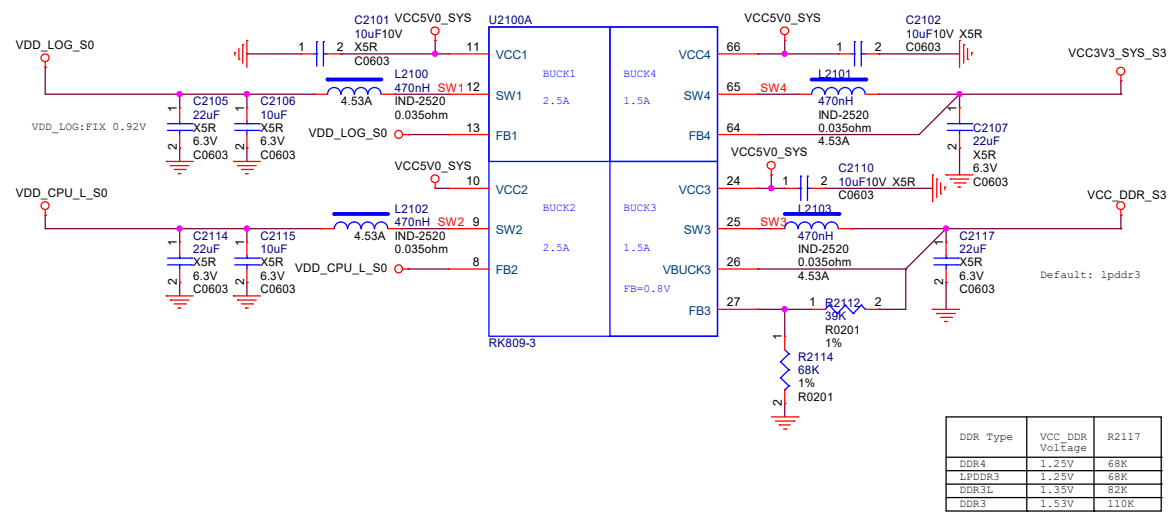


NPU CIF/RGMII/LCDC Controller



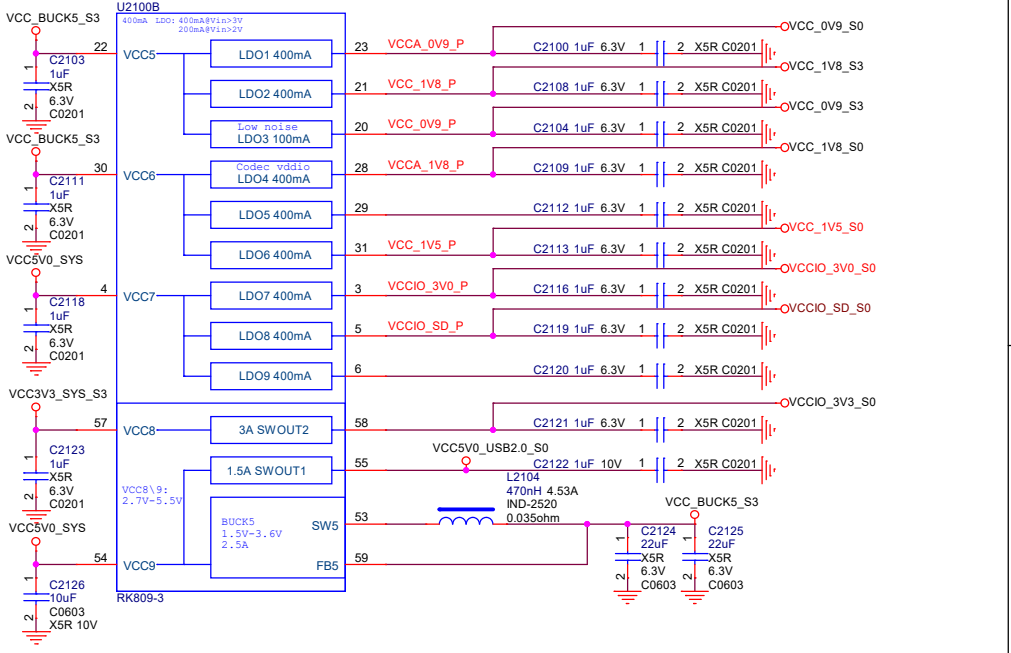
Title			RK3399Pro_vmarc		
Size	Document Number		Rev		
A4	RK3399 Pro RGMII/LCDC/CIF		1.1		
Date:	Tuesday, June 15, 2021	Sheet	10	of	17

PMIC RK809-3 DCDC

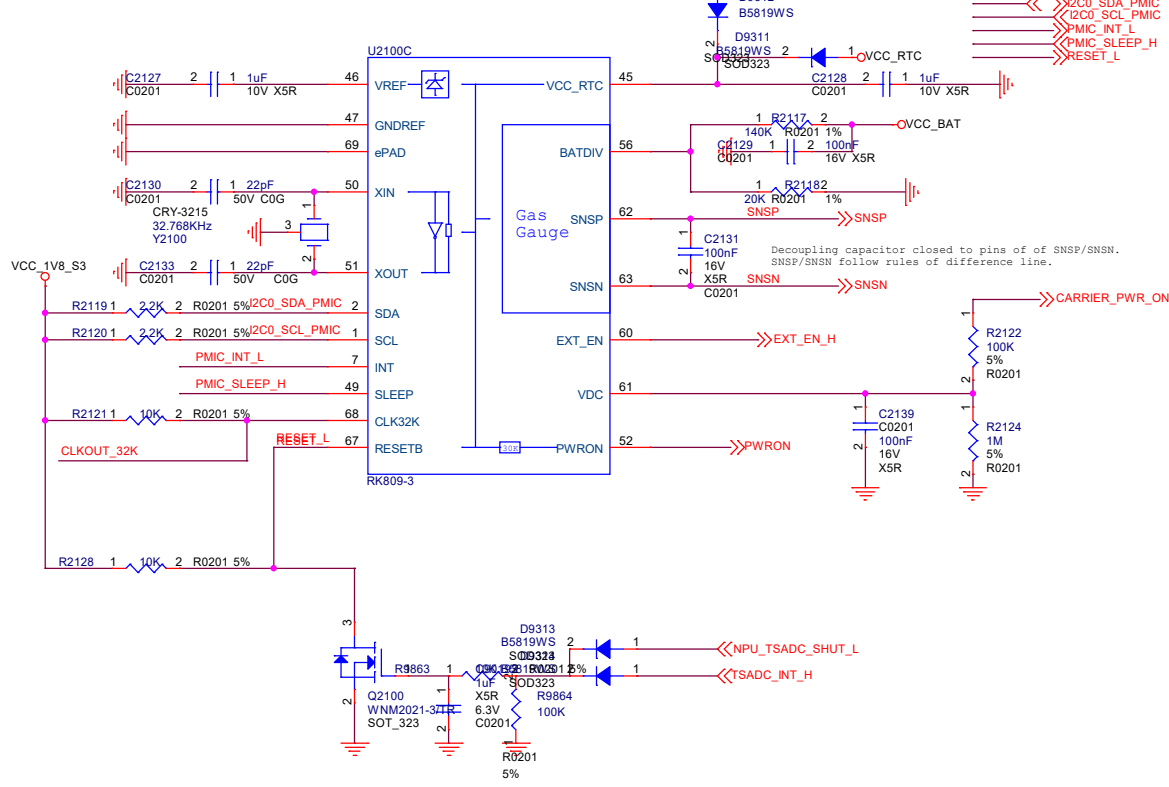


DDR Type	VCC_DDR Voltage	R2117
DDR4	1.25V	68K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	110K

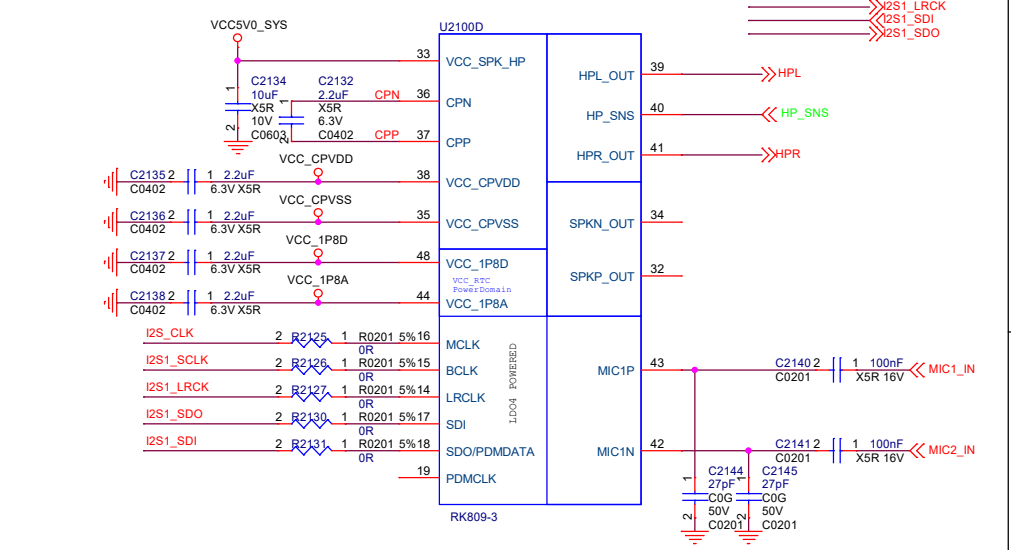
PMIC RK809-3 LDO



PMIC RK809-3 Management

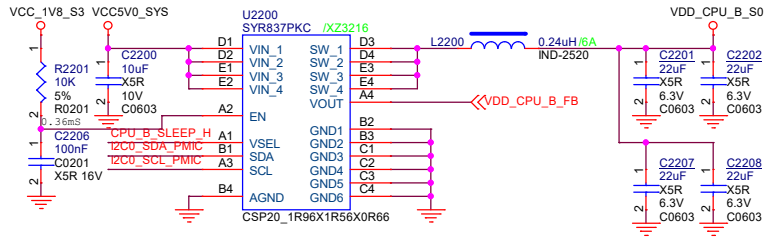


PMIC RK809-3 CODEC

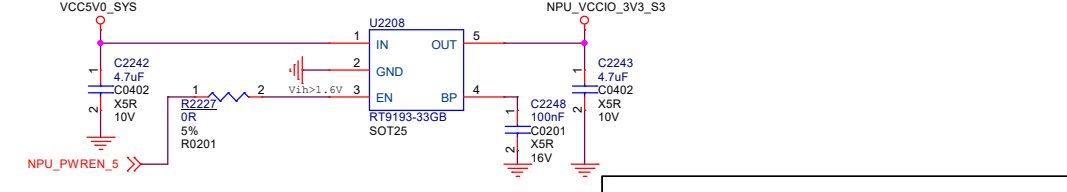
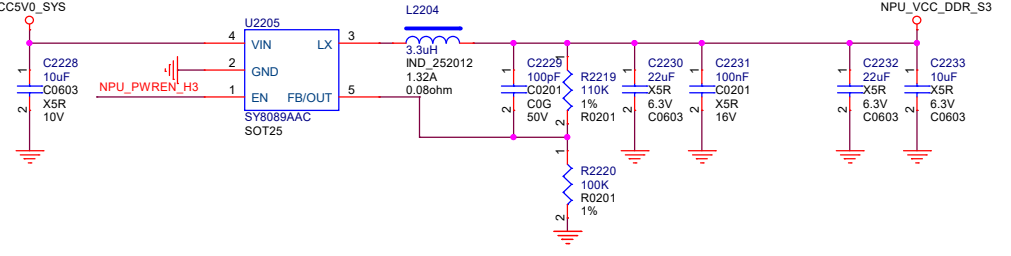
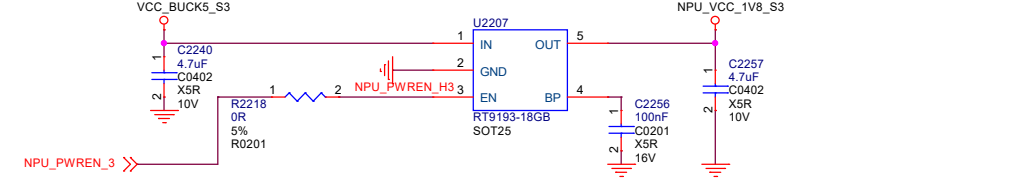
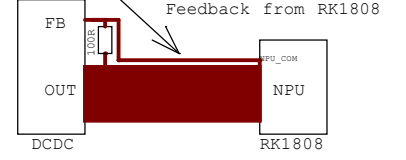
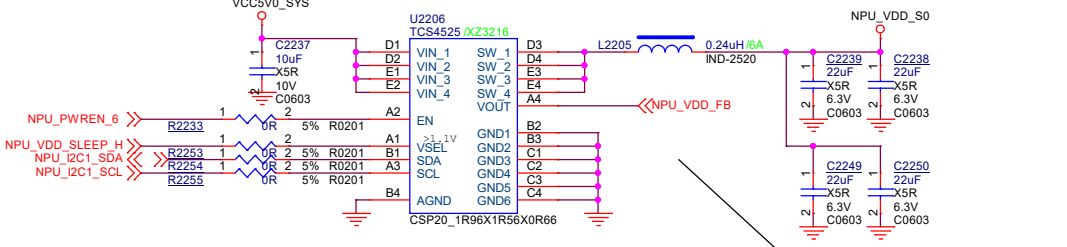
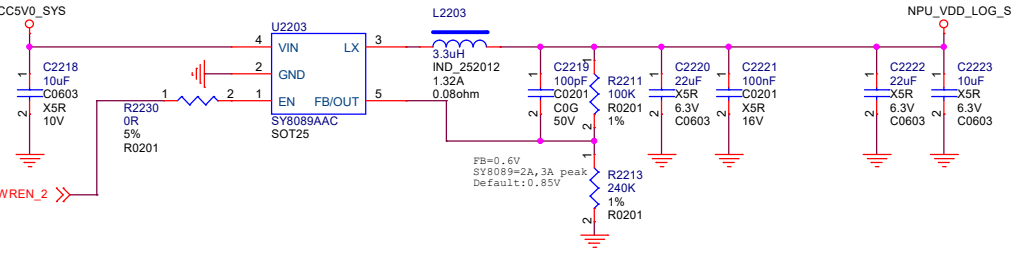
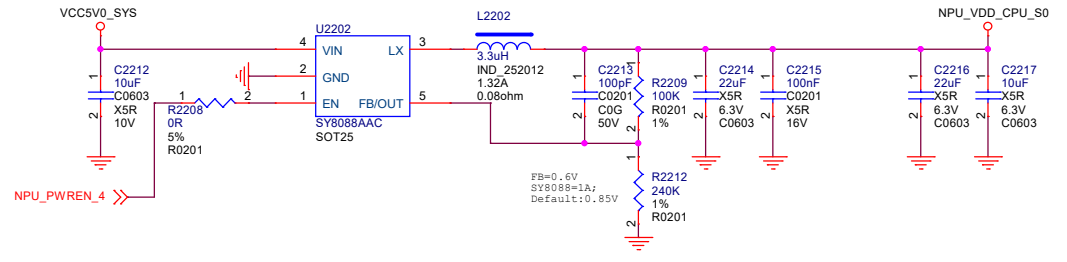
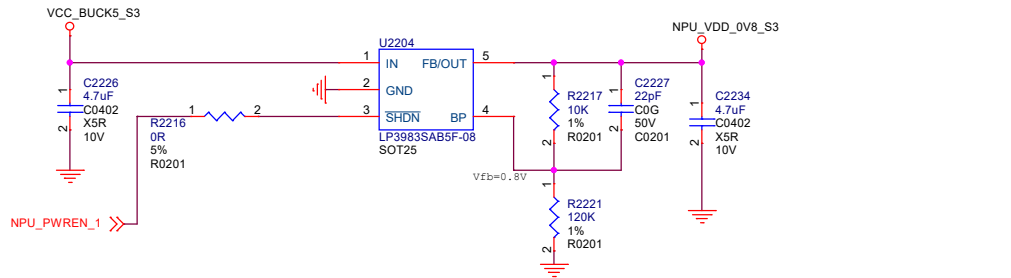
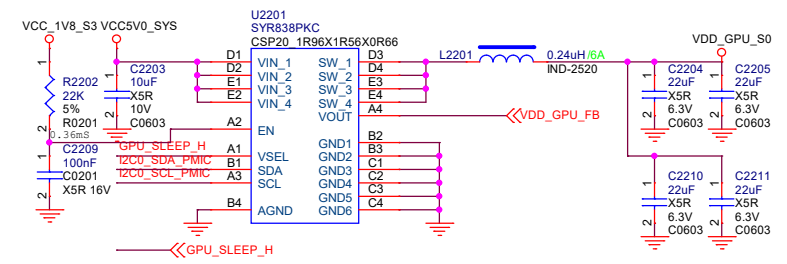


Title				RK3399Pro_vmarc	
Size A3	Document Number	Power-PMIC RK809-3		Rev	1.1
Date:	Friday, May 07, 2021	Sheet	11	of	17

VDD_CPU_B power



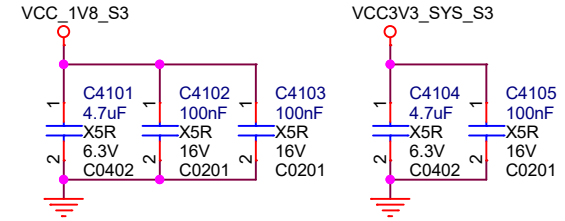
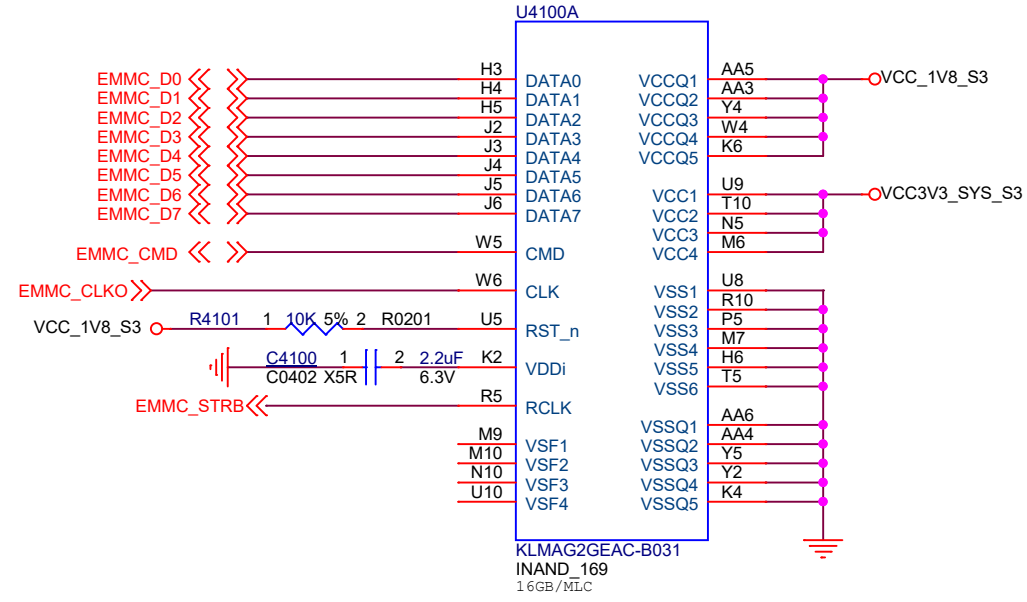
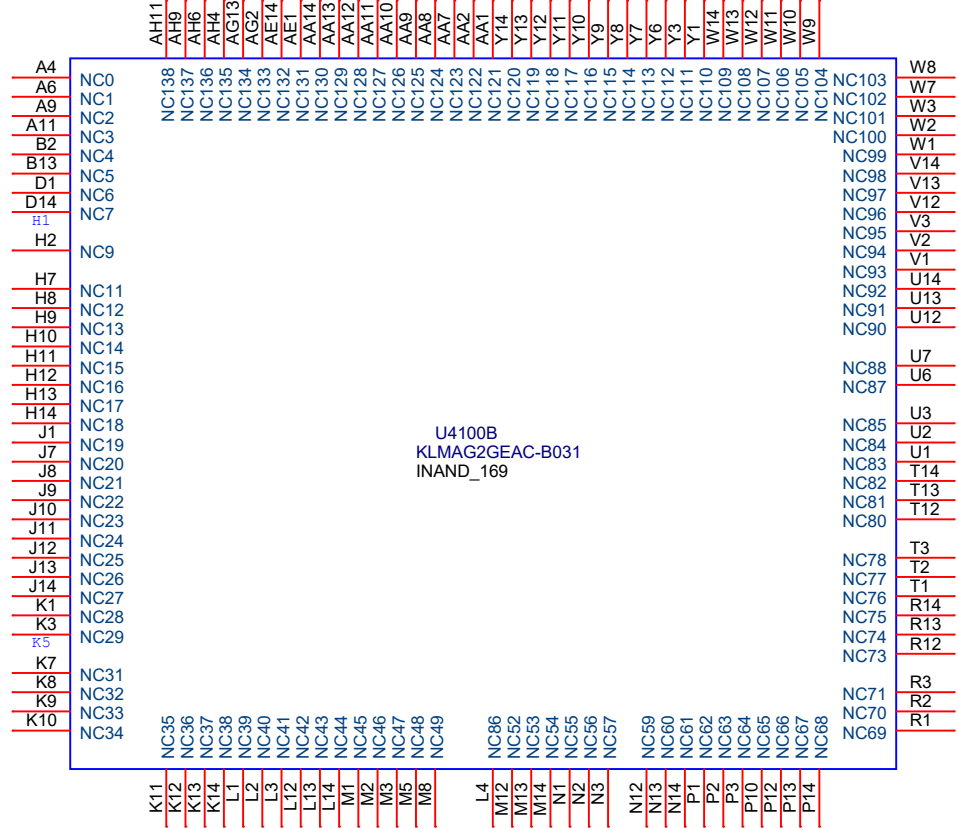
VDD_GPU power



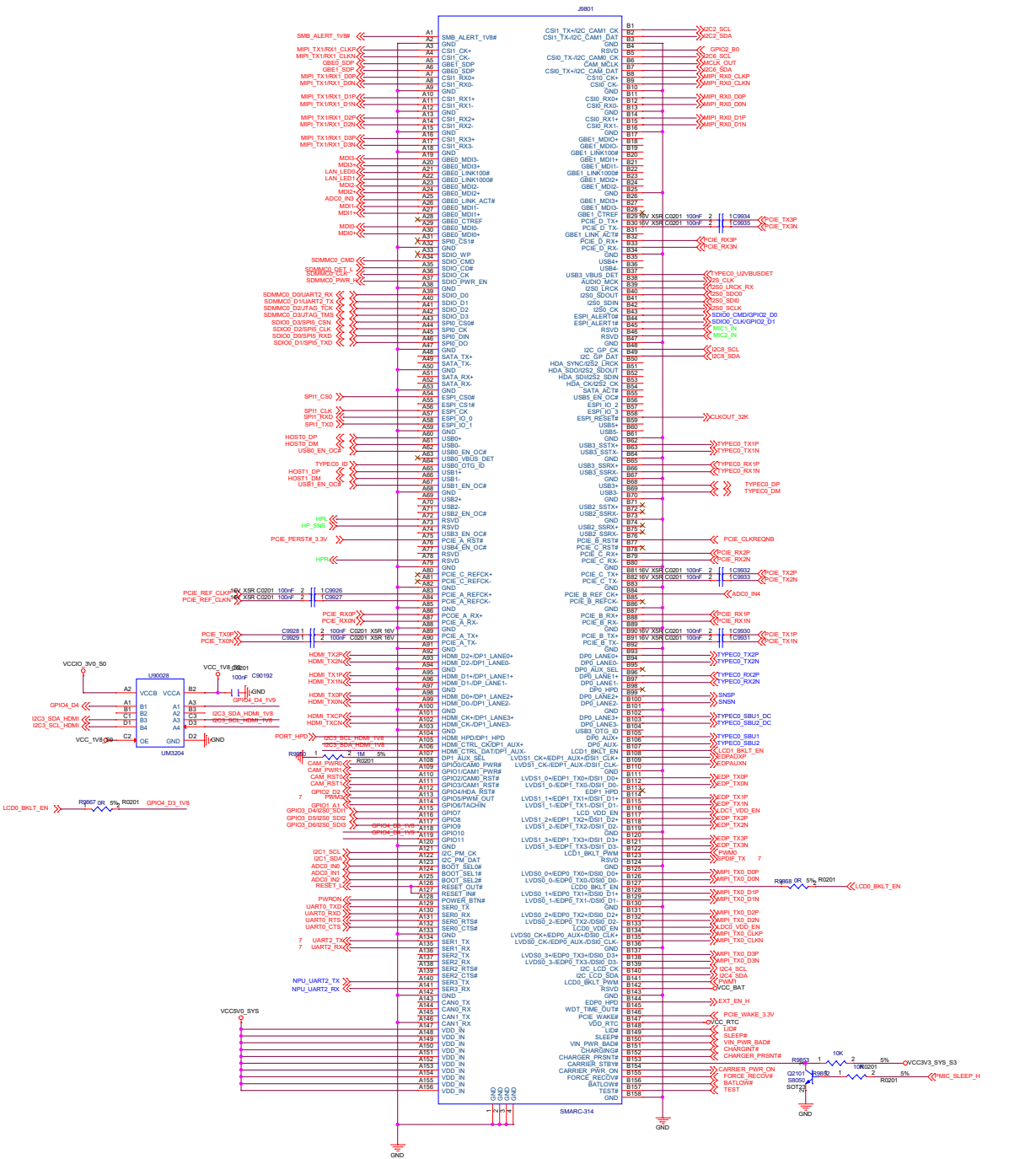
NPU Part power

Title				RK3399Pro_ymarc	
Size	A3	Document Number	POWER-CPU/GPU/NPU		Rev
Date:	Friday, May 07, 2021	Sheet	12	of	17

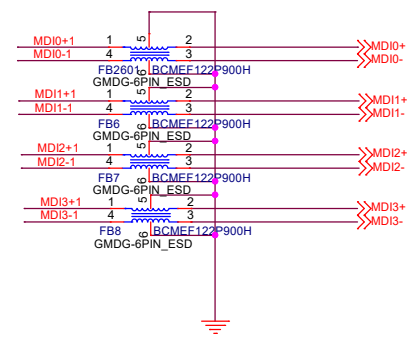
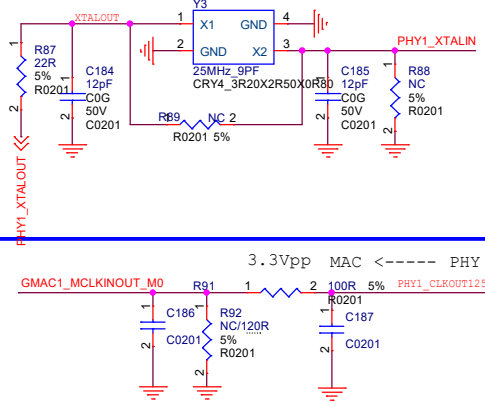
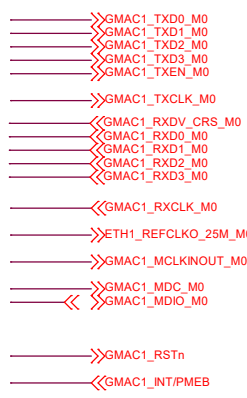
eMMC



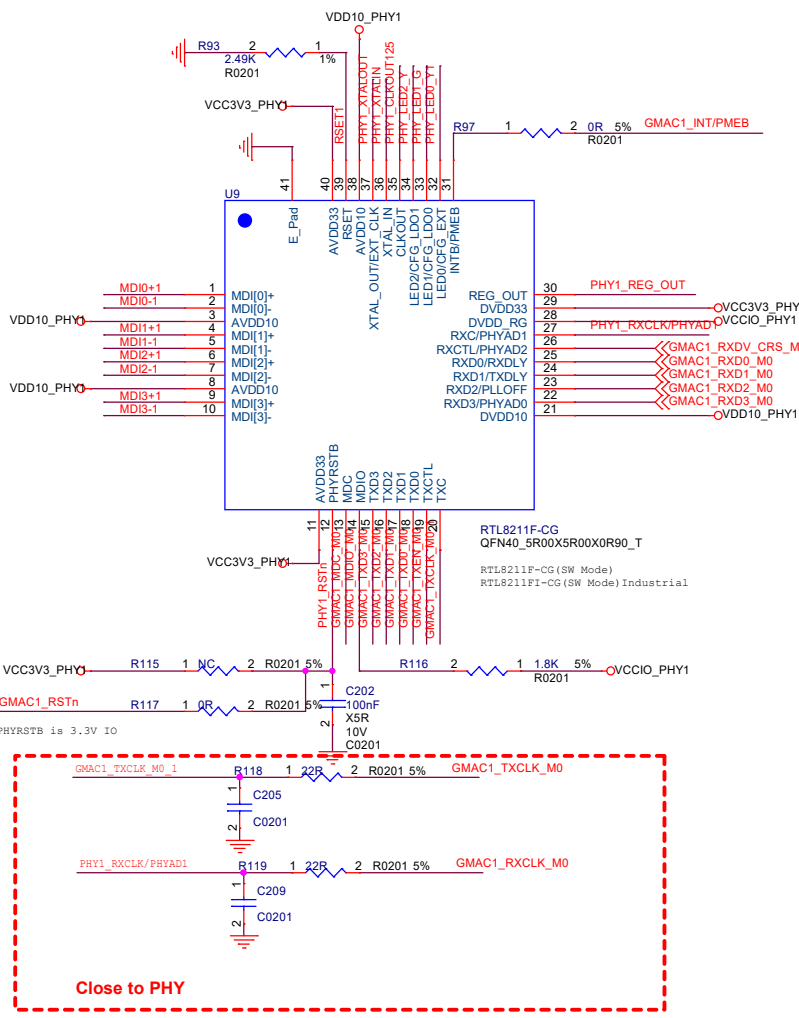
Title			RK3399Pro_vmarc		
Size	Document Number				Rev
A4	EMMC				1.1
Date:	Friday, May 07, 2021		Sheet	15	of 17



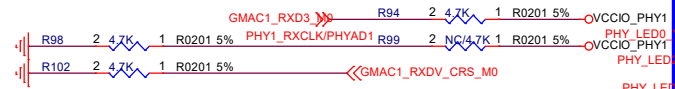
Ref	Document Number	Rev
	RK3399Pro_vmarc	1.1
Desc	CONNECT	
Clusm		
Date	Monday, June 21, 2021	Sheet 17 of 17



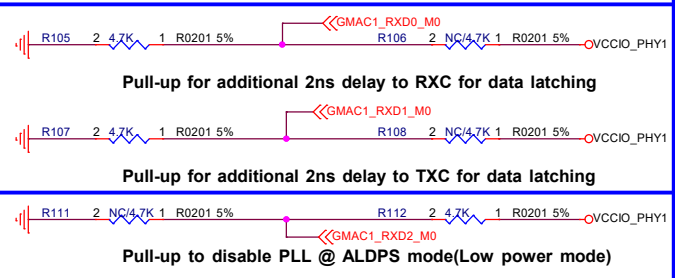
RGMI Power Source	CFG EXT	CFG LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V(default)	1'b0	2'b10



VCC_PHY1_IO Voltage Config



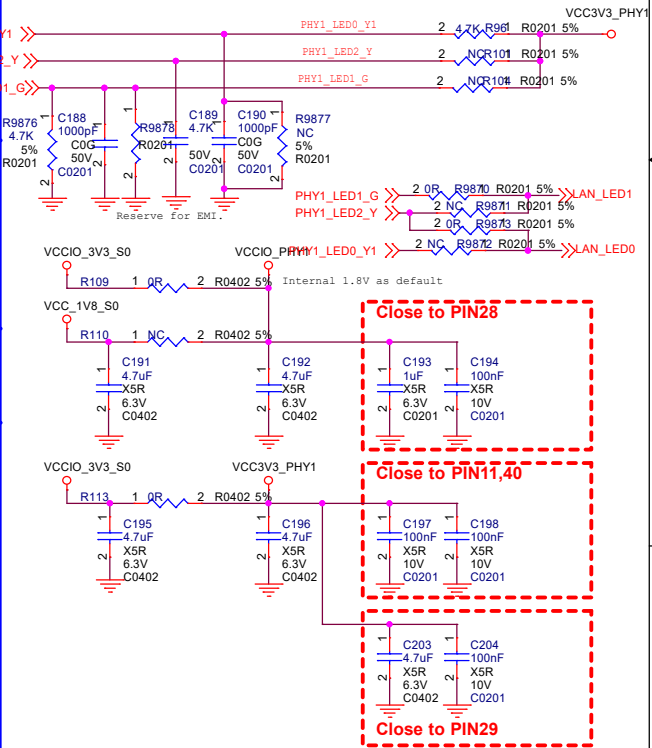
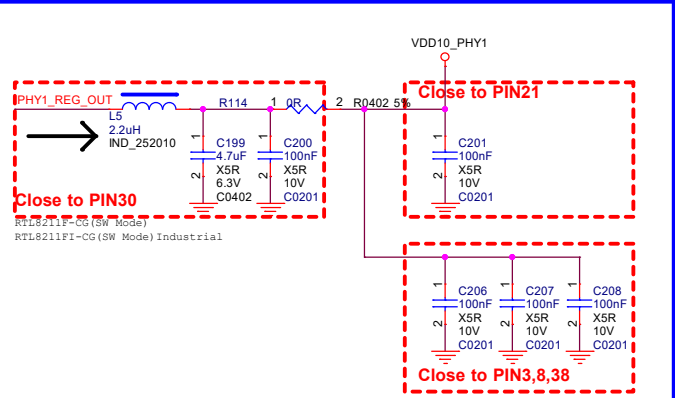
PHY Address Config



Pull-up for additional 2ns delay to RXC for data latching

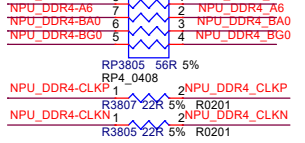
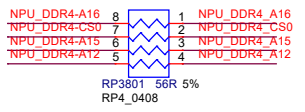
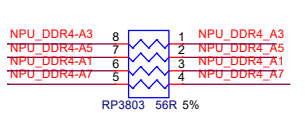
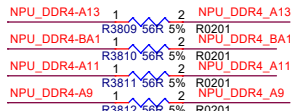
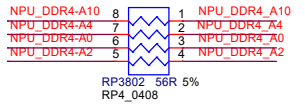
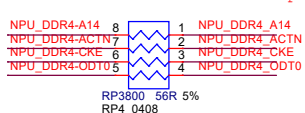
Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)

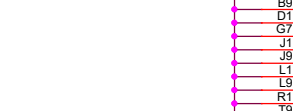
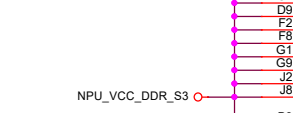
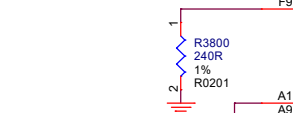
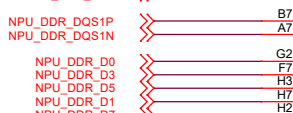
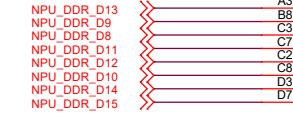


NPU DDR4 2x16bit

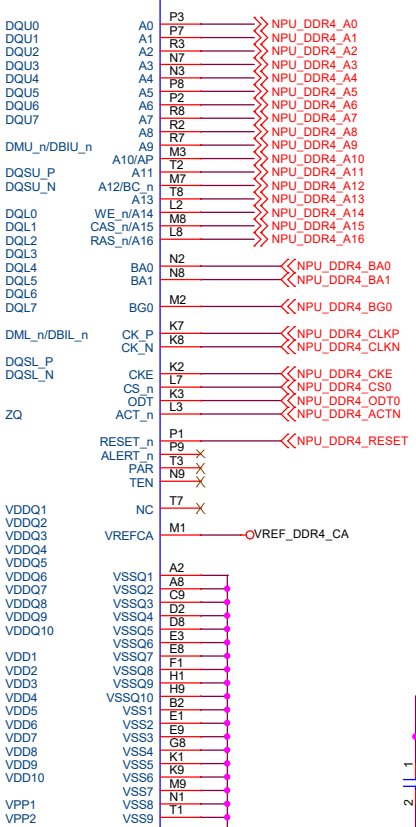
Note: The simulation frequency of the template is 1066MHz.
Refer to the latest AVL for parts selection.



For Daisy Chain Scheduling

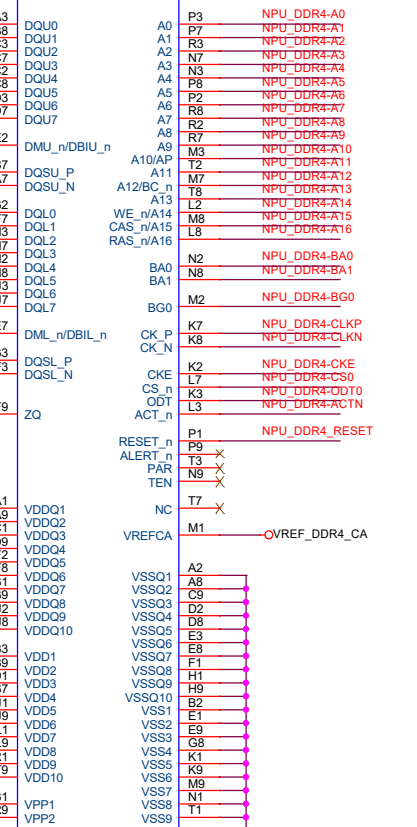


U3800
DDR4X16
FBGA96 14R00X11R00X1R20

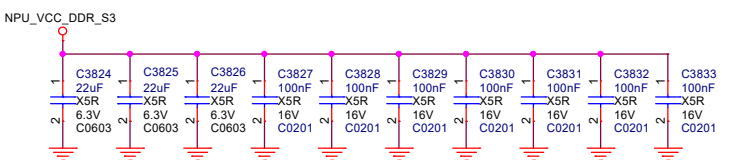
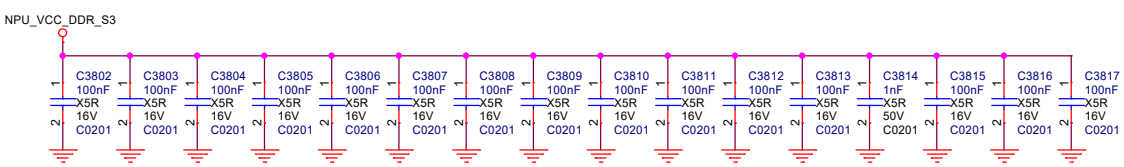
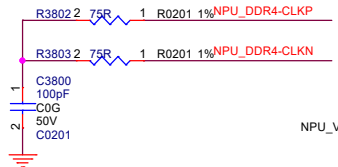


K4A8G165MB-BCPB
DDR4-2133(15-15-15)
512MR16

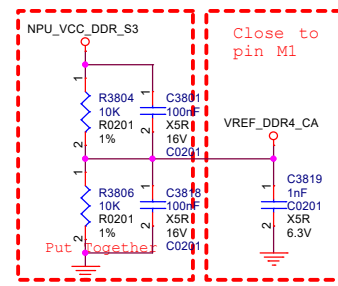
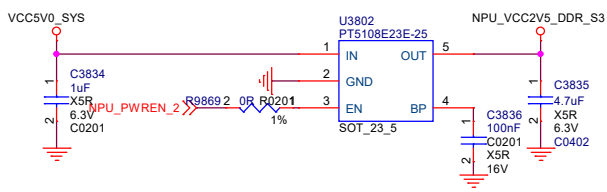
U3801
DDR4X16
FBGA96 14R00X11R00X1R20



Date can be switched in group.



VDD(1.25V): Supply Voltage
VDDQ(1.25V): Supply Voltage for output
VPP(2.5V): Peak to Peak Voltage
VPP must be equal or greater than VDD/VDDQ at all times.



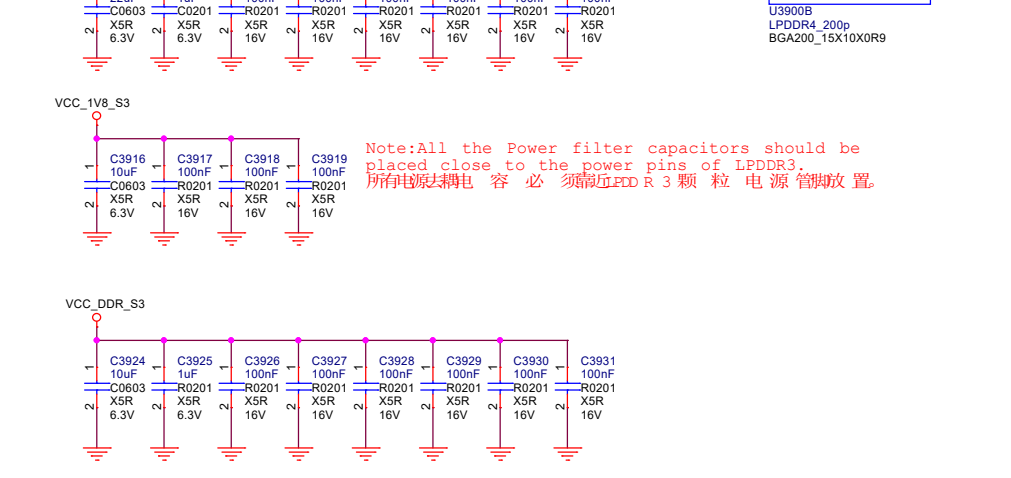
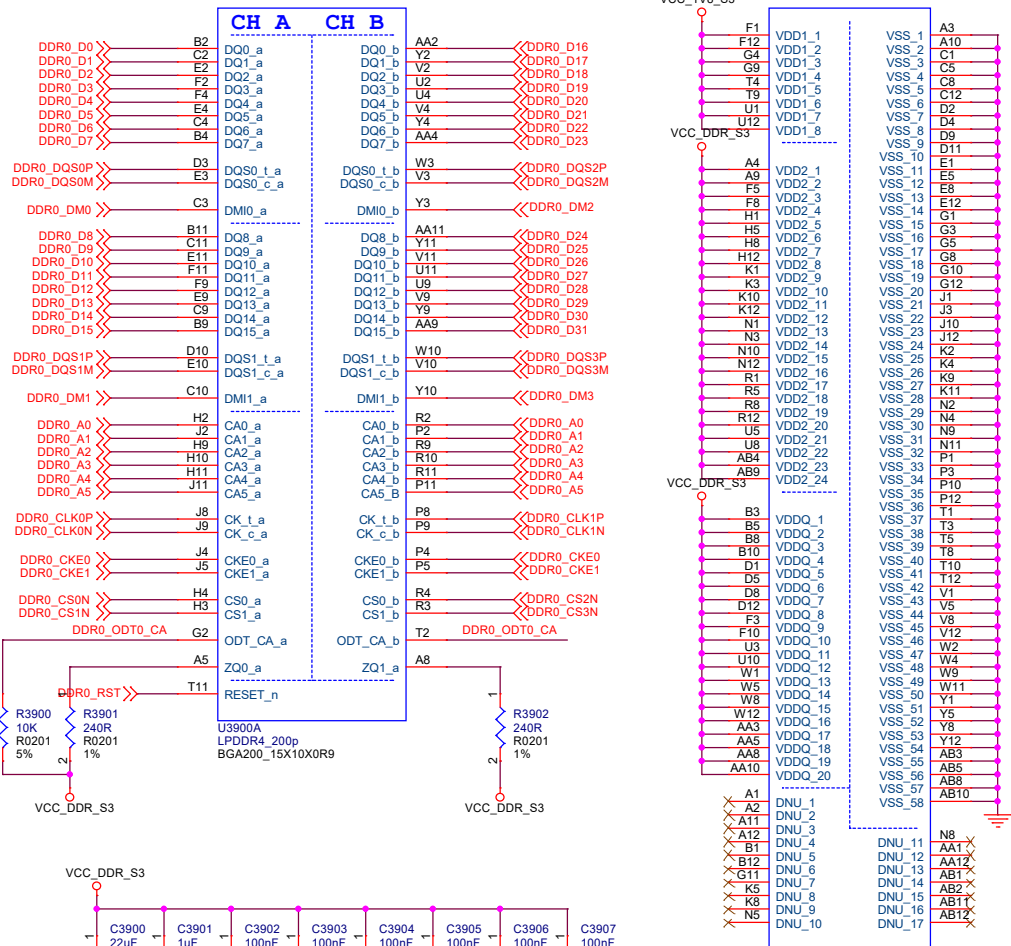
Note: All the Power filter capacitors should be placed close to the power pins of DDR4.
所有电源去耦电容 必须靠近DDR 4 颗粒 电源管脚放置。

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

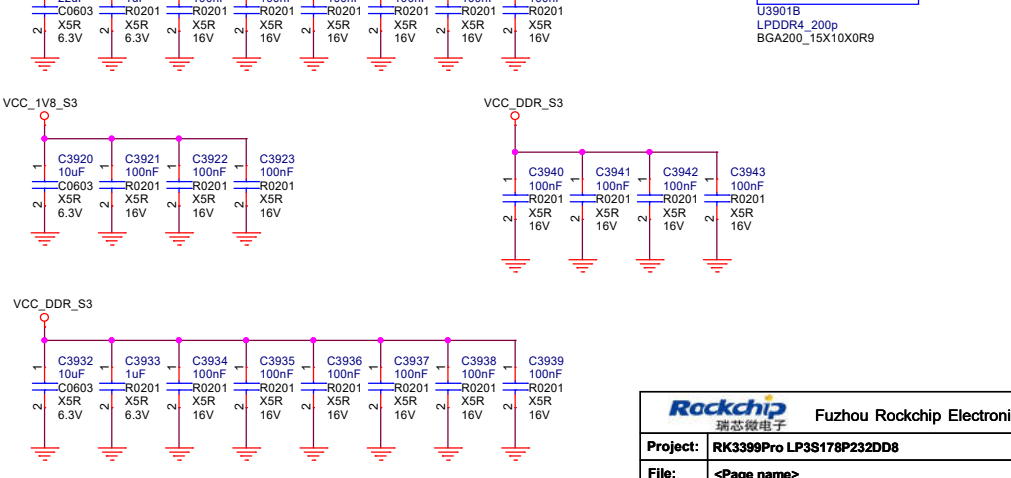
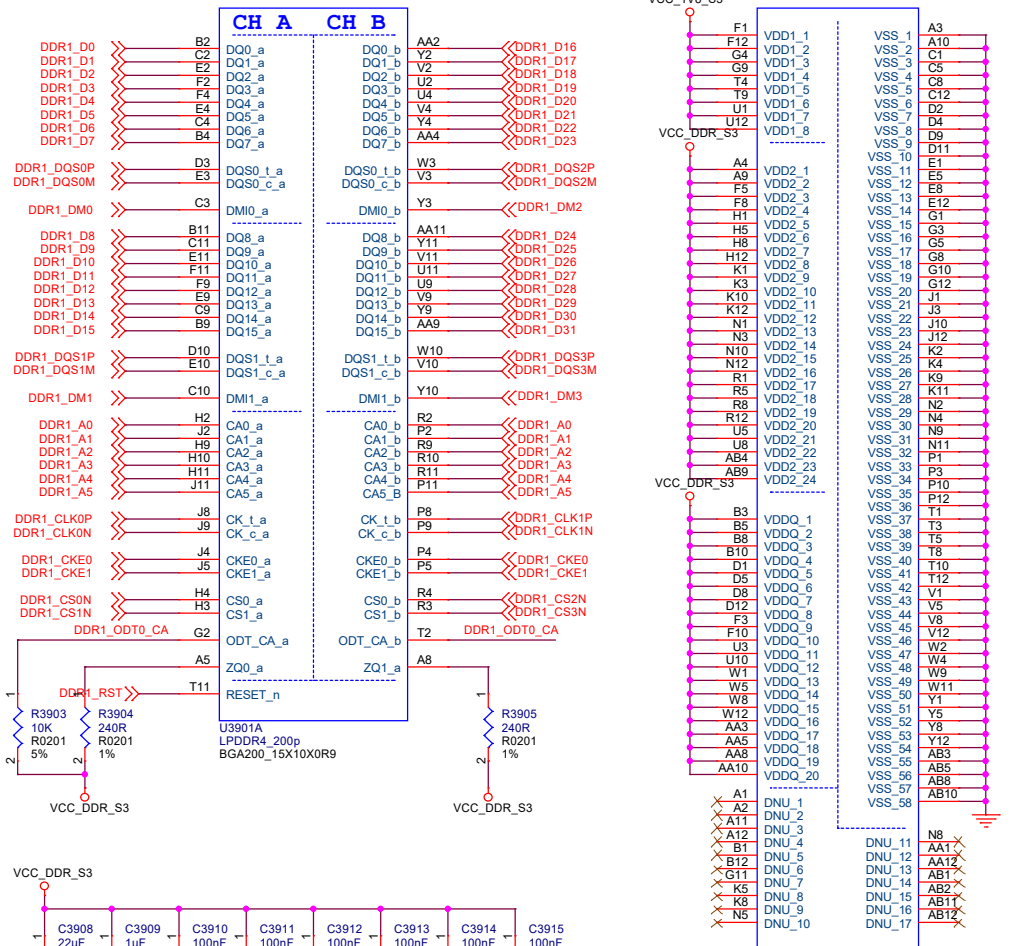
Project:	RK3399Pro LP3S178P232DD8
File:	RAM DDR4 4x16bit
Date:	Friday, May 07, 2021
Designed by:	XIAOHF
Rev:	V1.0
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LPDDR4 2x32bit 200ball

Note: The simulation frequency of the template is 800MHz.
 Refer to the latest AVL for parts selection.
 All the data can't be swap



Note: All the Power filter capacitors should be placed close to the power pins of LPDDR3.
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Designed by: Linus.Lin Reviewed by: <Checker> Rev: V1.1 Sheet: 27 of 46