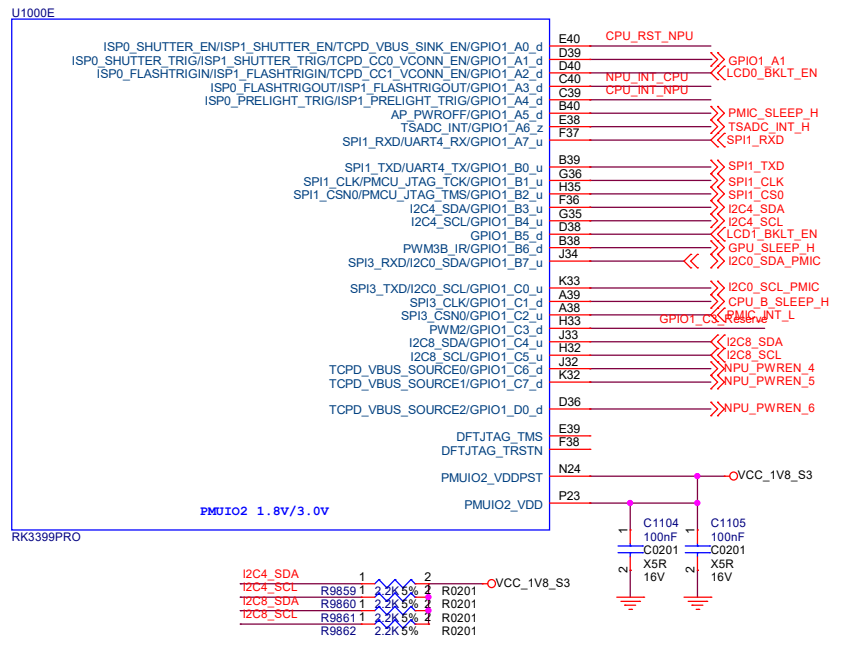
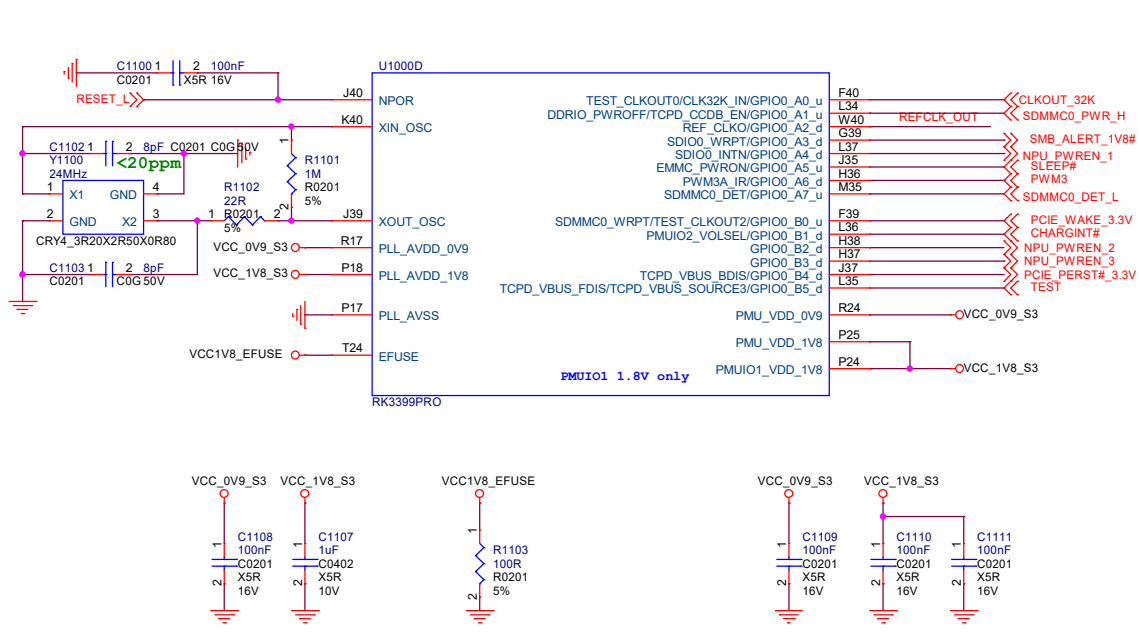
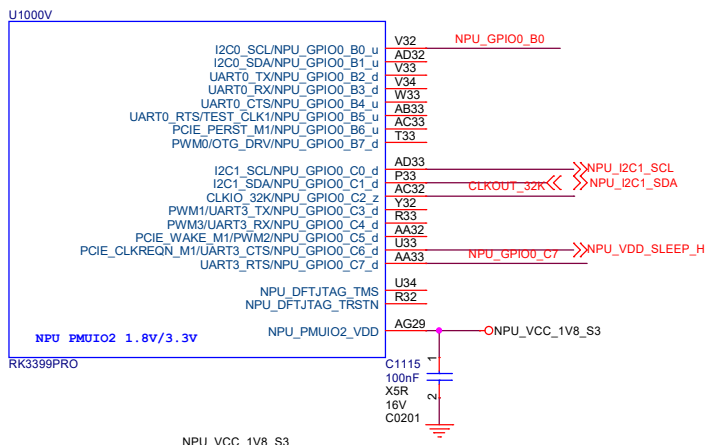
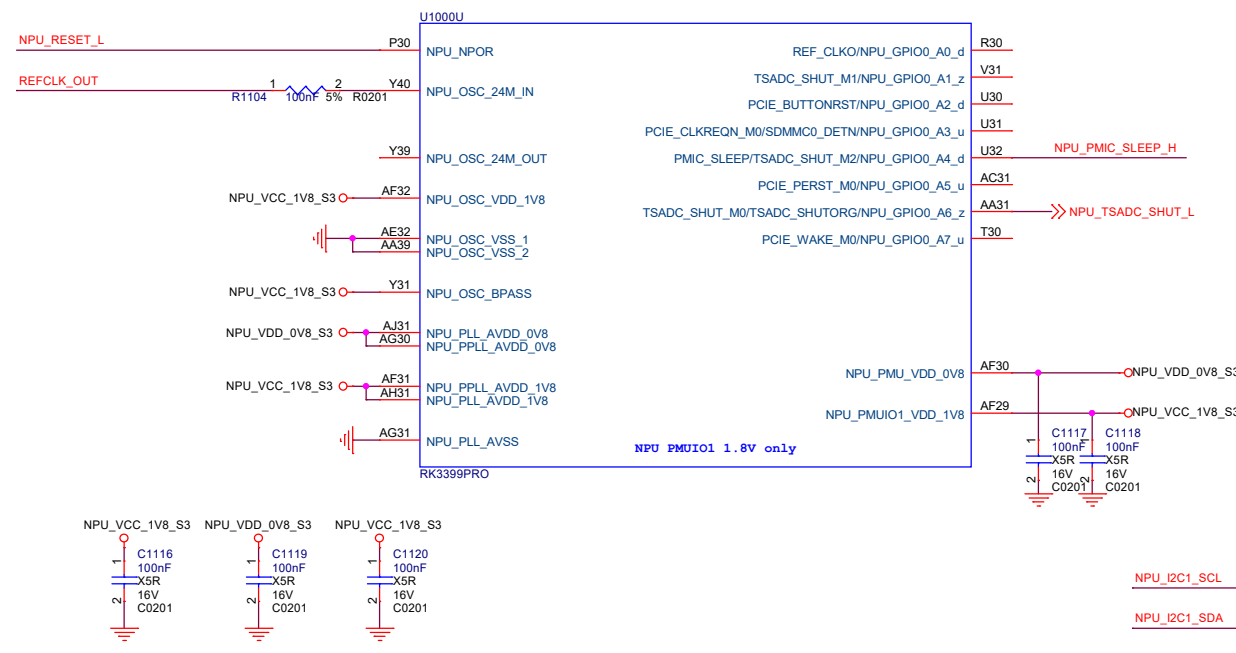
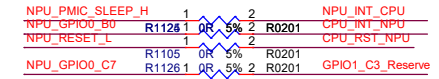


PMUIO1/PMUIO2

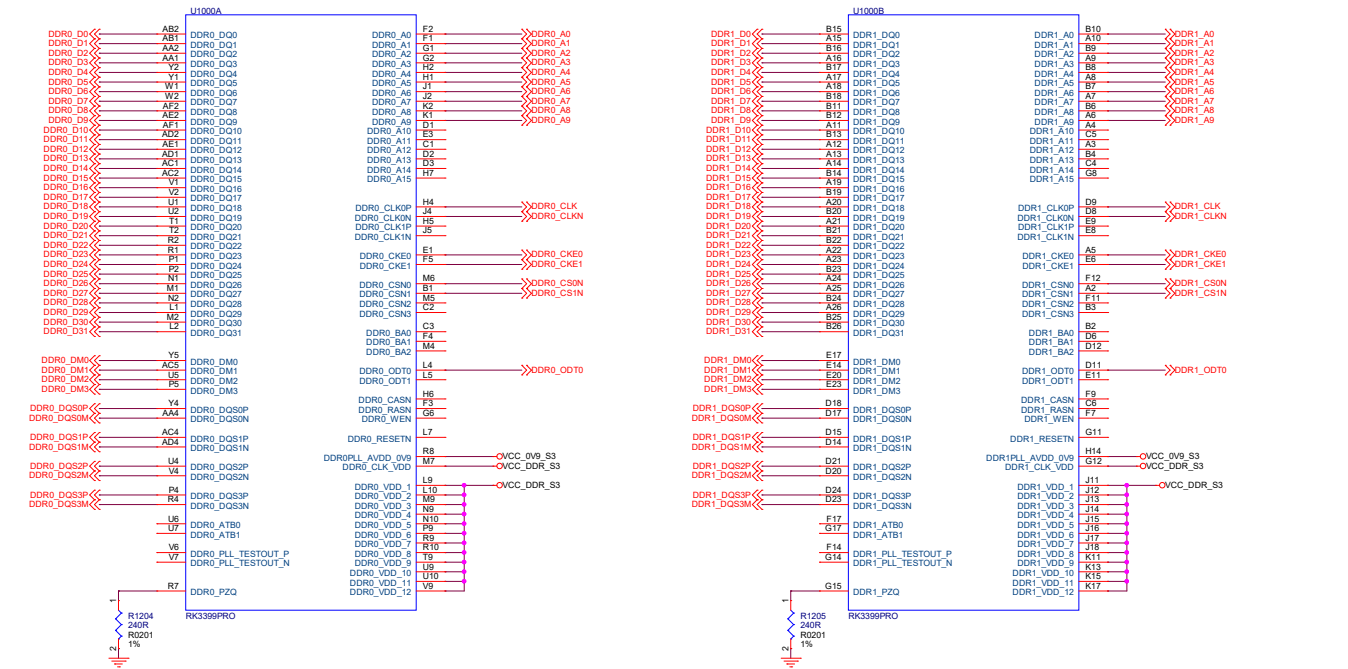


NPU PMUIO1/PMUIO2

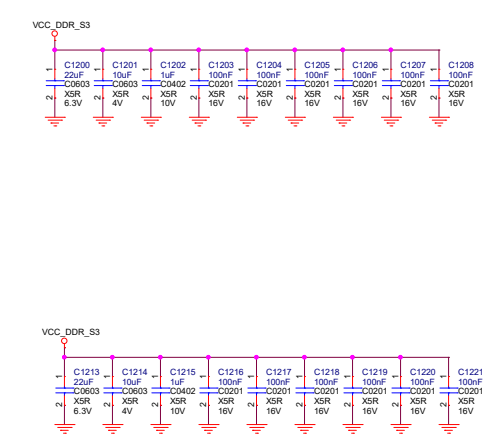


Title			
RK3399Pro_vmarc			
Size	Document Number	Rev	
A3	RK3399 Pro OSC/PMUIO1/PMUIO2	1.1	
Date:	Wednesday, November 13, 2019	Sheet	3 of 17

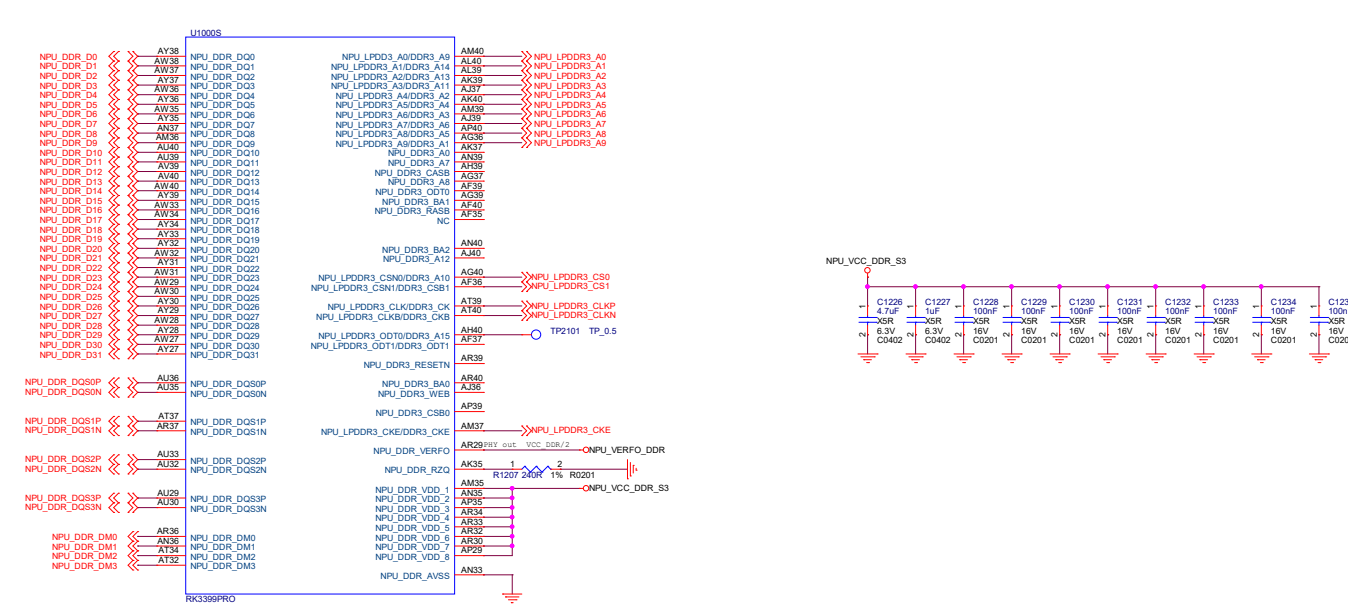
DDR Controller



DDR FILTER



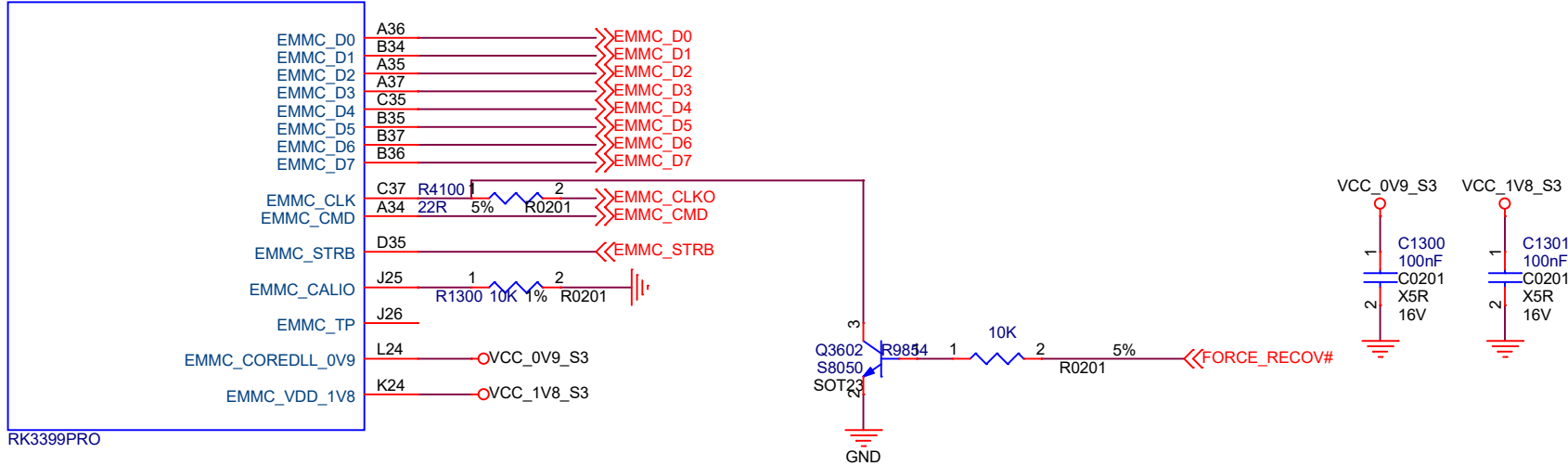
NPU DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A9
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN

EMMC Controller

U1000C



RK3399PRO

NPU EMMC Controller

U1000T

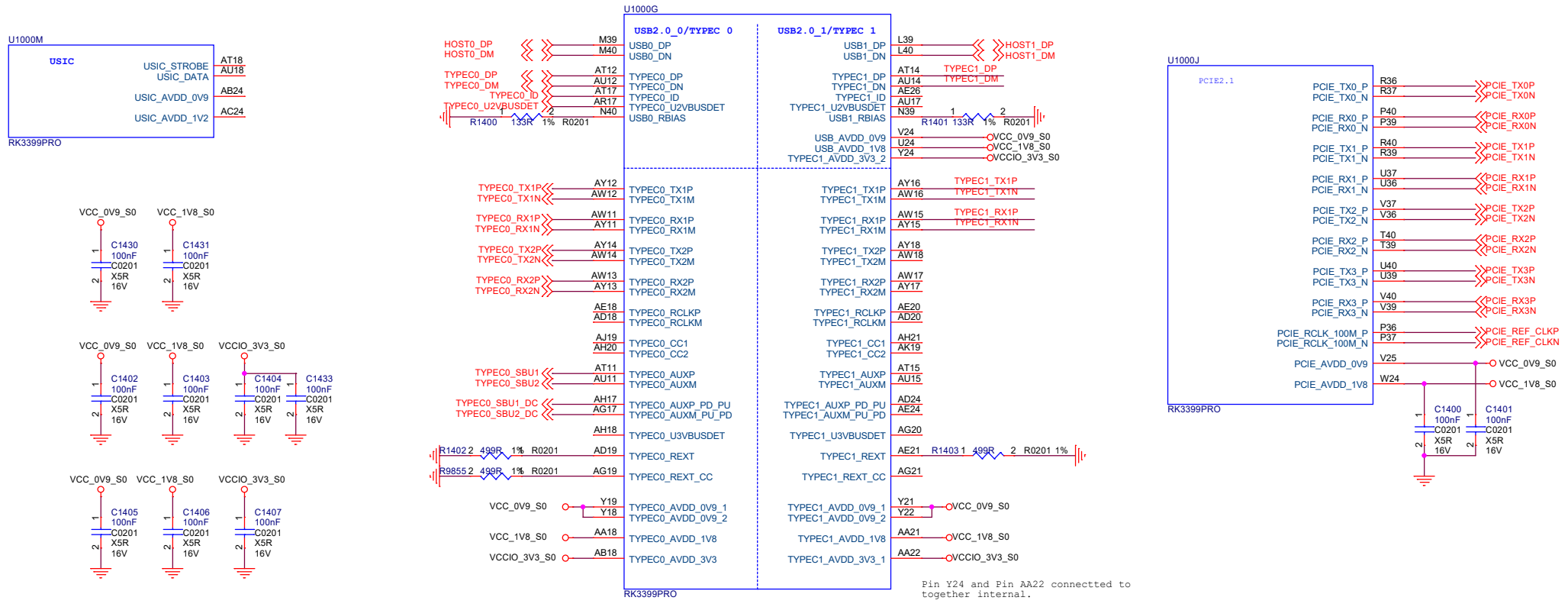


RK3399PRO

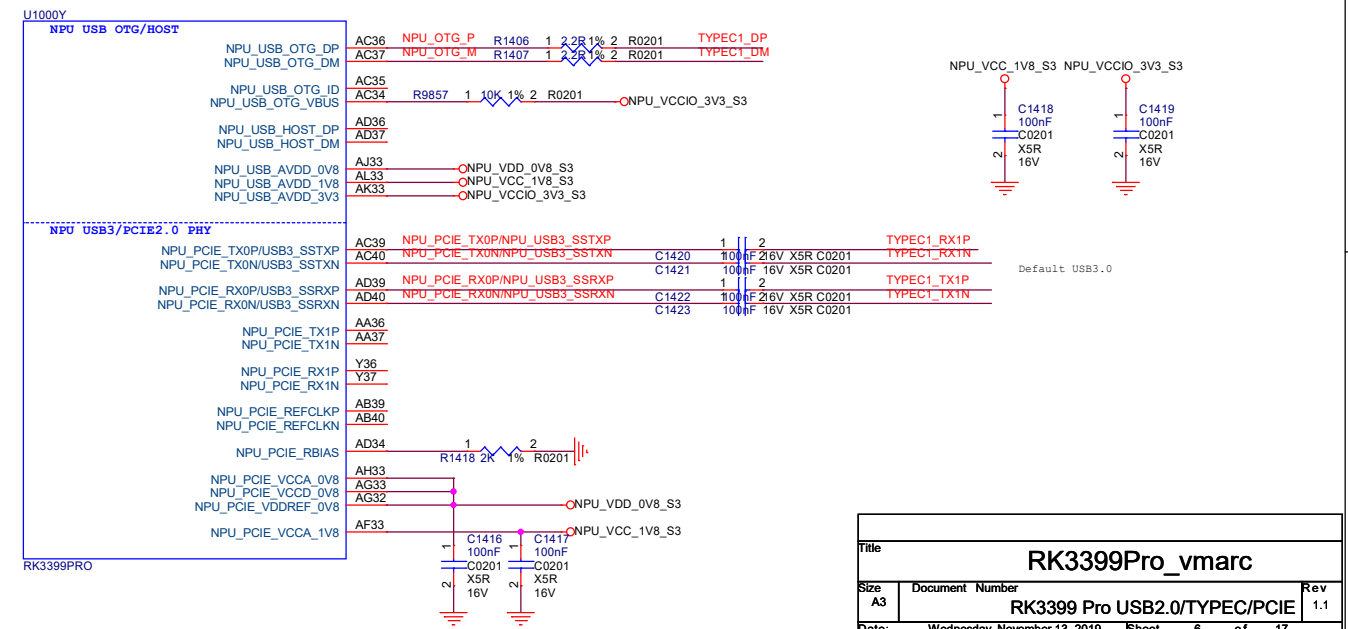
Title			RK3399Pro_vmarc		
Size	Document Number				Rev
A4	RK3399 Pro EMMC/SPI				1.1
Date:	Wednesday, November 13, 2019		Sheet	5	of 17

USB Controller

PCIe Controller



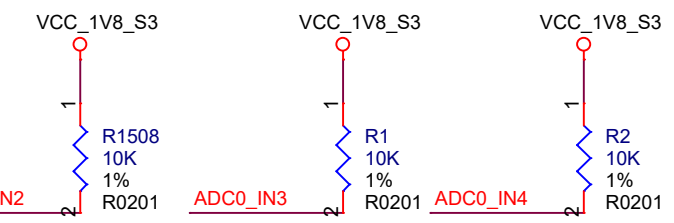
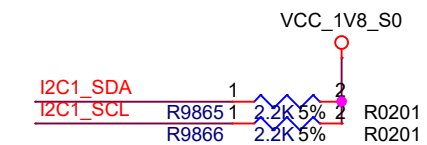
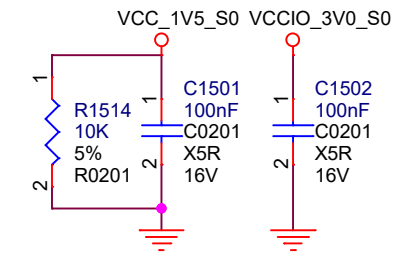
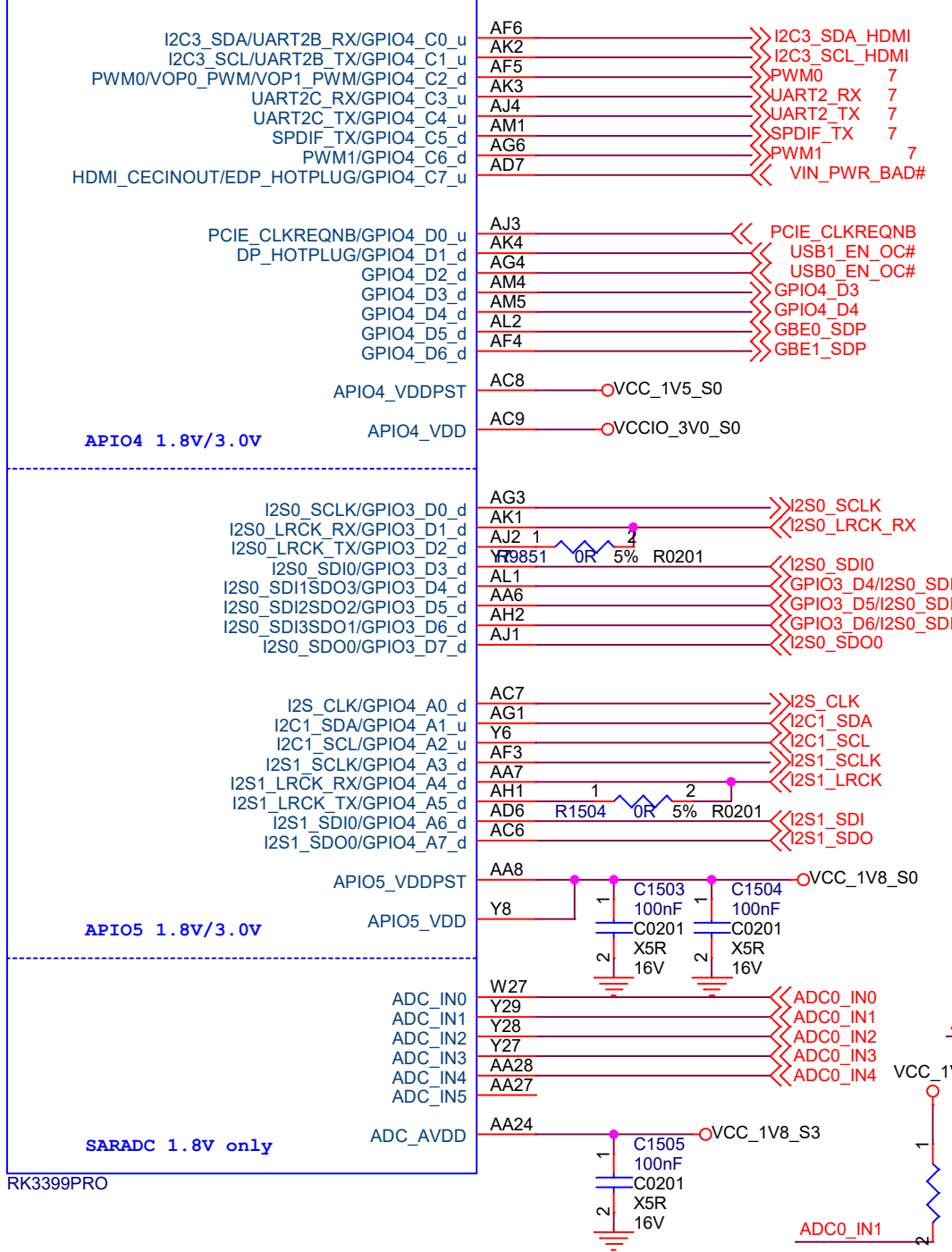
NPU PCIe/USB3.0 Controller



Title			
RK3399Pro_vmarc			
Size	Document Number	Rev	
A3	RK3399 Pro USB2.0/TYPEC/PCIE	1.1	
Date:	Wednesday, November 13, 2019	Sheet	6 of 17

GPIO/SARADC

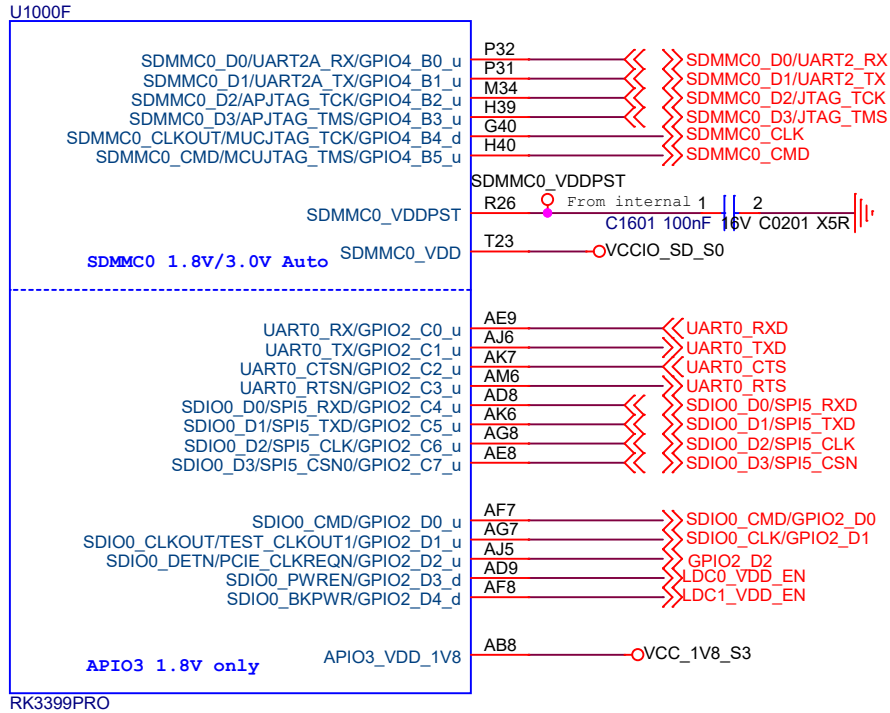
U1000N



RK3399PRO

Title		
RK3399Pro_vmarc		
Size	Document Number	Rev
A	RK3399 Pro SARADC/GPIO	1.1
Date:	Wednesday, November 13, 2019	Sheet 7 of 17

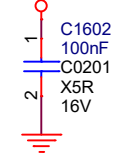
SDMMC0/SDIO0 Controller



VCCIO_SD_S0



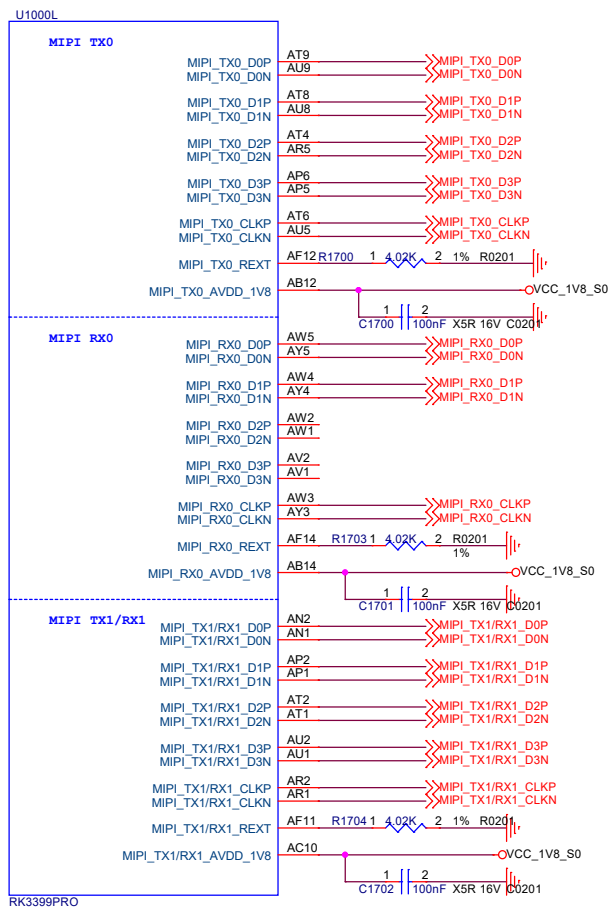
VCC_1V8_S3



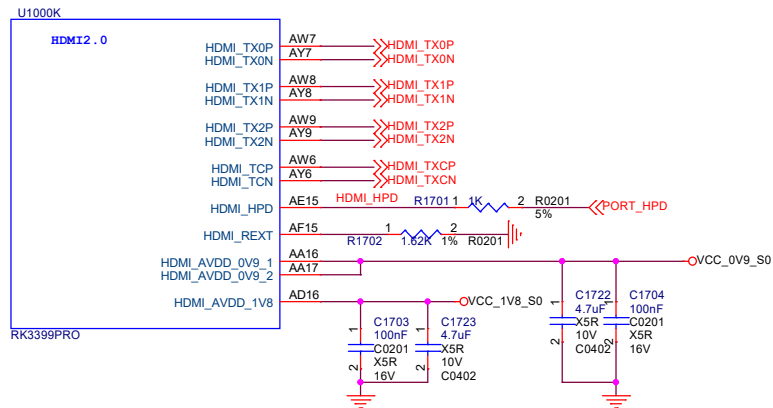
RK3399PRO

Title			RK3399Pro_vmarc		
Size	Document Number	Rev			
A4	RK3399 Pro SDMMC0/SDMMC1	1.1			
Date:	Wednesday, November 13, 2019	Sheet	8	of	17

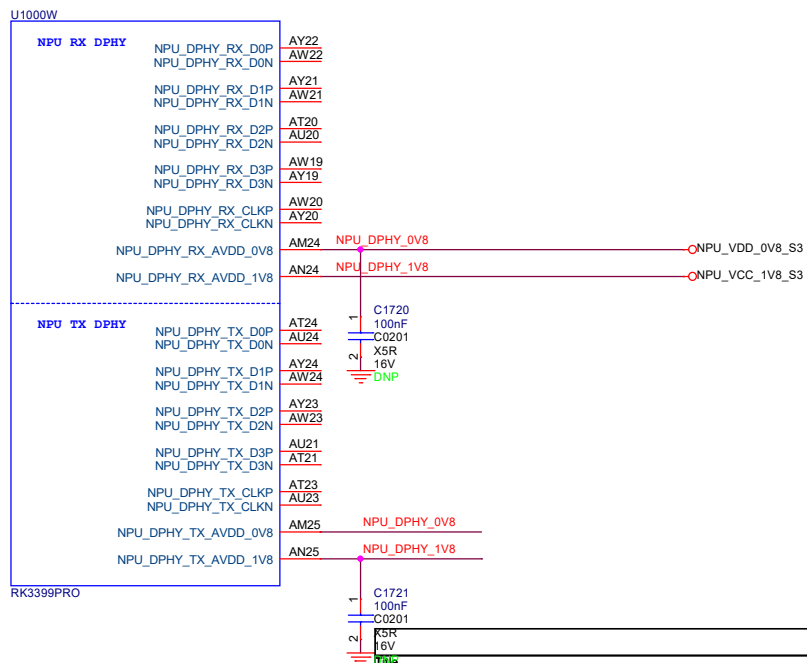
MIPI CSI/DSI Controller



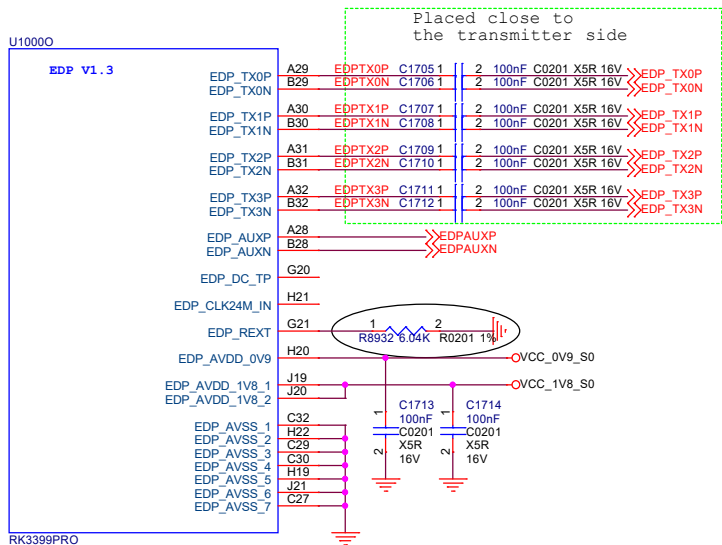
HDMI Controller



NPU MIPI DSI/CSI Controller



EDP Controller

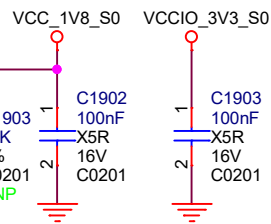


RK3399Pro_vmarc

Size	Document Number	Rev
A3	RK3399 Pro Display	1.1
Date:	Thursday, November 14, 2019	Sheet 9 of 17

MAC Controller

U1000I



APIO1 3.3V only

RK3399PRO

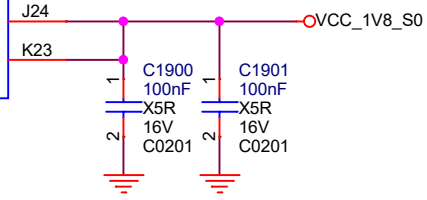
VOP/CIF Controller

U1000P

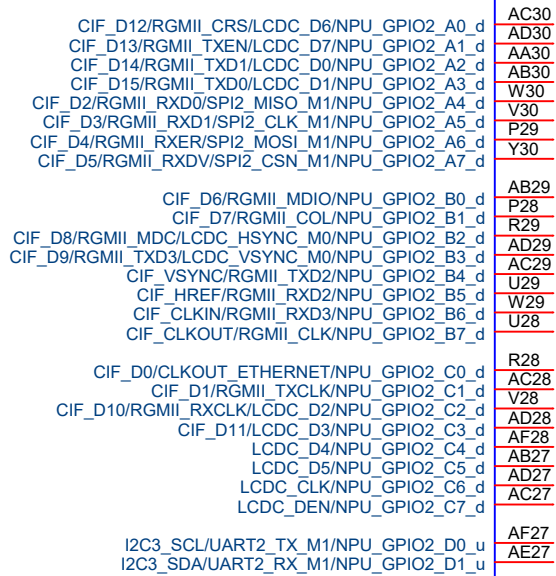


APIO2 1.8V/3.0V

RK3399PRO

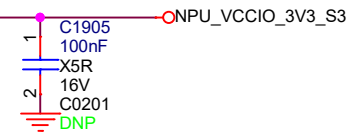


U1000X



NPU VCCIO2 1.8V/3.3V

NPU_VCCIO2

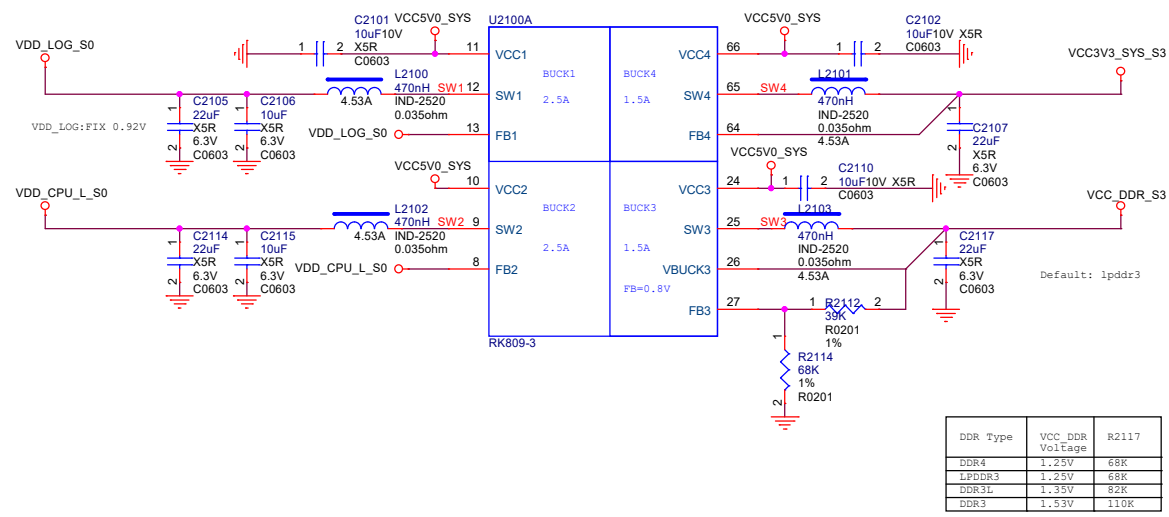


RK3399PRO

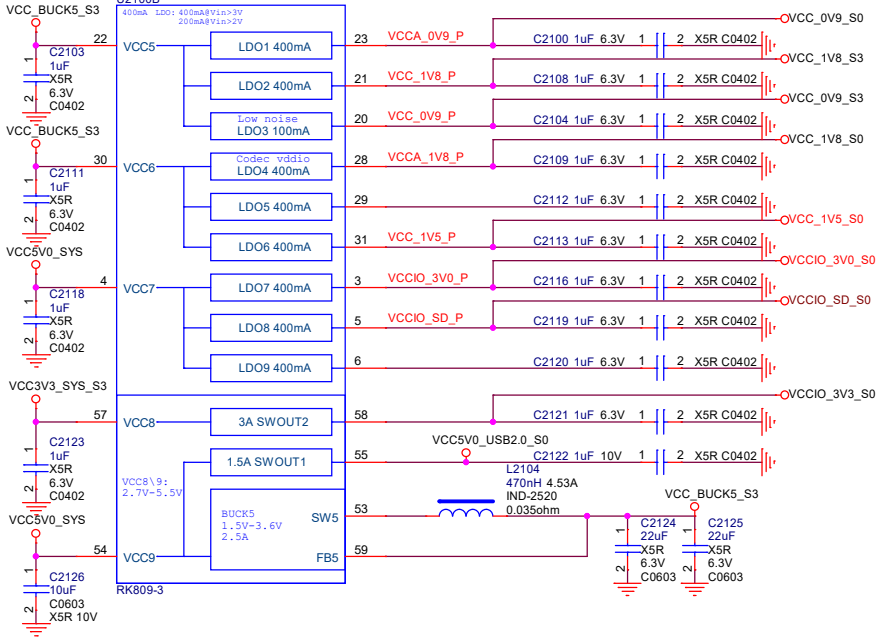
NPU CIF/RGMII/LCDC Controller

Title			RK3399Pro_vmarc		
Size	Document Number	Rev			
A4	RK3399 Pro RGMII/LCDC/CIF	1.1			
Date:	Thursday, November 14, 2019	Sheet	10	of	17

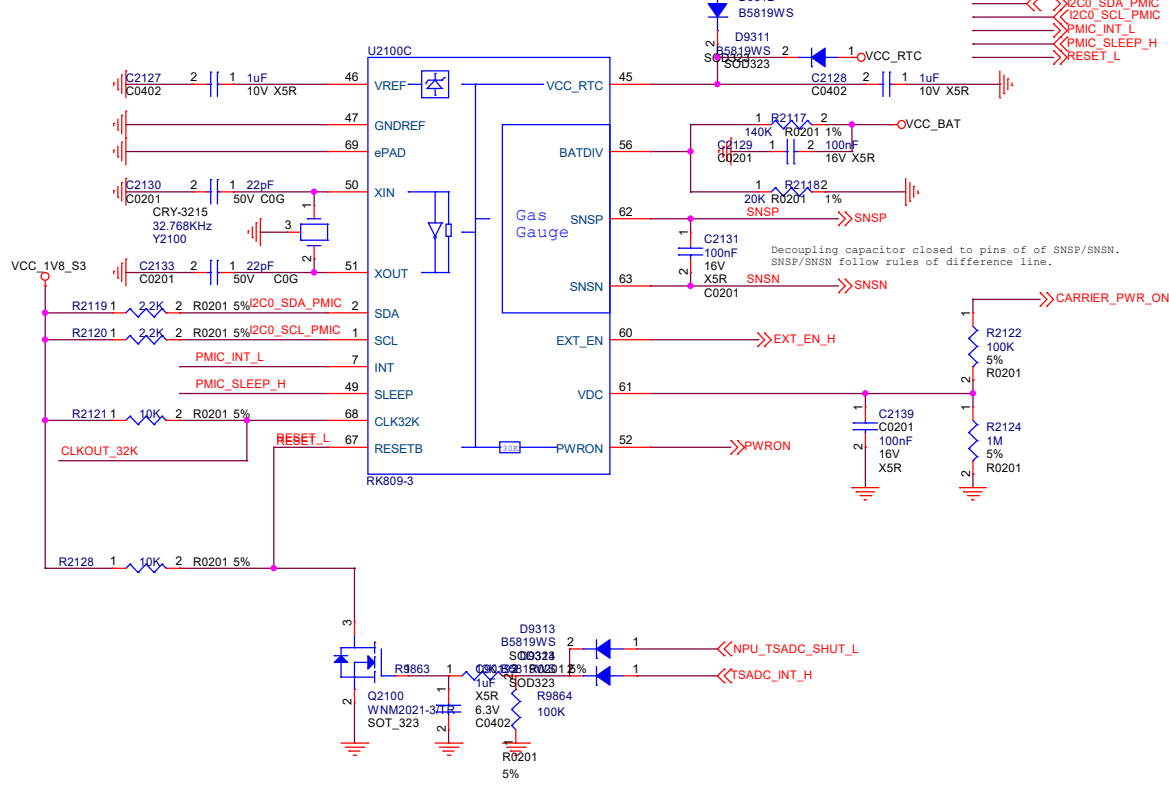
PMIC RK809-3 DCDC



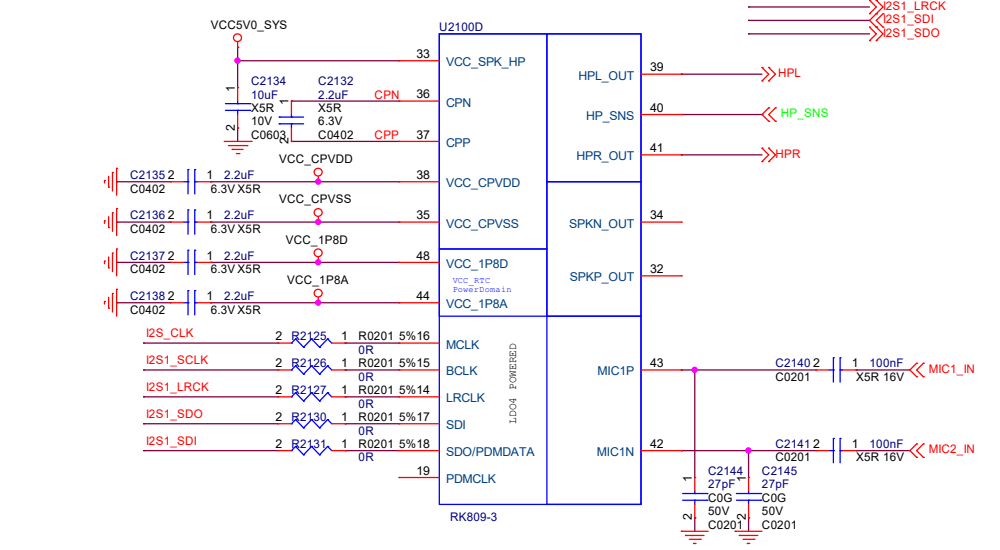
PMIC RK809-3 LDO



PMIC RK809-3 Management

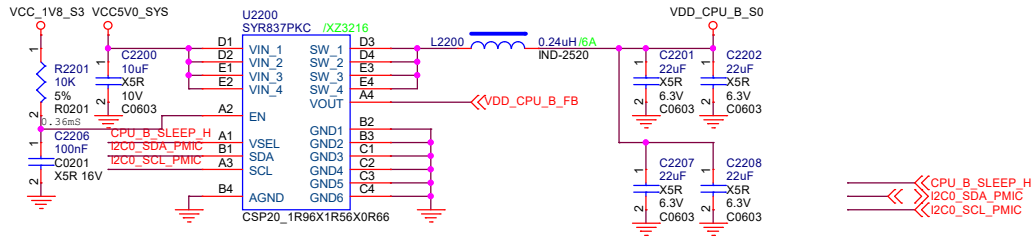


PMIC RK809-3 CODEC

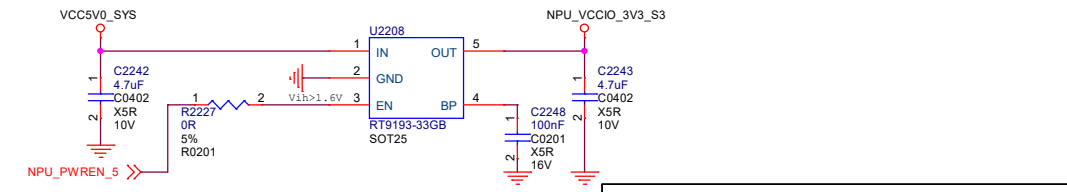
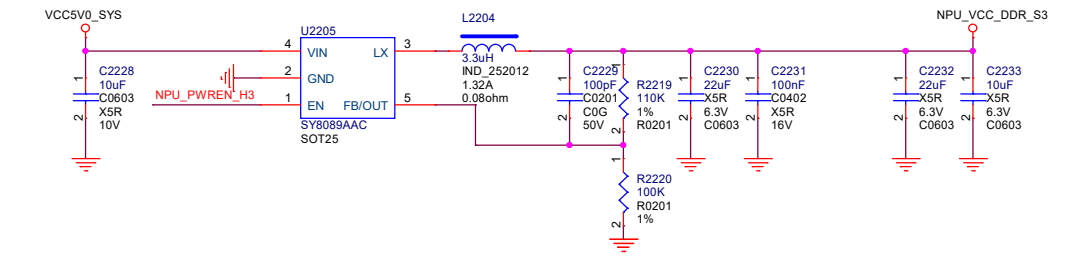
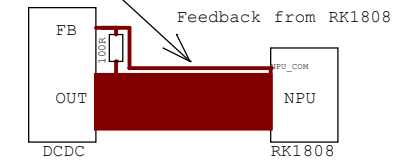
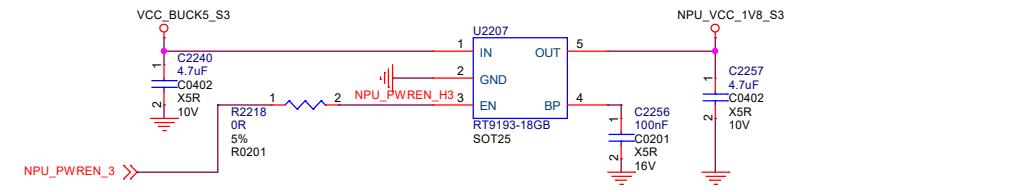
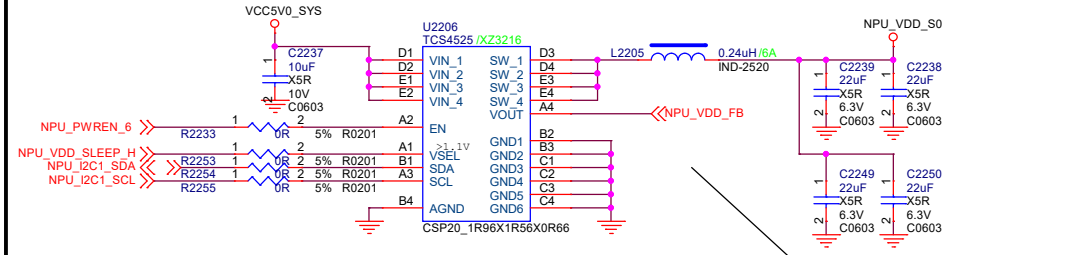
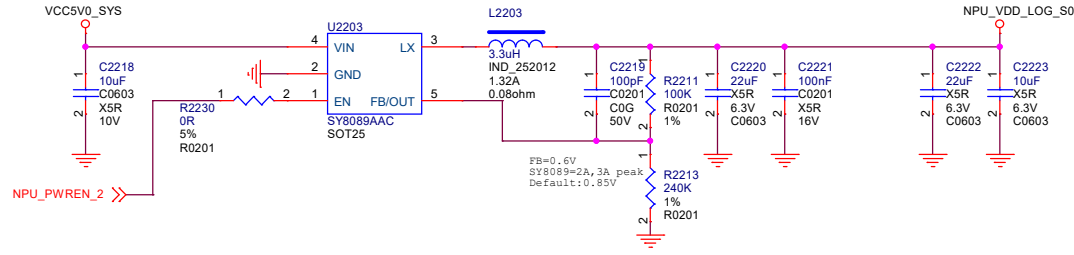
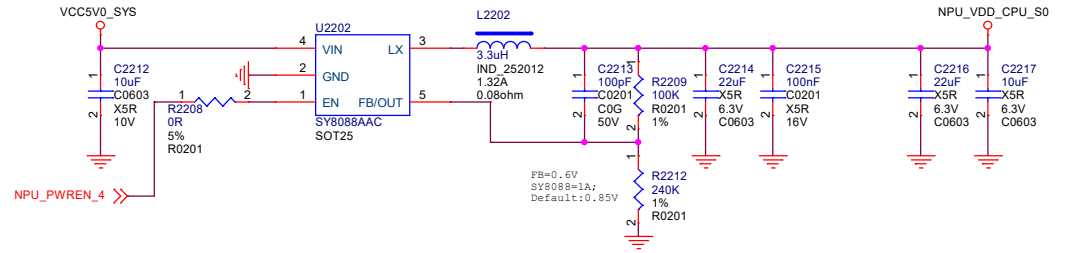
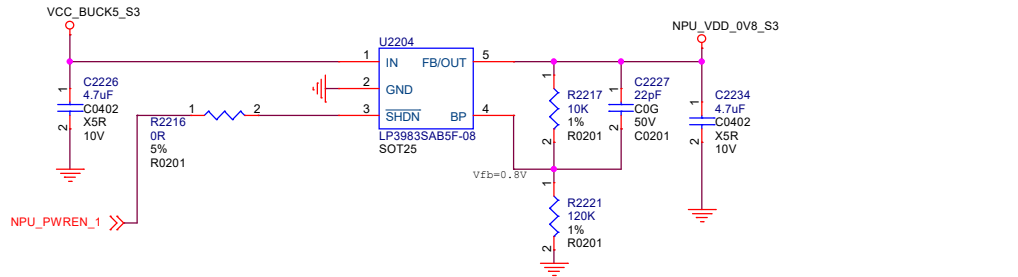
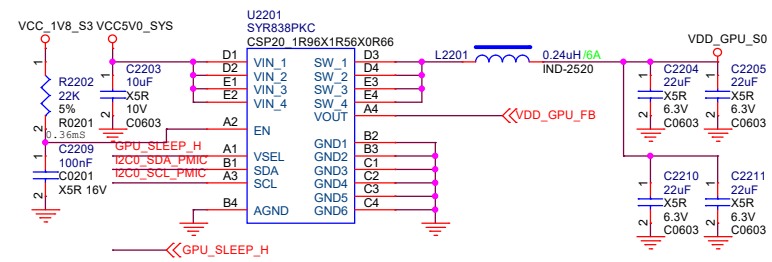


Title				RK3399Pro_vmarc	
Size	A3	Document Number	Power-PMIC RK809-3		
Date:	Thursday, November 14, 2019	Sheet	11	of	17
					Rev 1.1

VDD_CPU_B power



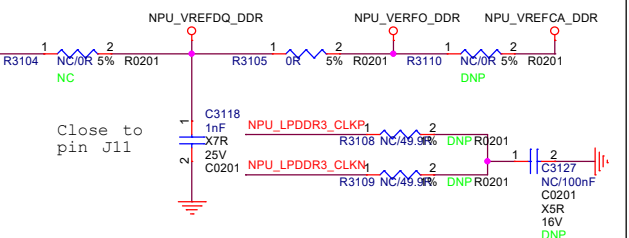
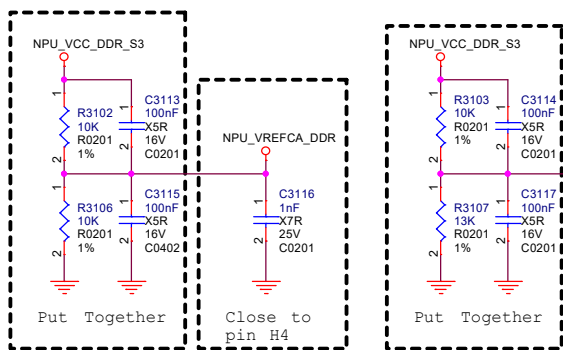
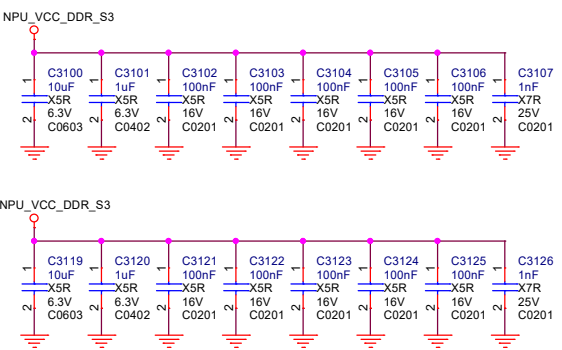
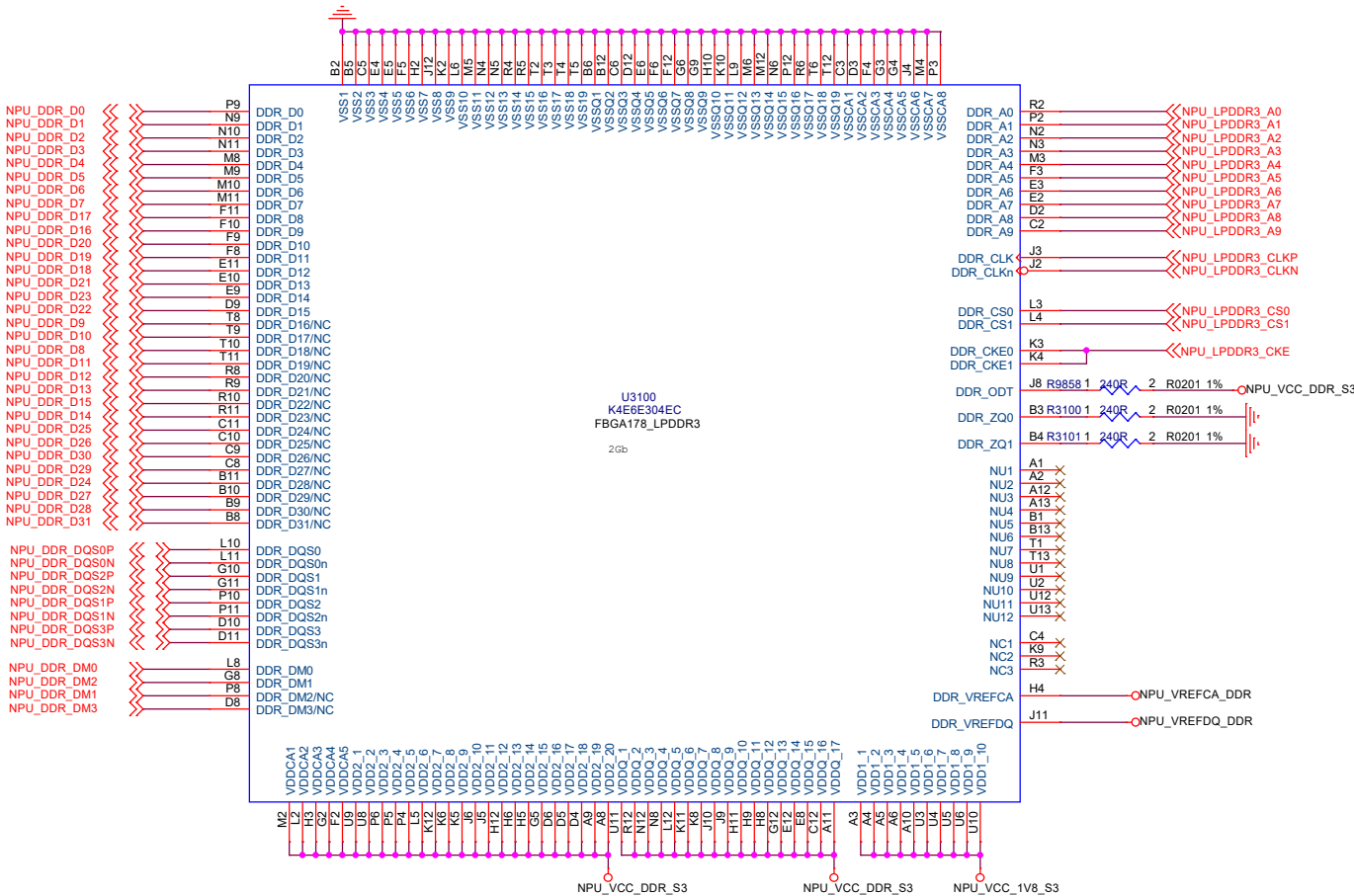
VDD_GPU power



NPU Part power

Title				RK3399Pro_ymarc	
Size	A3	Document Number	POWER-CPU/GPU/NPU		Rev
Date:	Thursday, November 14, 2019	Sheet	12	of	17

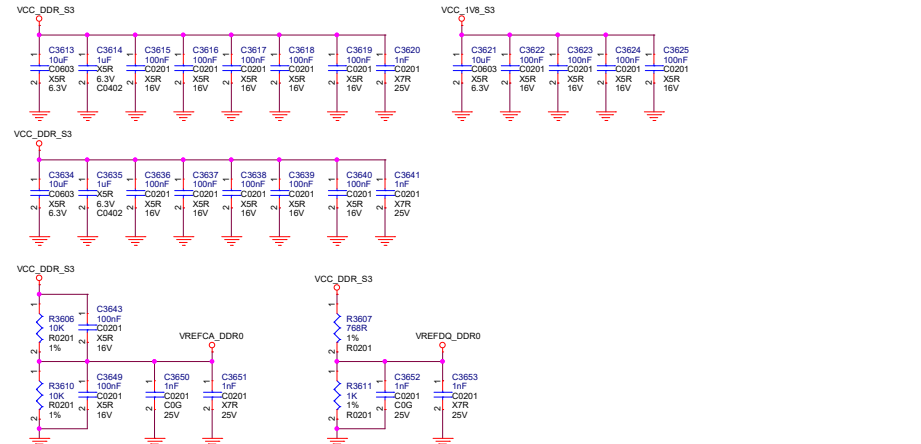
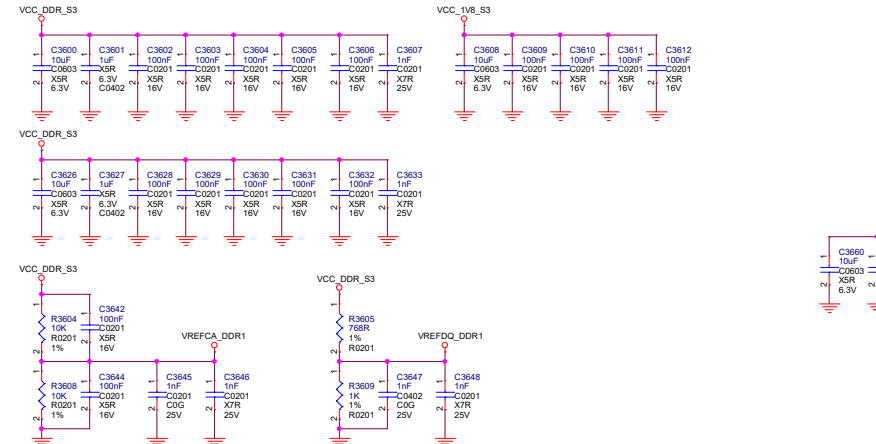
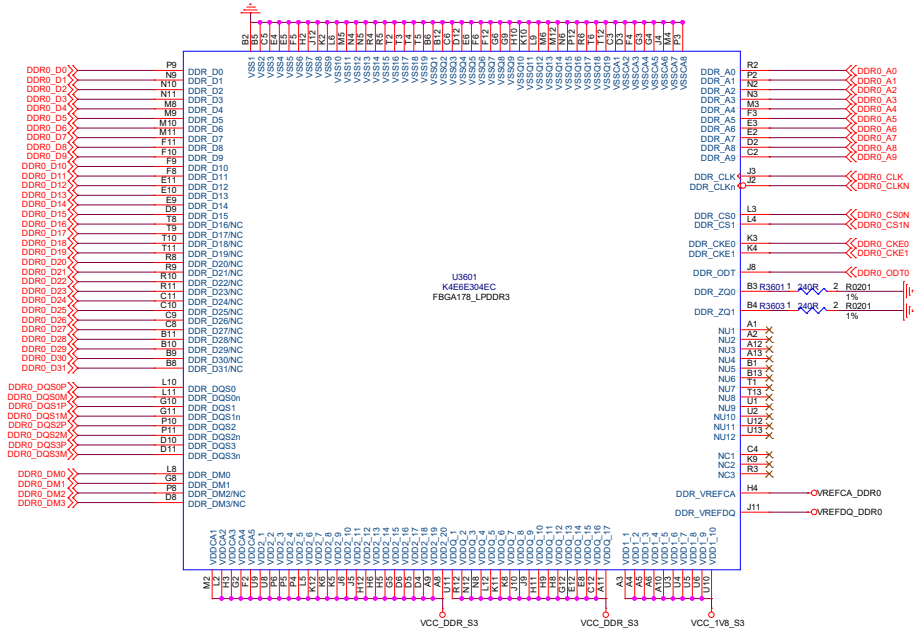
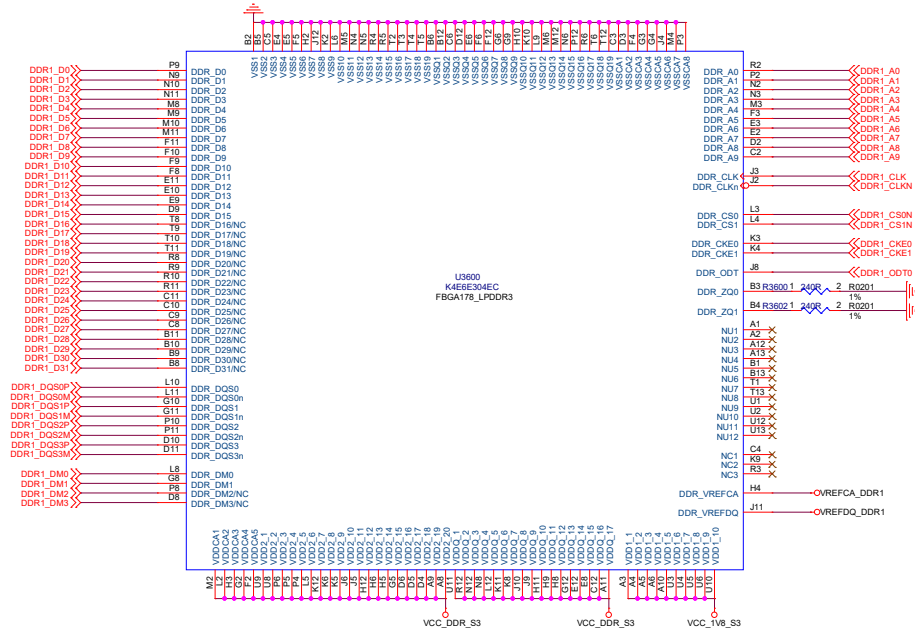
NPU LPDDR3 1x32bit



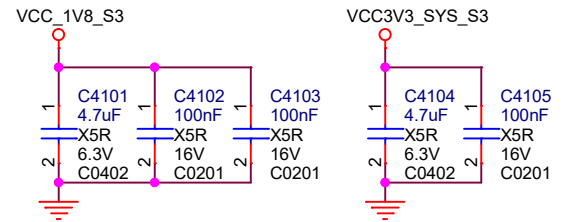
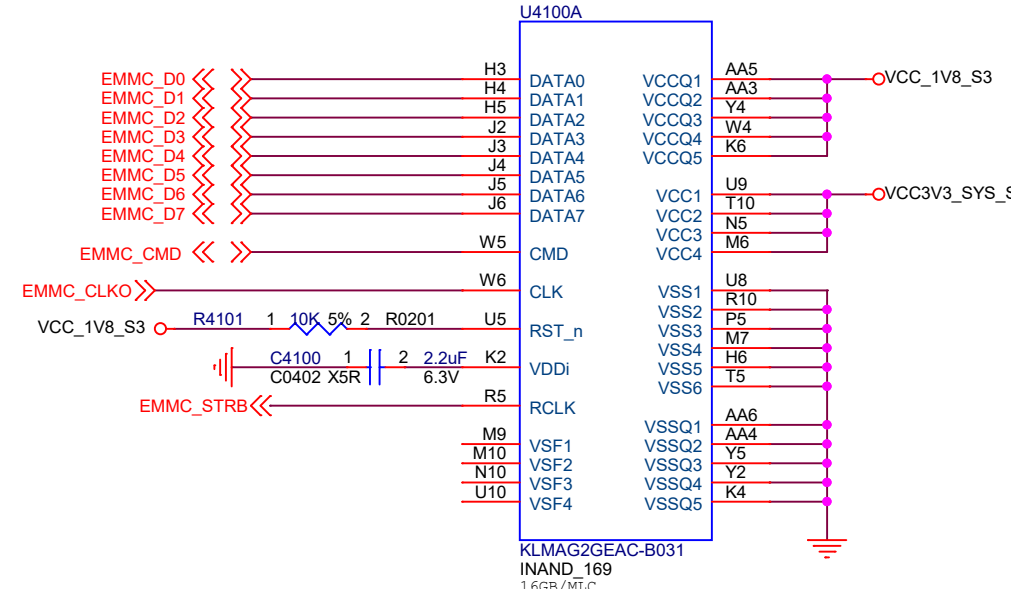
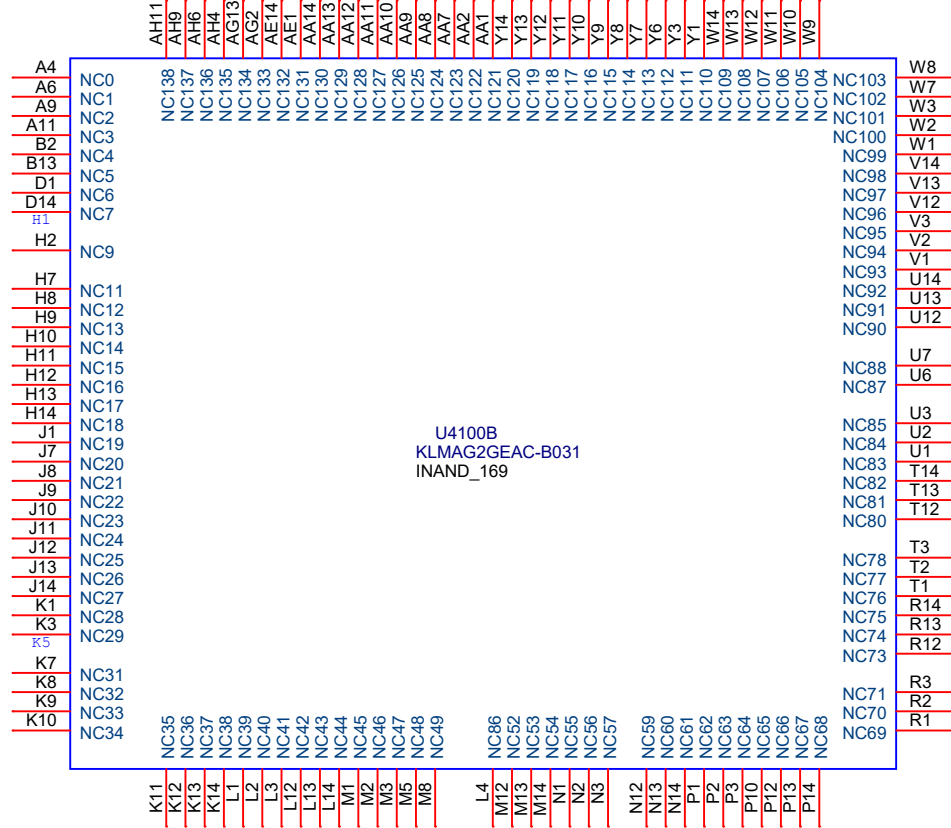
Note: All the power filter capacitors should be placed close to the power pins of LPDDR3

Note:
 $V_{ih} = V_{CC}$
 $V_{il} = V_{CC} \cdot R_{on} / (R_{on} + R_{odt})$
 $V_{REFDQ_DDR} = (V_{ih} + V_{il}) / 2$
 eg: $V_{CC} = 1.2V$, $R_{on} = 34\Omega$, $R_{odt} = 240\Omega$
 so, $V_{ih} = 1.2V$, $V_{il} = 0.149V$, $V_{REFDQ_DDR} = 0.674V$

Title			
RK3399Pro_vmarc			
Size	Document Number	Rev	
A3	NPU_RAM-LPDDR3 1x32bit	1.1	
Date:	Thursday, November 14, 2019	Sheet	13 of 17

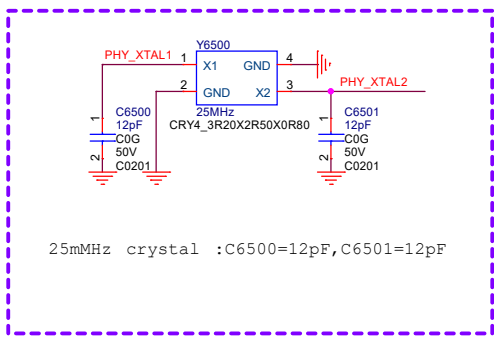


eMMC

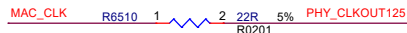


Title			RK3399Pro_vmarc		
Size	Document Number				Rev
A4	EMMC				1.1
Date:	Thursday, November 14, 2019	Sheet	15	of	17

- >>>PHY_TXD0
- >>>PHY_TXD1
- >>>PHY_TXD2
- >>>PHY_TXD3
- >>>PHY_TXEN
- >>>PHY_TXCLK
- <<<MAC_RXD0
- <<<MAC_RXD1
- <<<MAC_RXD2
- <<<MAC_RXD3
- <<<MAC_RXDV
- <<<MAC_RXCLK
- <<<MAC_CLK
- >>>MAC_MDIO
- >>>MAC_MDC
- >>>PHY_RST
- >>>PHY_INT
- >>>PHY_PMEB

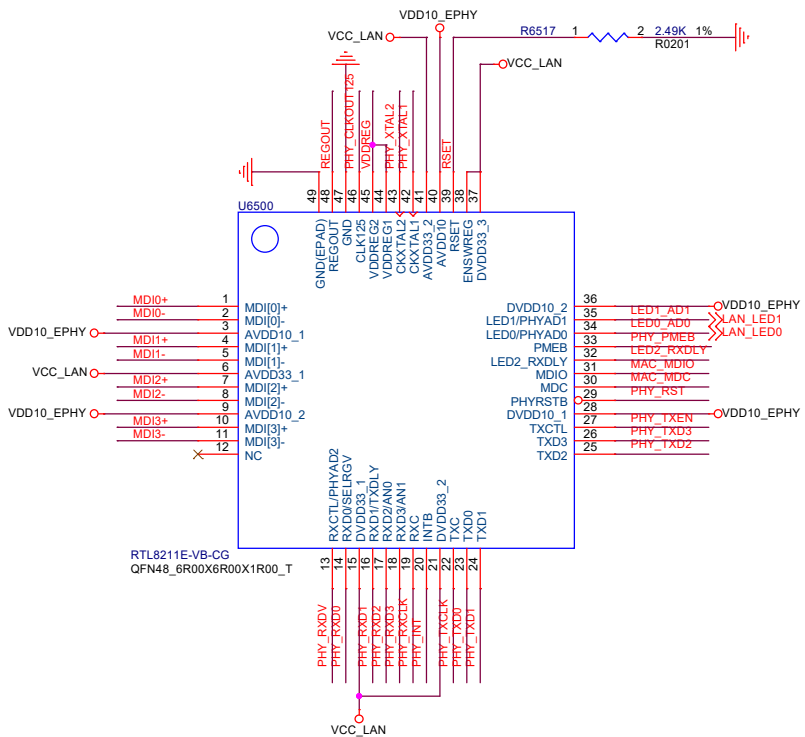


25mMHz crystal : C6500=12pF, C6501=12pF

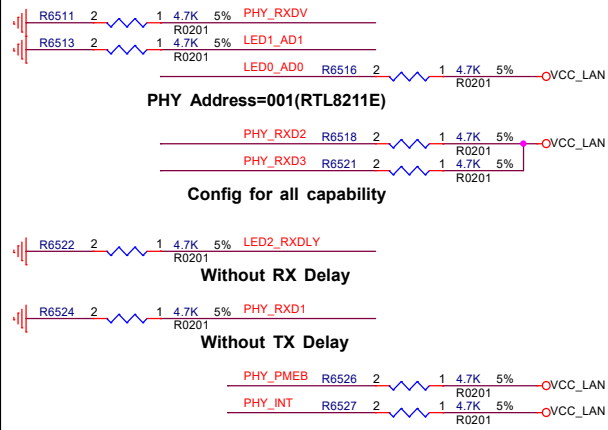


MAC <----- PHY

- >>>MDI3-
- >>>MDI3+
- >>>MDI2-
- >>>MDI2+
- >>>MDI1-
- >>>MDI1+
- >>>MDI0-
- >>>MDI0+



Close to PHY



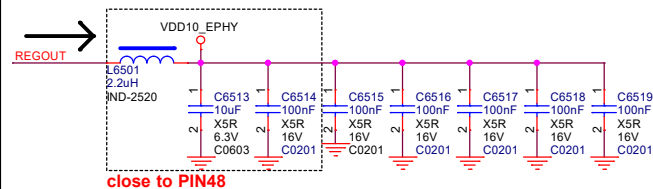
PHY Address=001(RTL8211E)

Config for all capability

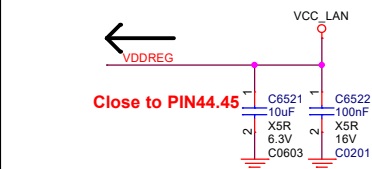
Without RX Delay

Without TX Delay

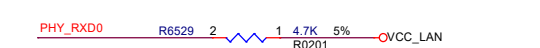
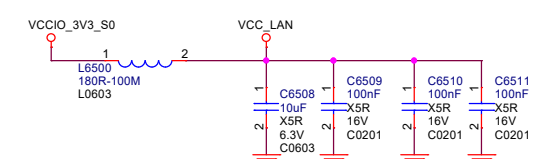
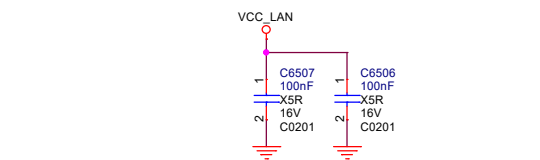
Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.



close to PIN48



Close to PIN44.45

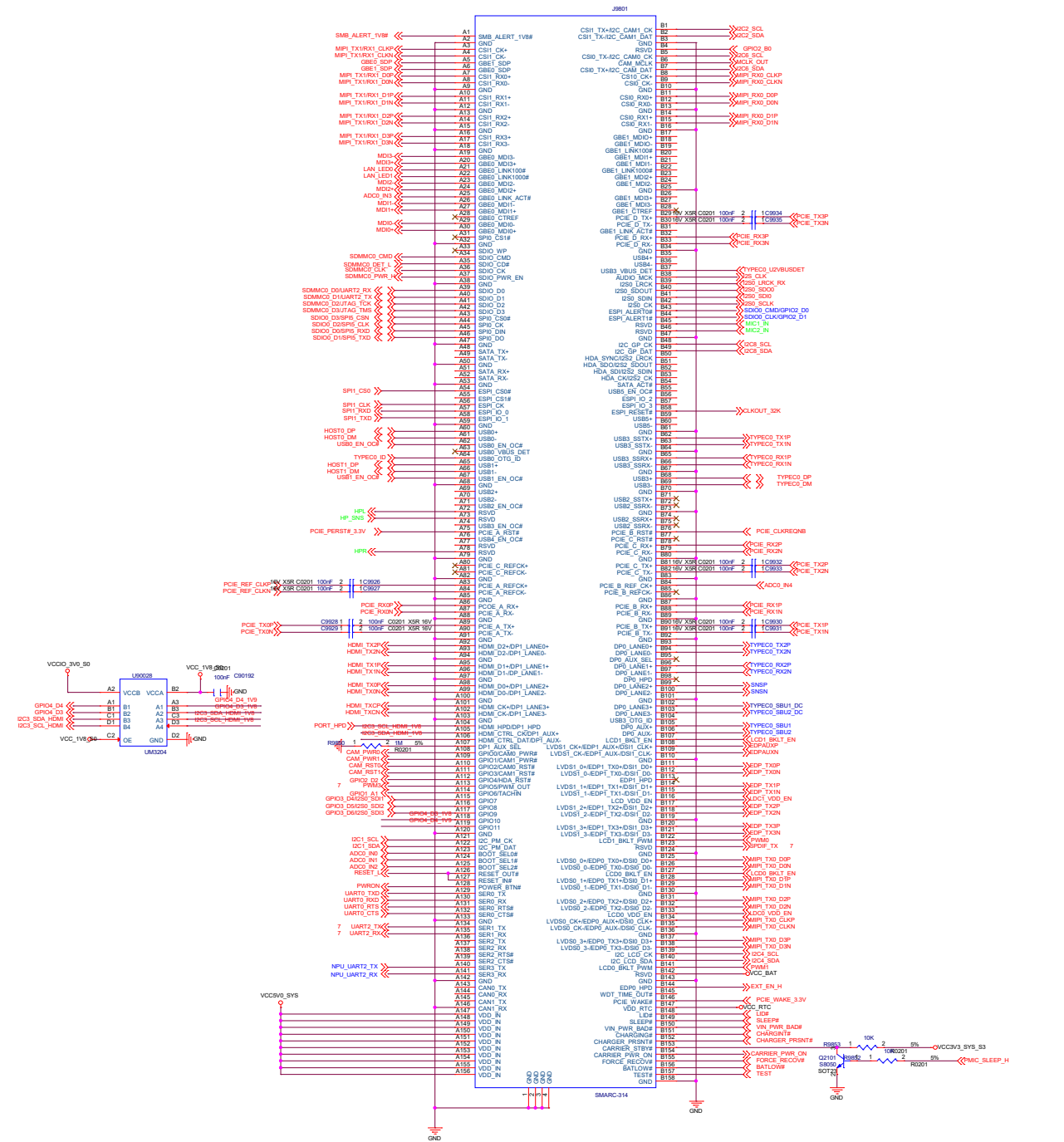


Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)



RGMII 1000M

Title			RK3399Pro_vmarc
Size	Document Number	RGMII-10/100/1000M	
A3			Rev 1.1
Date:	Thursday, November 14, 2019	Sheet	16 of 17



Doc No	RK3399Pro_vmarc		Rev
Doc Name	CONNECT		1.1
Doc Date	Thursday, November 14, 2019	Sheet	17 of 17