Radxa rCore-RK3308 Datasheet

A low-cost SoM for IoT and Audio applications

Revision 1.1

2025-04-28

Radxa Computer

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1 Revision Control Table

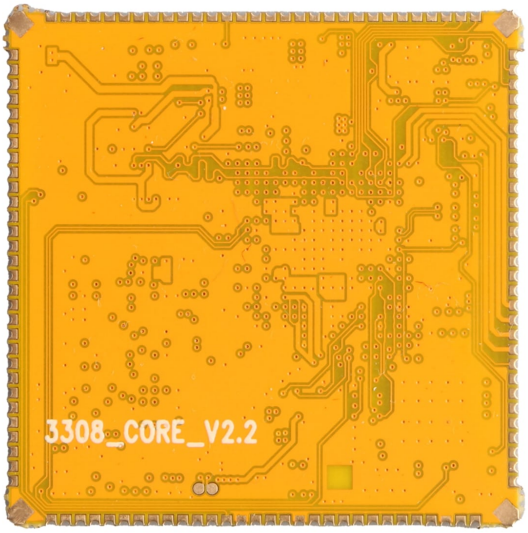
Version	Date	Changes from previous version
1.0	2024/11/29	First Version
1.1	2025/04/25	Change PDF fonts to avoid CJK characters

2 Introduction

Note:
The Radxa ROCK Pi S Core has now been incorporated into the Radxa rCore Series. The latest product name is Radxa rCore-RK3308.

2.1 Overview

Radxa rCore-RK3308 is a Rockchip RK3308B based SoM(System on Module) by Radxa. It equips a 64bits quad core processor, Ethernet, wireless connectivity and voice activity detection(VAD) at the size of 35x35mm, make it perfect for IoT and voice applications. rCore-RK3308 comes in two ram sizes 256MB or 512MB DDR3, and uses eMMC or NAND Flash for OS and storage. Optionally, rCore-RK3308 can provide on board storage version with 128MB / 256MB / 512MB NAND flash or 8GB / 16GB eMMC.



Note:
The actual board layout or components location may change during the time but the main connectors type and location will remain the same.

2.2 Hardware

This Radxa rCore-RK3308 is based on the Rockchip RK3308B SoC, featuring a quad-core Cortex®-A35 processor with a clock speed of 1.0GHz, making it suitable for a wide range of voice embedded applications. For memory, it offers two DDR3 RAM options: 256MB and 512MB. In terms of storage, it supports various choices, including 128MB, 256MB, or 512MB NAND Flash, as well as 8GB and 16GB eMMC storage modules to meet different needs.

For wireless connectivity, the product supports 802.11 b/g/n WiFi(WiFi 4) and BT 4.0, with an external antenna connector to ensure stable network and Bluetooth connections. It also features a 100Mbps Ethernet interface, suitable for basic network connectivity requirements.

The hardware offers a rich set of interfaces with extensive expansion capabilities, including GPIO, SDIO 3.0, USB2.0 OTG, USB2.0 HOST, up to 3 SPI interfaces, up to 4 I2C interfaces, and up to 5 UART interfaces, enabling easy communication and data exchange with external devices.

2.3 Feature Summary

Table 2: *Radxa rCore-RK3308 Feature Summary*

Features	Description
Form factor:	Stamp Footprint at 35 mm × 35 mm
Processors:	Rockchip RK3308B SoC, Quad Cortex®-A35 @ 1.0GHz
Memory:	256MB or 512MB DDR3 RAM (depending on SKU)
Storage:	1x Onboard 128MB / 256MB / 512MB NAND Flash or 8GB / 16GB eMMC (depending on SKU) 1x SDMMC
Wireless:	IEEE 802.11 b/g/n WiFi and BT 4.0 with Antenna Connector
USB:	USB 2.0 OTG USB 2.0 HOST
Ethernet:	Support 100Mbps Ethernet MAC

Connectivity:	6x SARADC 1x UART 1x LCD Controller 1x SPI 2x I2C 1x PDM 1x S/PDIF 3x I2S 1x Line Out 1x Headphone Out 5x Microphone Input

Note:
Radxa rCore-RK3308 has obtained certification as a component for use in Information Technology Equipment in certain countries. However, it is the responsibility of the system integrator to conduct testing and acquire any additional country-specific regulatory approvals, including all necessary system-wide certifications.

2.4 Block Diagram

Figure below is a block diagram of the major functional areas of Radxa rCore-RK3308.

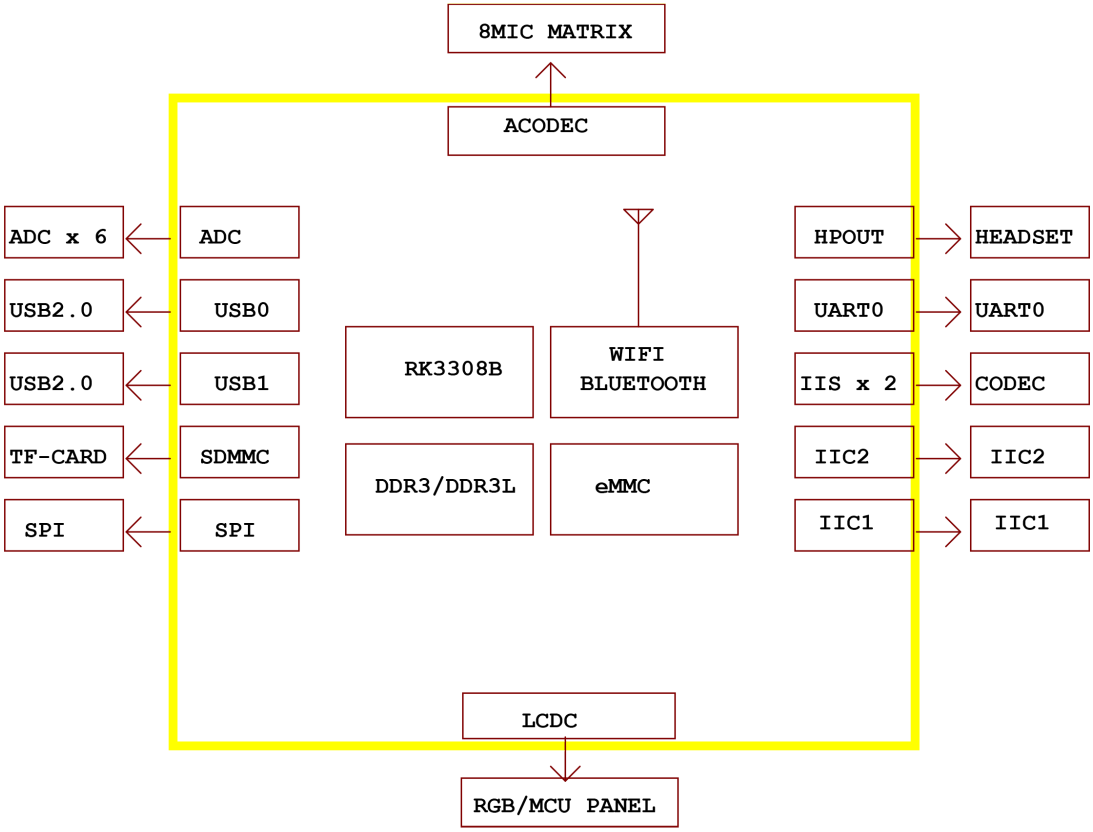


Figure 1: *Radxa rCore-RK3308 Block Diagram*

2.5 Compute Module Layout

The following figure displays the board layout of the Radxa rCore-RK3308. Each connector and major component is labeled with a number or letter for easy identification. A description of each labeled item is provided in the table below the figure.

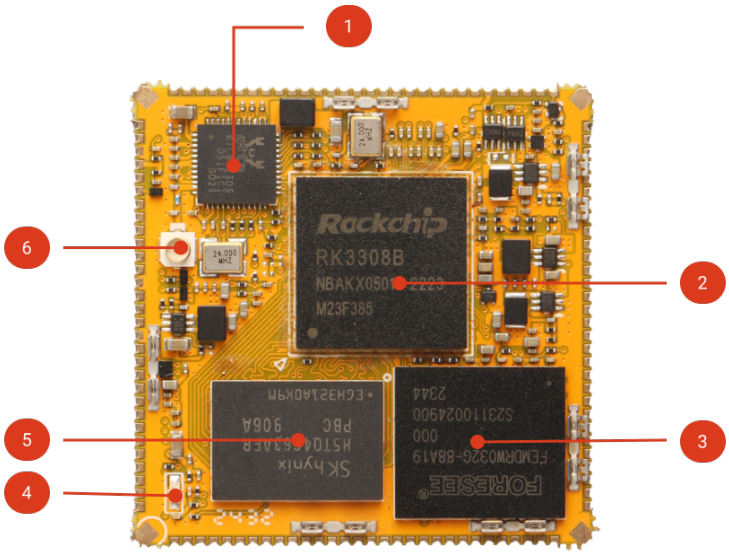


Figure 2: *Radxa rCore-RK3308*

Figure: Radxa rCore-RK3308 Top View

Table 3: *Radxa rCore-RK3308 Top View*

No.	Description	No.	Description
1	RTL8723DS-CG	2	Rockchip RK3308B
3	eMMC	4	LED Light
5	DDR3 RAM	6	Antenna Connector

3 Interface

3.1 Power Supply

3.1.1 Power Supply Pins

Radxa rCore-RK3308 supports 5V DC input.

Table 4: *Power Supply Pins*

Signal	Pin number	Power Input / Output	Typical Voltage	Voltage Range	Typical Current
VCC5V0_SYS	pin111, 112	Input	5V	3.8V to 5.2V	2A
VCC_IO	pin66, 116	Output	3.3V	3.3V	200mA

3.2 Analog Audio Interface

Radxa rCore-RK3308 has 5 Microphone input interfaces, one Line Out and one Headphone Out.

3.2.1 Microphone Input

The Radxa rCore-RK3308 is equipped with two MICBIAS outputs, and each MICBIAS can supply a current of 3mA. In application scenarios, it is recommended to evenly distribute these two MICBIAS power supplies for use by microphones. For example, if 5 analog microphones are used in the product, one MICBIAS can be arranged to provide power support for 3 microphones, and the other MICBIAS can be used to power the remaining 2 microphones.

3.2.2 Line Out

The Radxa rCore-RK3308 is equipped with a set of DAC Line Out output pins. Its core purpose is to connect to an external power amplifier and serve as the input interface for the signal source of the external power amplifier.

3.2.3 Headphone Out

The Radxa rCore-RK3308 is configured with a set of HP Out, which can be connected to headphones and has the function of insertion detection. When the headphones are inserted, the PHONE_DET signal will change from a low level to a high level, with the value of the high level being 1.8V. Meanwhile, the value of the headphone detection register will be set to 0x01 and reported to the interrupt system so that the interrupt system can respond to the headphone insertion operation, ensuring that the system can promptly be aware of the change in the connection status of the headphones and providing accurate basis and adaptation for subsequent related operations such as audio output.

3.3 Analog Microphone Reference Circuit

The reference circuit of the analog silicon microphone is shown in the figure below.

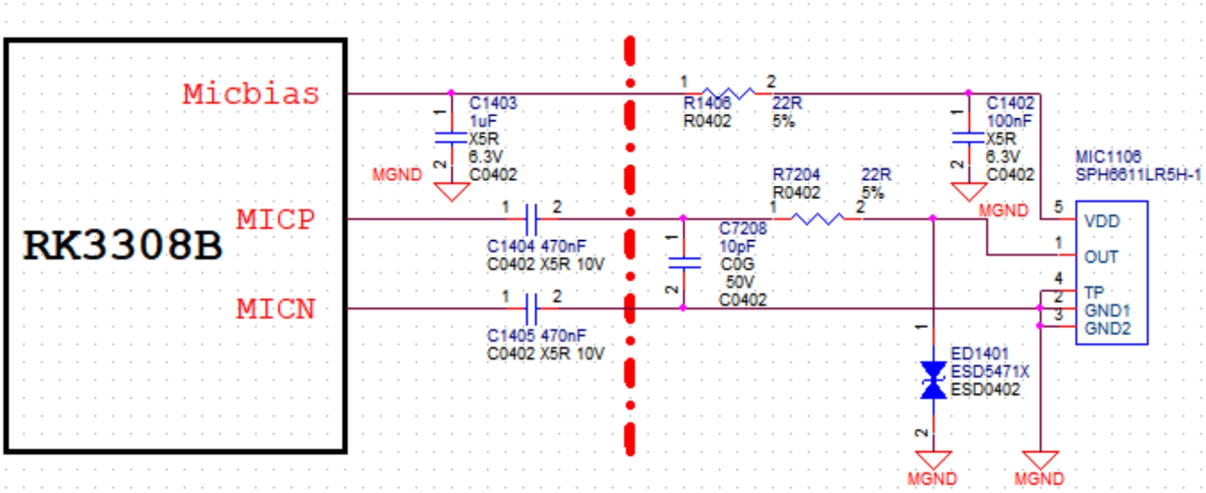


Figure 3: *Analog Silicon Microphone*

The reference circuit of the electret microphone is shown in the figure.

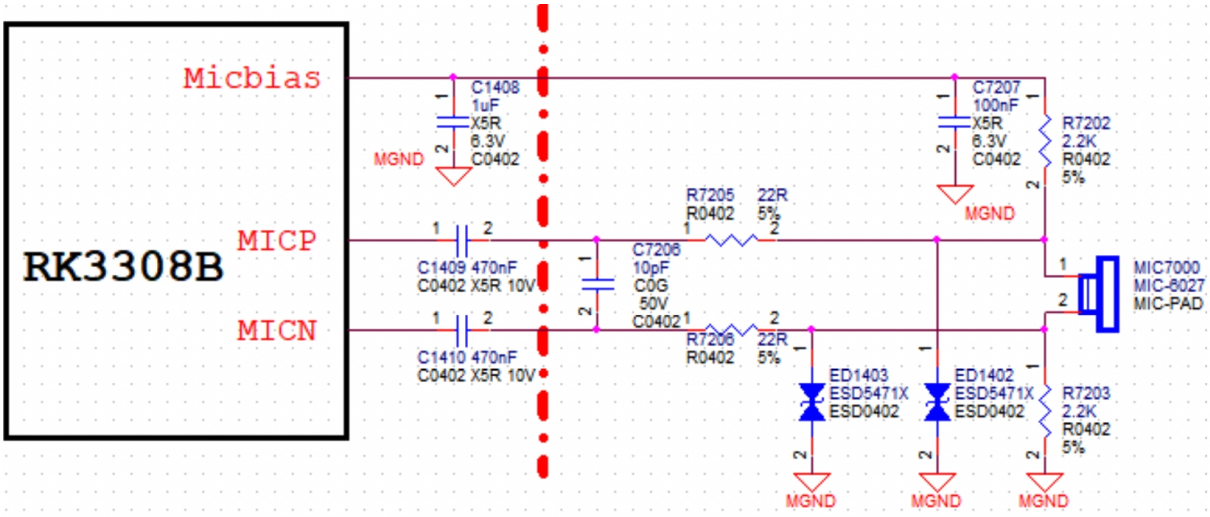


Figure 4: *Analog Electret Microphone*

Note:
The circuit on the left side of the dashed line needs to be placed close to the ADC, while the part on the right side of the dashed line must be placed close to the MIC. Meanwhile, since the microphone must have an opening design in the form of voice products, in order to improve the electrostatic discharge (ESD) resistance of the system, ESD protection devices are added to the microphone circuit and placed close to the microphone.

3.4 Digital Audio Interface

3.4.1 I2S

The Radxa rCore-RK3308 is equipped with two sets of standardized and mutually independent I2S interfaces, specifically including I2S0_8CH and I2S1_8CH. Both of these interfaces are capable of supporting either the Master mode or the Slave mode, demonstrating excellent flexibility. The sampling rate of its I2S interfaces can reach an impressive upper limit of 192 kHz, and the resolution can be freely selected between 16 bits and 32 bits, which is sufficient to meet various high-precision audio processing requirements. Particularly importantly, these two sets of I2S interfaces are independent of each other and can be individually enabled without interfering with each other. This provides great convenience and extensibility for the construction of complex audio systems, allowing audio processing tasks to be accurately allocated according to different application scenarios and requirements, thereby realizing efficient and stable audio transmission and processing functions.

The I2S0_8CH interface is equipped with four SDI0 and four SDO0 interfaces. Under the default state, the input channel `SDIx` corresponds to `SCLK_RX` and `LRCK_RX` respectively, while the output channel `SDOx` corresponds to `SCLK_TX` and `LRCK_TX`. In the case where `SDOx` and `SDIx` only need to refer to one set of bit/frame clocks, `SCLKTX` and `LRCKTX` will be preferentially used as their common clocks.

Table 5: *I2S0_8CH Interface Design*

Signal	Pull-Up/Down	Connection	Description
I2S0_8CH_MCLK	Pull-Down	Series 22ohm Resistor	System clock output
I2S0_8CH_SCLK_TX	Pull-Down	Series 22ohm Resistor	Bit clock output (TX, associated with SDOx)
I2S0_8CH_SCLK_RX	Pull-Down	Series 22ohm Resistor	Master: Bit clock output (RX, associated with SDIx) ;Slave: Bit clock input
I2S0_8CH_LRCK_TX	Pull-Down	Series 22ohm Resistor	Frame clock output, used for channel selection (TX, associated with SDOx).
I2S0_8CH_LRCK_RX	Pull-Down	Series 22ohm Resistor	Frame clock, Master: Frame clock output (RX, associated with SDIx) ;Slave: Frame clock input
I2S0_8CH_SDIx	Pull-Down	Series 22ohm Resistor	Data input channel x

Signal	Pull-Up/Down	Connection	Description
I2S0_8CH_SDOx	Pull-Down	Series 22ohm Resistor	Data output channel x

The I2S1_8CH interface is equipped with one SDI0, one SDO0 and three SDIx/SDOx interfaces. Based on this, the SDIx and SDOx interfaces can be flexibly configured. It can simultaneously support the mode of 8-channel input combined with 2-channel output, or the combination of 8-channel output and 2-channel input. To meet the requirements of different sampling rates in the processes of playback and recording, two sets of bit clocks and frame clocks have been correspondingly set up, namely (SCLK_TX/LRCK_TX, SCLK_RX/LRCK_RX).

Under the default situation, the input channel SDIx corresponds to SCLK_RX and LRCK_RX respectively, while the output channel SDOx corresponds to SCLK_TX and LRCK_TX. When SDOx and SDIx only need to refer to one set of bit/frame clocks, SCLKTX and LRCKTX will be preferentially regarded as the clocks they use in common.

Table 6: *I2S1_8CH Interface Design*

Signal	Pull-Up/Down	Connection	Description
I2S1_8CH_MCLK_M0/M1	Pull-Down	Series 22ohm Resistor	System clock output
I2S1_8CH_SCLK_TX_M0/M1	Pull-Down	Series 22ohm Resistor	Bit clock output (TX, associated with SDOx)
I2S1_8CH_SCLK_RX_M0/M1	Pull-Down	Series 22ohm Resistor	Master: Bit clock output (RX, associated with SDIx) ;Slave: Bit clock input
I2S1_8CH_LRCK_TX_M0/M1	Pull-Down	Series 22ohm Resistor	Frame clock output (TX, associated with SDOx).
I2S1_8CH_LRCK_RX_M0/M1	Pull-Down	Series 22ohm Resistor	Frame clock, Master: Frame clock output (RX, associated with SDIx) ;Slave: Frame clock input
I2S1_8CH_SDO0_M0/M1	Pull-Down	Series 22ohm Resistor	Data Output channel 0
I2S1_8CH_SD01SDI3_M0/M1	Pull-Down	Series 22ohm Resistor	Data Output channel 1 / Input channel 3
I2S1_8CH_SDO2SDI2_M0/M2	Pull-Down	Series 22ohm Resistor	Data Output channel 2 / Input channel 2
I2S1_8CH_SDO3SDI1_M0/M2	Pull-Down	Series 22ohm Resistor	Data Output channel 3 / Input channel 1
I2S1_8CH_SDI0_M0/M1	Pull-Down	Series 22ohm Resistor	Data Input channel 0

Note:
I2S1_8CH_M0 and I2S1_8CH_M1 actually belong to the same group of I2S inside the chip. In practical applications, only the same group can be selected simultaneously, that is, either M0 or M1 can be chosen.

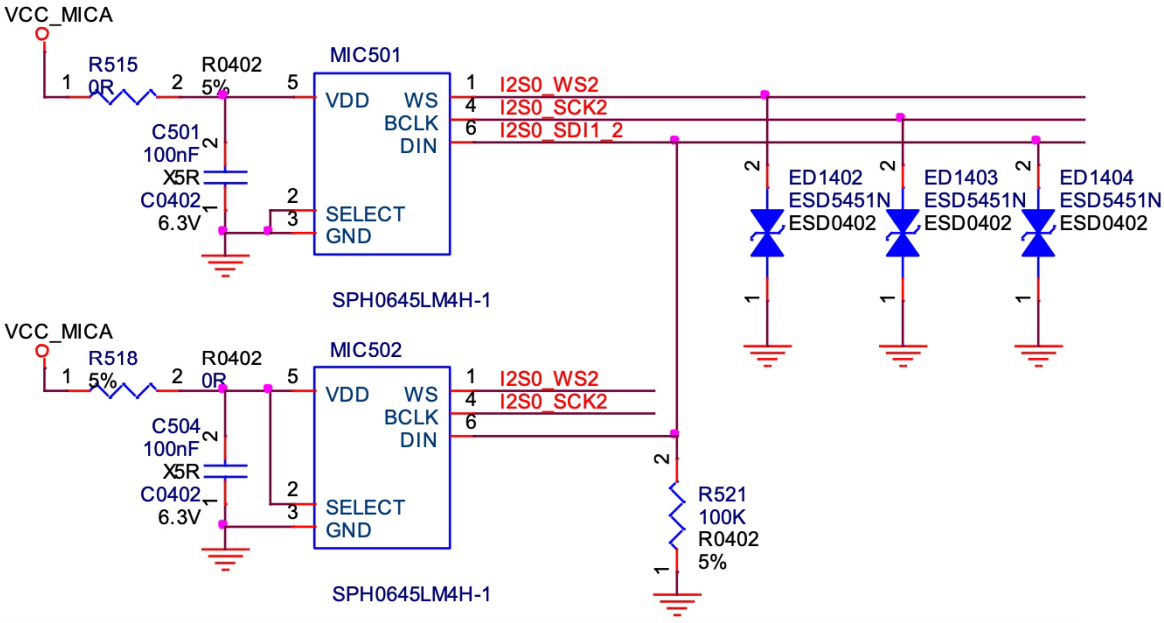


Figure 5: *I2S Microphone Circuit*

3.4.1.1 I2S Microphone Circuit The I2S microphones are required to be provided with the I2S_SCLK (bit clock signal) and I2S_LRCK (frame clock signal) of the I2S. Moreover, the DIN pins of the data of the two I2S microphones are jointly connected to the same I2S_SDI line. This means that the data of the left and right channels can be transmitted through only one data line, and which channel each of the two microphones corresponds to can be set by means of a signal pin (SELECT signal).

When SELECT = low level, it indicates that the data of the left channel is being transmitted; when SELECT = high level, it indicates that the data of the right channel is being transmitted. During the design process, the left and right channel levels need to be correctly set according to the arrangement of the microphones. There is a polarity configuration bit in the I2S register of RK3308B, which can invert the left and right polarities.

Note:
Since the microphone must have an opening design in the form of voice products, in order to improve the electrostatic discharge (ESD) resistance of the system, ESD protection devices need to be added to the I2S_SCLK, I2S_LRCK, and I2S_SDI lines. The ESD protection devices should be placed close to the microphone.

3.4.2 PDM

The Radxa rCore-RK3308 is equipped with a set of standardized PDM interfaces. This PDM interface can only operate in the Master Receive mode. Its sampling accuracy ranges from 16 to 24 bits, and the sampling rate can reach up to 192 kHz. The PDM interface includes one CLK output interface and four SDI input interfaces. The PDM interface can be multiplexed to PDM_M0, PDM_M1, and PDM_M2. Among them, PDM_M0 and PDM_M1 are in the VCCIO1 power domain, while PDM_M2 is located in the VCCIO2 power domain. The main purpose of multiplexing it into three groups is to enable users to have greater flexibility when carrying out product design work, allowing them to make appropriate selections according to the functional requirements of the product and the easiest implementation schemes.

Note:
PDM_M0, PDM_M1 and PDM_M2 actually belong to the same group of PDM inside the chip. In practical applications, only the same group can be selected simultaneously, that is, either M0, M1 or M2 can be chosen.

Table 7: *PDM Interface Design*

Signal	Pull-Up/Down	Connection	Description
PDM_8CH_CLK_M0/M1/M2	Pull-Down	Series 22ohm Resistor	Clock output
PDM_8CH_SDI0_M0/M1/M2	Pull-Down	Series 22ohm Resistor	Data Input channel 0
PDM_8CH_SDI1_M0/M1/M2	Pull-Down	Series 22ohm Resistor	Data Input channel 1
PDM_8CH_SDI2_M0/M1/M2	Pull-Down	Series 22ohm Resistor	Data Input channel 2
PDM_8CH_SDI3_M0/M1/M2	Pull-Down	Series 22ohm Resistor	Data Input channel 3

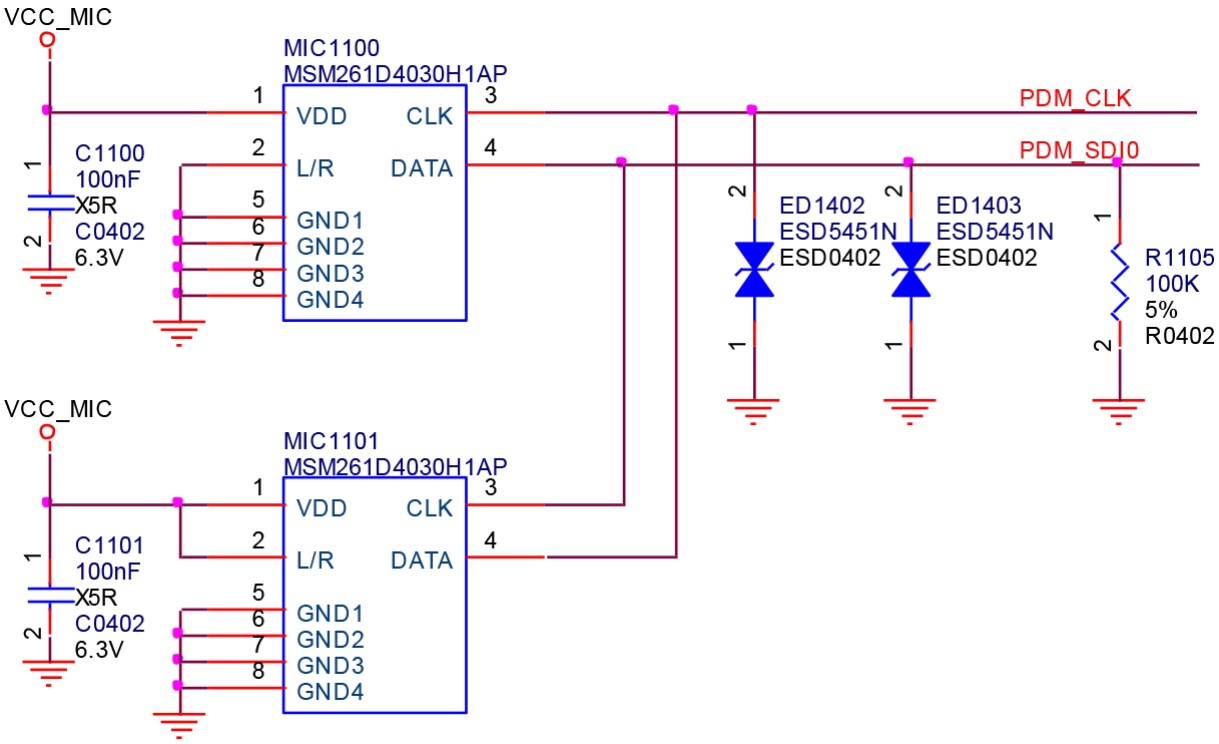


Figure 6: *PDM Microphone Circuit*

3.4.2.1 PDM Microphone Circuit PDM microphones are required to be provided with the PDM_CLK signal. Meanwhile, the DATA pins of the two PDM microphones are connected to the same PDM_SDI line. This means that the data of the left and right channels can be transmitted through a single data line, and which channel each of the two microphones corresponds to can be set by means of a signal pin (L/R signal).

The correspondence between the high and low levels of the L/R signal and the left and right channels varies among different PDM microphone manufacturers. It needs to be set according to the descriptions in the microphone specification sheets.

During the design process, the left and right channel levels need to be correctly set according to the arrangement of the microphones. There is a polarity configuration bit in the PDM register of RK3308B, which can invert the left and right polarities.

Note:
Since the microphone must have an opening design in the form of voice products, in order to improve the electrostatic discharge (ESD) resistance of the system, ESD protection devices need to be added to the `PDM_CLK` and `PDM_SDI` lines. The ESD protection devices should be placed close to the microphone.

3.4.3 S/PDIF

The Radxa rCore-RK3308 has one set of S/PDIF interfaces. It supports both S/PDIF output and input functions. It supports resolutions of 16 bits, 20 bits and 24 bits. The maximum sampling rate it can support is 192 kHz.

3.5 SDMMC

The Radxa rCore-RK3308 is equipped with an SDMMC interface, which supports the SDMMC 3.0 protocol. It has the following characteristics:

- The functions of SDMMC and UART2 are multiplexed with each other.
- VCCIO_SDMMC serves as the IO power supply. In the SD 2.0 mode, it requires an external 3.3V power supply; while in the SD 3.0 mode, it requires an external adjustable power supply of 3.3V/1.8V to ensure the stable operation of the device in different modes.

Table 8: *SDMMC Interface Design*

Signal	Pull-Up/Down	Connection	Description
SDMMC_D[3:0]	Pull-Up	Series 22ohm Resistor	SD data sending/receiving
SDMMC_CLK	Pull-Down	Series 22ohm Resistor	SD clock transmission
SDMMC_CMD	Pull-Up	Series 22ohm Resistor	SD command send/receive

3.6 UART Debug

The Radxa rCore-RK3308 uses UART0 for serial port debugging by default.

Table 9: *UART0 Interface Design*

Signal	Connection	Description
UART0_RX	Direct Connection	Data Input
UART0_TX	Direct connection	Data Output

3.7 USB 2.0

The Radxa rCore-RK3308 is equipped with two sets of USB 2.0 interfaces. Among them, USB0 is of the OTG interface type, while USB1 is of the HOST interface type.

- The USB0 interface is set as the system firmware burning port by default, and this interface must be used during the debugging process.

- The USB_ID has an internal pull-up resistor of about 150K, which is pulled up to USB_AVDD_1V8. At this time, the OTG port is in the Device mode by default. When the USB_ID is at a low level and the USB2.0 OTG is used as a HOST port, the controller will also switch to the HOST state.

Table 10: *USB 2.0 Interface Design*

Signal	Connection	Description
USB0_DP/DM	Series 22ohm Resistor	USB2.0 OTG differential signal
USB_ID	Series 100ohm Resistor(Internal Pull-Up)	USB2.0 OTG ID identification, required for Micro-B interface
USB_VBUS	-	USB2.0 OTG insertion detection
USB1_DP/DM	Series 22ohm Resistor	USB2.0 HOST differential signal

3.8 100Mbps Ethernet MAC

The RK3308B has an integrated MAC for 100Mbps Ethernet internally. With this MAC, it can be connected externally to various Ethernet PHY chips to achieve the functionality of a 100Mbps network. When carrying out specific circuit design, please refer in detail to the design documents provided by the original manufacturers of the 100Mbps Ethernet PHY to ensure the accuracy and standardization of the design and guarantee the stable realization and efficient operation of the network functions.

- The reset of the PHY by the MAC can be controlled by using GPIO. In addition, it can also be achieved by using an RC hardware reset circuit. What needs to be particularly noted during this process is that if an RC hardware reset circuit is adopted, the power supply of the PHY must be in a controllable state.
- The interface used for transmitting control and status information between the MAC and the PHY is the MDIO interface. Associated with it are the clock MDC signal and the data MDIO signal. It should be particularly noted that, in order to ensure the stability and accuracy of signal transmission, the MDIO signal must be pulled up.

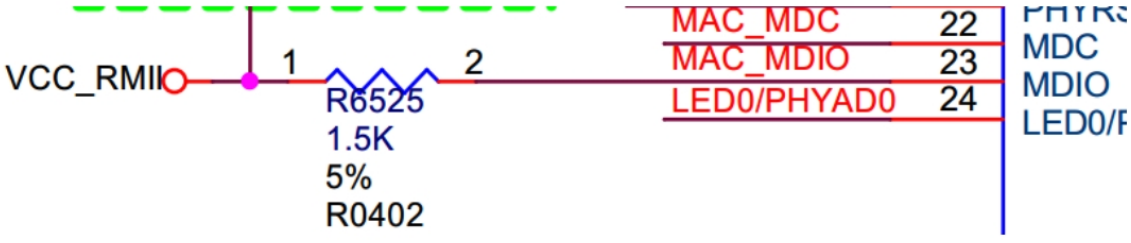


Figure 7: *RMII MDIO Circuit*

Note:
The clock signal required for the operation of the PHY can be either generated by using an external crystal or provided by the MAC_CLK output of the RK3308B chip.

Table 11: *100Mbps Ethernet Mac Interface Design*

Signal	Pull-Up/Down	Connection	Description
MAC_CLK	Pull-Down	Series 22ohm Resistor	MAC master clock output
MAC_TXD[2:0]	Pull-Down	Series 22ohm Resistor	Data transmission
MAC_RXD[2:0]	Pull-Down	Series 22ohm Resistor	Data Reception
MAC_TXEN	Pull-Down	Direct connection	Send data enable
MAC_RXDV	Pull-Down	Direct connection	Receive data valid indication
MAC_MDC	Pull-Down	Direct connection	Configuring the Interface Clock
MAC_MDIO	Pull-Down	Direct connection	Configuring Interface I/O

3.9 LCD Controller

The LCDC interface equipped on the Radxa rCore-RK3308 has 18-bit data signals, namely LCDC_D0 to LCDC_D17, and this interface can support RGB screens and MCU screens. When using 18/24-bit RGB screens and 8-bit/16-bit MCU screens, the corresponding connection relationships of the LCDC signals can refer to the following diagram:

Correspondence between LCDC DATA and RGB/MCU				
LCDC	18bit RGB Panel	24bit RGB Panel	16bit MCU Panel	8bit MCU Panel
LCDC_D0	B0	B2	DB0	DB0
LCDC_D1	B1	B3	DB1	DB1
LCDC_D2	B2	B4	DB2	DB2
LCDC_D3	B3	B5	DB3	DB3
LCDC_D4	B4	B6	DB4	DB4
LCDC_D5	B5	B7	DB5	DB5
LCDC_D6	G0	G2	DB6	DB6
LCDC_D7	G1	G3	DB7	DB7
LCDC_D8	G2	G4	DB8	
LCDC_D9	G3	G5	DB9	
LCDC_D10	G4	G6	DB10	
LCDC_D11	G5	G7	DB11	
LCDC_D12	R0	R2	DB12	
LCDC_D13	R1	R3	DB13	
LCDC_D14	R2	R4	DB14	
LCDC_D15	R3	R5	DB15	
LCDC_D16	R4	R6		
LCDC_D17	R5	R7		
LCDC_CLK	LCDC_CLK	LCDC_CLK	MCU_CMD (Command)	MCU_CMD (Command)
LCDC_HSYNC	LCDC_HSYNC	LCDC_HSYNC	MCU_WR (write signal)	MCU_WR (write signal)
LCDC_VSYNC	LCDC_VSYNC	LCDC_VSYNC	MCU_CS (Chip select)	MCU_CS (Chip select)
LCDC_DEN	LCDC_DEN	LCDC_DEN	MCU_RD (Read signal)	MCU_RD (Read signal)

Figure 8: *LCDC Signal Correspondence*

Note:
When used in combination with an MCU screen, the read (RD), write (WR), chip select (CS), and control signal (CMD) on the MCU screen must be operated strictly in accordance with the signal control methods corresponding to the diagram, and must not be randomly changed to other GPIO controls.

3.10 SARADC

The Radxa rCore-RK3308 has 6 channels of SARADC. The power supply is 1.8V and the sampling accuracy is 10 bits. The RK3308B defaults to using ADC_KEY_IN1 of SARADC as the function key input port.

The input key value can be set by adjusting the ratio of the voltage divider resistors. It is recommended that the interval between any two key values be greater than 35 during design. ADC_KEY_IN1 is also multiplexed as the system upgrade key input port.

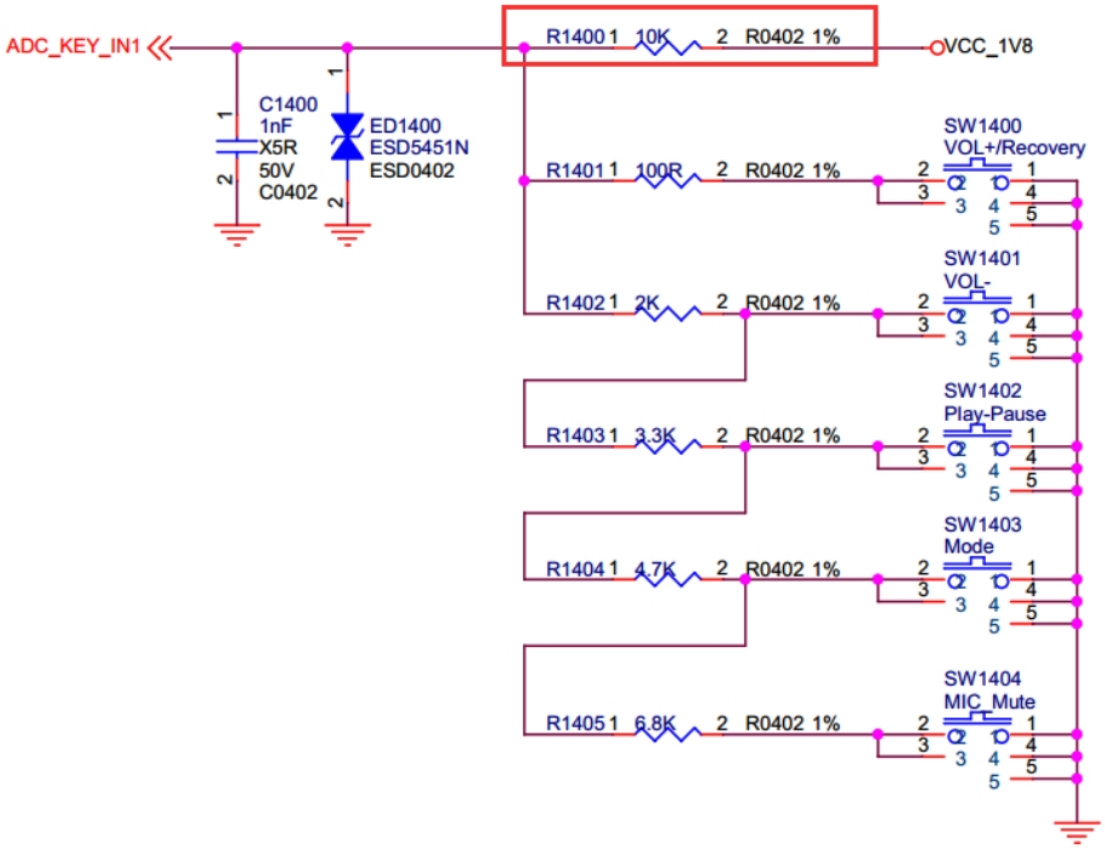


Figure 9: *SARADC Circuit*

As shown in the figure, the first key, that is, the VOL+/Recovery key, functions as VOL+ when the system is working normally; it is multiplexed as the Recovery mode only when powering on. The specific usage method is as follows: on the premise that the firmware has been burned into the system, press the VOL+/Recovery key to pull down ADC_KEY_IN1 when the system starts. Keep ADC_KEY_IN1 at 0V level (not exceeding 100mV at most), and then the Radxa rCore-RK3308 enters the Rockusb burning mode. When the PC recognizes the USB device, release the key to make ADC_KEY_IN1 return to a high level (1.8V), and then the firmware can be burned.

Note:
The ADC_KEY_IN1 signal must be pulled up.

3.11 Maskrom Mode

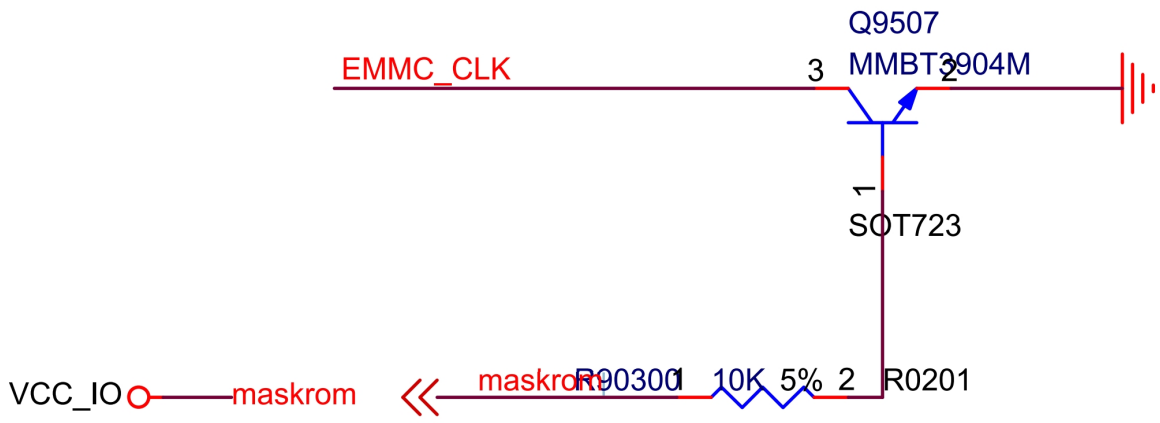


Figure 10: *Maskrom Circuit*

The maskrom pins of Radxa rCore-RK3308 have specific functions. When the maskrom pins are pulled up, the Radxa rCore-RK3308 can enter the maskrom mode. In this mode, the operation of downloading firmware to the onboard eMMC can be performed. It should be noted that the maskrom mode needs to be used in conjunction with the RKDevTool software of RK.

Note:
Regarding the downloaded RKDevTool tool.

3.12 Wireless Connection

The Radxa rCore-RK3308 adopts the Realtek RTL8723DS - CG. The Realtek RTL8723DS - CG is a single-chip that complies with the 802.11bgn standard and operates in the 2.4G frequency band. This chip integrates the functions of Wireless LAN (WLAN) and Bluetooth 2.1/4.2. Among them, the WLAN is connected via the SDIO interface, while the Bluetooth

is connected through the UART interface. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip.

3.12.1 Antenna Connection

The Radxa rCore-RK3308 does not come with any pre-connected antennas. It requires appropriate antennas for wireless and Bluetooth functionality. Depending on the enclosure design, you can choose to use internal or external antennas. The location of the antenna connection on the top side of the board is indicated as item 6 in Figure 2.

The wireless module utilizes a standard 2x2 mm RF micro coaxial receptacle (connector) with an outer diameter of 1.5 mm. When selecting the appropriate plug, ensure it is compatible with the cable diameter. Refer to the figure below for the minimum requirements and dimensions of the compatible RF connectors and mating plugs.

- Receptacle physical outline: 2mm x 2mm x 0.6mm
- Receptacle outer diameter: 1.5mm

The example Plug model is I-PEX MHF® I Type Plug.

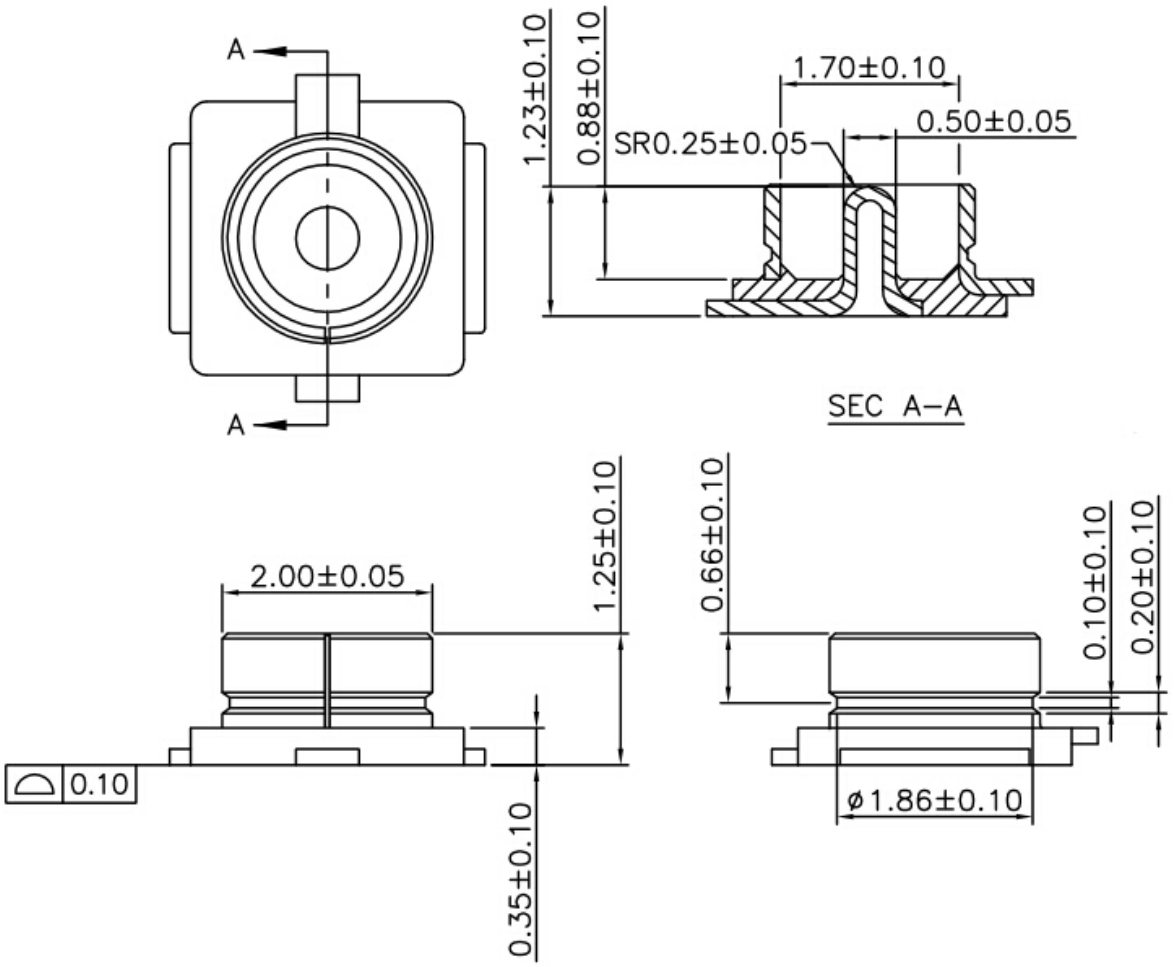


Figure 11: *Antenna Dimensions*

4 Mechanical

The Radxa rCore-RK3308 is measuring 35 × 35mm.

- The following figures provide a visual representation of the Radxa rCore-RK3308's mechanical form factor. All dimensions are given in millimeters (mm).

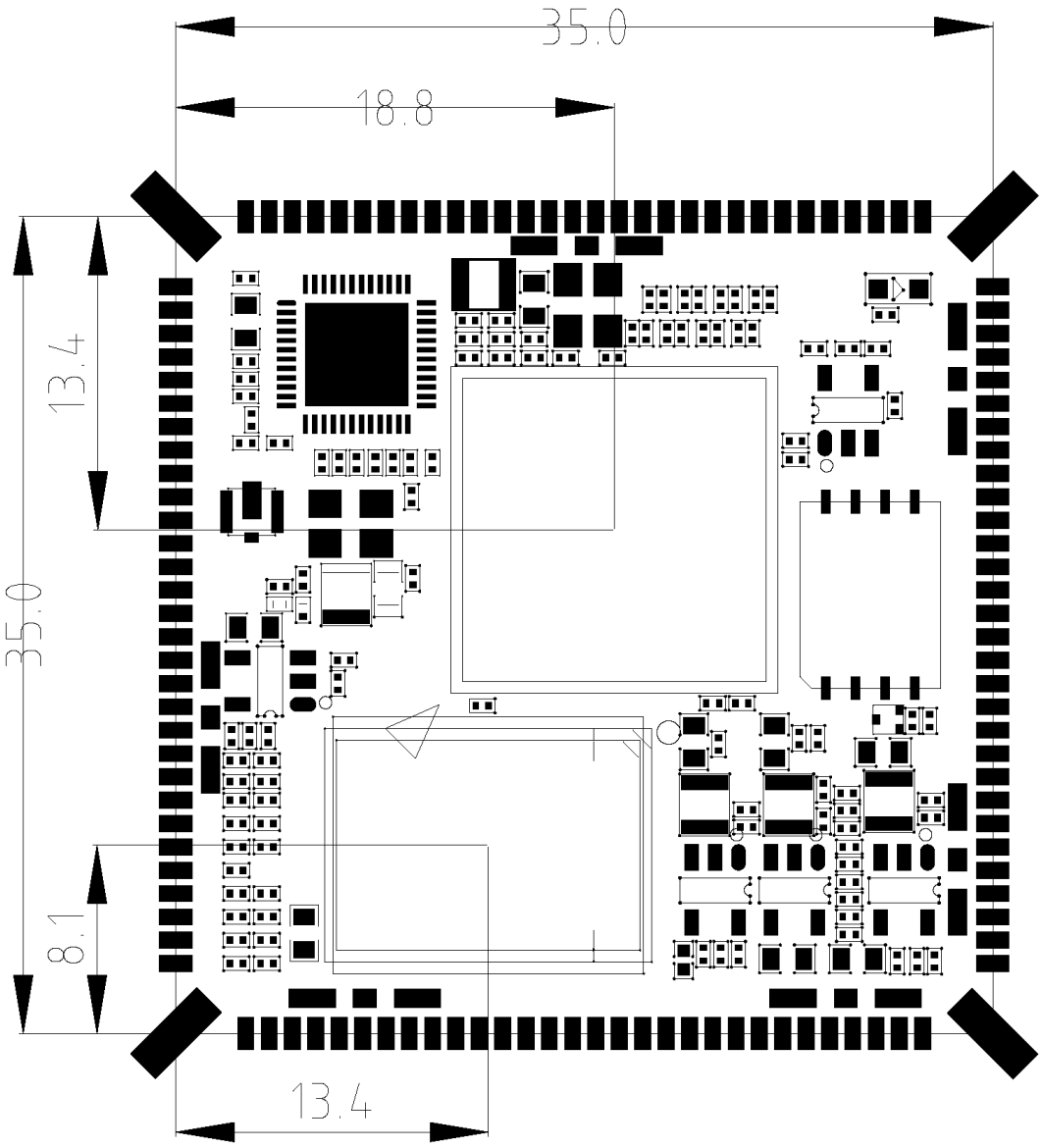


Figure 12: *Dimension*

5 Electrical Characteristics

5.1 DC Characteristics for Digital GPIO 3.3V

Parameters	Symbol	Min	Typ	Max	Unit
Input Low Voltage	Vil	-0.3	NA	3.3x0.3	V
Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
Output Low Voltage	Vol	NA	NA	0.4	V
Output High Voltage	Voh	3.3-0.4	NA	NA	V
Pullup Resistor	Rpu	33.7	58	101.5	Kohm
Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm

5.2 DC Characteristics for Digital GPIO 1.8V

Parameters	Symbol	Min	Typ	Max	Unit
Input Low Voltage	Vil	-0.3	NA	1.8x0.3	V
Input High Voltage	Vih	1.8x0.7	1.8	1.8+0.3	V
Output Low Voltage	Vol	NA	NA	0.4	V
Output High Voltage	Voh	1.8-0.4	NA	NA	V
Pullup Resistor	Rpu	35	62.9	120	Kohm
Pulldown Resistor	Rpd	35.1	61	113.9	Kohm

5.3 Electrical Characteristics for Digital GPIO 3.3V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	10	uA
		Vin = 3.3V, pull down enabled	NA	NA	106.4	uA
Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
		Vin = 0V, pull up enabled	NA	NA	107.8	uA

5.4 Electrical Characteristics for Digital GPIO 1.8V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	10	uA
		Vin = 1.8V, pull down enabled	NA	NA	61.3	uA
Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
		Vin = 0V, pull up enabled	NA	NA	61.4	uA

5.5 Electrical Characteristics for USB 2.0

- Transmitter

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
High input level	VIH	-	NA	1.1	NA	V
Low input level	VIL	-	NA	0	NA	V
Output Resistance	ROUT	Classic Mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS Mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS Mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS) mode; Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS) mode; Io=6mA	2.2	2.7	NA	V
		HS Mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS) mode; Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS) mode; Io=6mA	NA	0.3	0.8	V
		HS Mode; Io=0mA	-40	0	40	mV

- Receiver

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Receiver Sensitivity	RSENS	Classic mode		±250		mV
		HS Mode		±25		mV
Receiver Common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS Mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS Mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance		seen at D+ or D-	NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High Output level	VOH		NA	3.3	NA	V
Low Output level	VOL		NA	0	NA	V

5.6 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution				10		bit
Effective Number of Bit	ENOB			9		bit
Differential Nonlinearity	DNL		-1		+1	LSB
Integral Nonlinearity	INL		-2		+2	LSB
Input Voltage Range	VIN		0		1	AVDD
Input Capacitance	CIN			10		pF
Sampling Rate	fs				1	MS/s
Analog power	IAVDD	FS = 1MS/s		450		uA
Digital power	IVDD	FS = 1MS/s		50		uA
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IVDD	Power down		1		uA

6 Appendix A: Troubleshooting

6.1 Hardware Checklist

1. Check if the `VCC5V0_SYS` supply is good. Ensure that the power supply is providing a stable voltage of 5V to the Radxa rCore-RK3308. Verify the voltage using a multimeter or a power supply tester. Any fluctuations or deviations from the expected voltage may cause instability or failure of the module.

2. Check if the green LED on the rCore-RK3308 is on. The green LED indicates that the module is receiving power and is properly connected. If the LED is not illuminated, check the power supply connections, ensure the power source is active, and verify that the power input to the module is correct.
3. When the eMMC on rCore-RK3308 is empty(factory default), without SD Card, the rCore-RK3308 should stay in maskrom mode after power on. Plug the USB OTG into a PC and check if any USB devices are detected. Connect the rCore-RK3308 with IO board to a computer using the USB OTG port and verify if the PC recognizes the device. Check the device manager or system logs to see if the rCore-RK3308 is detected as a USB device. Additionally, measure the voltages of `USB_DET` and `USB_ID` pins on the module to ensure they are above 1V, indicating proper power and identification signals. Measure `USB_OTG_DM`/`DP` to ensure that the USB data lines are functioning correctly, as improper communication can cause connectivity issues.
4. Verify the connections and integrity of other hardware components. Ensure that all necessary connections between the Radxa rCore-RK3308 and other peripherals or components on the carrier board are secure and properly seated. Check for any loose or disconnected cables, connectors, or modules. Inspect the physical condition of the components, looking for any signs of damage or irregularities.

By following this hardware checklist, you can troubleshoot common hardware-related issues and ensure that the Radxa rCore-RK3308 and its associated components are functioning correctly.

If after above the hardware checklist the Radxa rCore-RK3308 is still not recognized or you encounter persistent issues, don't hesitate to seek further assistance. Radxa provides dedicated support channels to help resolve any technical difficulties you may encounter.

6.2 Boot Order

The Radxa rCore-RK3308 supports multiple boot media options. Upon system reset, the bootrom will search for booting code in the following sequence from external storage media:

- NAND Flash
- eMMC
- SDMMC

If no bootable code is found in any of the boot media, the rCore-RK3308 will enter the maskrom mode. In this mode, `USB_OTG` will be set to device mode, waiting for commands from the host PC.

6.3 Serial Console

The low-level debug serial console is enabled by default on the Radxa rCore-RK3308 using the `UART0_RX` and `UART0_TX` pins. The baud rate for the serial console is set to **1500000** (1.5Mbps). For instructions on setting up the serial console on a host PC, please refer to the following link: https://wiki.radxa.com/Rock3/dev/serial-console

7 Appendix B: Availability

7.1 Availability

Radxa guarantees availability of the Radxa rCore-RK3308 until at least September 2033.

7.2 Support

For support please see the hardware documentation section of the Radxa Documentation website and post questions to the Radxa forum.

8 Appendix C: Alternative Function

8.1 Pinout

The Pinout document for Radxa rCore-RK3308 offers a detailed explanation of pin assignments and connectivity. You are welcome to visit Radxa rCore-RK3308 Pinout to access this valuable resource. Download it for comprehensive information.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