RK3308 Series S-Version Chip

Hardware Design Modification Introduction

RK3308 old process chip is pin to pin compatible with RK3308 series S-version chip, and the circuits of them can be designed compatible. But it is necessary to pay attention to the following modification points and adjust the related components.

This document aims to help customers quickly complete the switch of the RK3308 series S-version chip based on the current circuit design. The corresponding relationship between the chips is as follows:

Old process chip silk screen printing	Corresponding to S-version chip silk screen printing	Remark
RK3308、RK3308B	RK3308B-S	
RK3308G、RK3308H	RK3308H-S	Sealed DDR2 version

Revision History

Version	Revision Description	Remark
20210827	Initial Release	
V10_20211009	Update the description of the VDD_CORE power supply. The voltage regulating circuit is consistent with the RK3308B parameters, and the voltage is controlled by software in the power-on/standby state.	
V1.0.1 20211018	1. Modify the file name; 2. Add the comparison description between RK816B-3 and RK816B-6; 3. Add the description of the discrete power supply scheme for the combination of VDD_CORE/VDD_LOG	

1. Hardware Main Changes

1) The ballmap of the old process chip and the RK3308 series S-version chip are the same, but due to the difference in process, the following power supply voltage changes are involved：

Old process chip Net Name	Old process chip Supply Voltage (Typical Value)	S-version chip Net Name	S-version chip Supply Voltage (Typical Value)
VDD_LOG	1.0V	VDD_LOG	0.9V
VDD_CORE	1.0V	VDD_CORE	0.9V
PLL_AVDD_1V0	1.0V	PLL_AVDD_0V9	0.9V
USB_VDD_1V0	1.0V	USB_VDD_0V9	0.9V

For the modification example of the power supply voltage, refer to the chapter4/5/6 of this article, and refer to the corresponding reference according to the specific product power supply plan.

2) Due to the update of USB PHY, the external circuit of PIN C15 needs to be adjusted

Old process chip Net Name	Old process chip Circuit Connection method	S-version chip Net Name	S-version chip connection method
USB_EXTR	Pull down to ground with a 133R 1% resistance	NC	Leave floating

For the modification example of USB_EXTR, refer to Chapter 7 of this article.

2. IO Power Domain Configuration Verification (very important)

The IO level of the main control power domain must be consistent with the IO level of the external peripheral chip. Note that the voltage configuration of the software IO power domain of the main control terminal must be consistent with the hardware power supply voltage, otherwise the chip IO may be damaged. For example, if the hardware IO level is 1.8V, the voltage configuration of the software should be 1.8V accordingly; the hardware IO level is 3.3V, and the voltage configuration of the software should be 3.3V.

Please check the actual power supply of the hardware IO power domain according to the specific design.

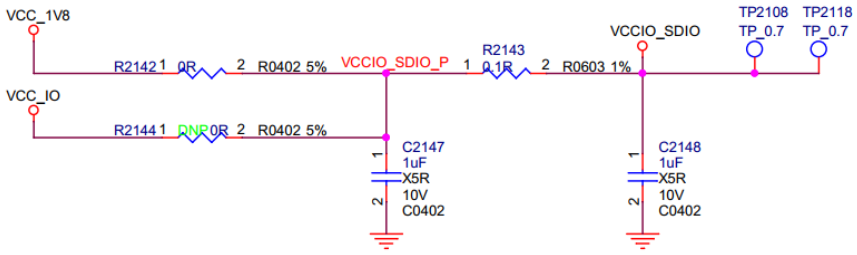
In software, the configuration node of the IO power domain is generally in the board-level dtsi, and the node information is as follows:

```
&io_domains {
    status = "okay";

    vccio0-supply = <&vcc_io>;
    vccio1-supply = <&vcc_io>;
    vccio2-supply = <&vcc_io>;
    vccio3-supply = <&vcc_io>;
    vccio4-supply = <&vcc_io>;
    vccio5-supply = <&vcc_io>;
};
```

The board-level dtsi (such as: rk3308-evb-v1x.dtsi、rk3308b-evb-v10.dtsi、rk3308-voice-module-v1x-aarch32.dtsi) in the RK3308 SDK is configured according to the actual hardware power supply of the EVB board. Many customers include the dtsi of the rk3308 evb directly in their board-level dts. Be sure to pay special attention to check whether the IO power domain matches the current hardware setting.

It should be reminded that there are reserved power supply options in the reference design, such as the following circuit diagram. When checking, pay attention to the actual connection of power supply, if the BOM table is different from the schematics, the hardware engineers and software engineers need to check clearly to avoid errors.



3. The Difference in IO Drive Strength (very important)

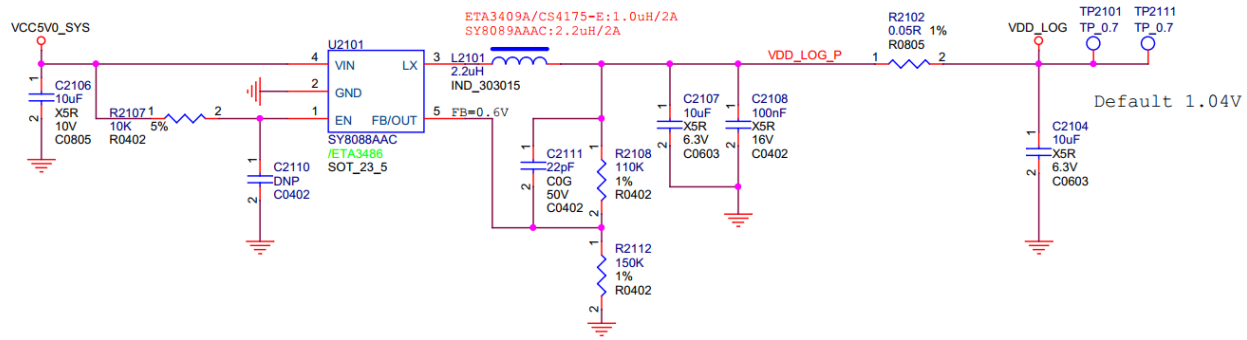
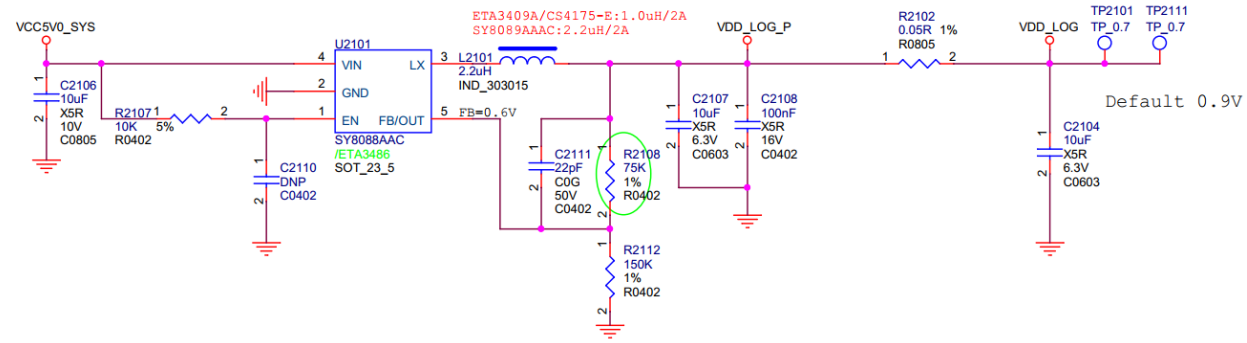
There are some differences in IO drive strength between the old process chip and the S-version chip. The released SDK and patch have made corresponding adaptations to the hardware reference configuration of the RK platform. Mainly for Ethernet, Wi-Fi, FLASH and TF cards.

If there have been IO drive strength modifications on the products of the old process chip before, pay special attention to testing whether the current drive strength configuration can meet the product requirements of the S-version chip. If the requirements are not met (for example, the signal test is not satisfied or the function is problematic), it's need to adjust the drive strength configuration according to the method mentioned in the software document "RK3308B-S&RK3308H-S Software Compatibility Introduction".

4. Circuit Parameters Comparison and Modification Examples of Typical Discrete Power Supply Scheme (Take Reference Design/EVB as an Example)

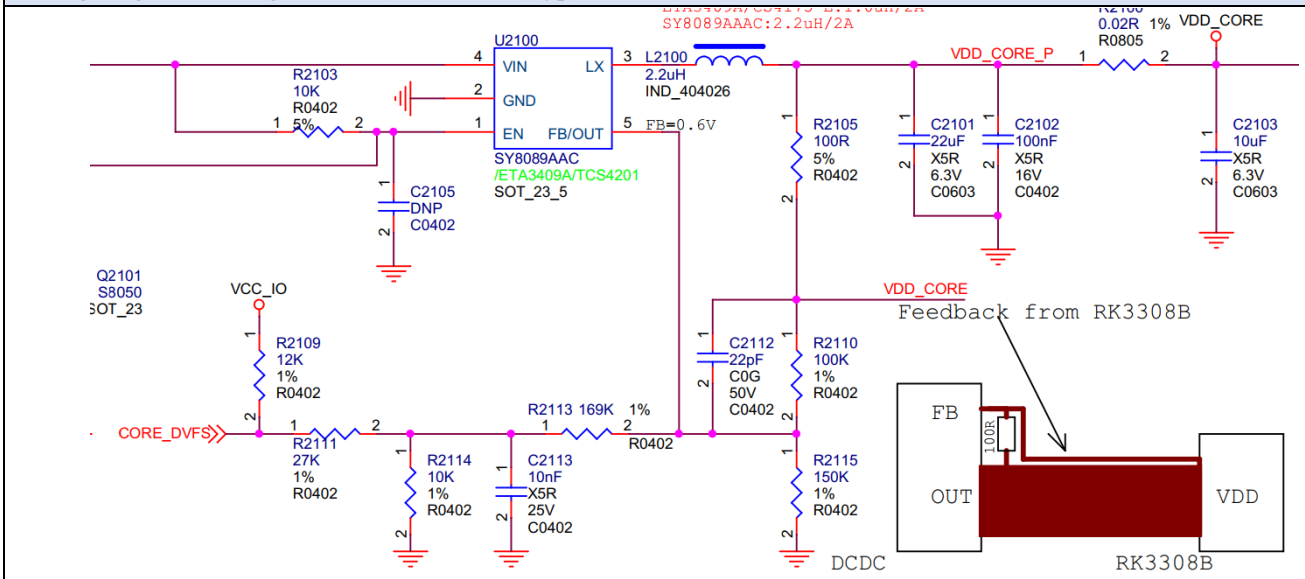
The typical discrete power supply scheme circuit refers to a discrete power supply scheme that VDD_CORE and VDD_LOG are supplied separately. VDD_CORE supports voltage regulation through the PWM pin, and VDD_LOG is a fixed voltage.

1) VDD_LOG Power Supply

Old process chip VDD_LOG power supply circuit parameters are as shown in the figure below. The Typical value is 1.0V, and the actual circuit default value is 1.04V.

S-version chip VDD_LOG power supply circuit parameters are shown in the figure below, and the Typical value is 0.9V, R2108 is changed to 75K 1%.


2) VDD_CORE Power Supply

Old process chip VDD_CORE power supply circuit parameters are shown in the figure below. Typical value is 1.0V. Voltage regulation range: 0.826 (min)-1.015 (Typ)-1.34V (Max)



S-version chip VDD_CORE power supply circuit parameters are the same as old process chip.

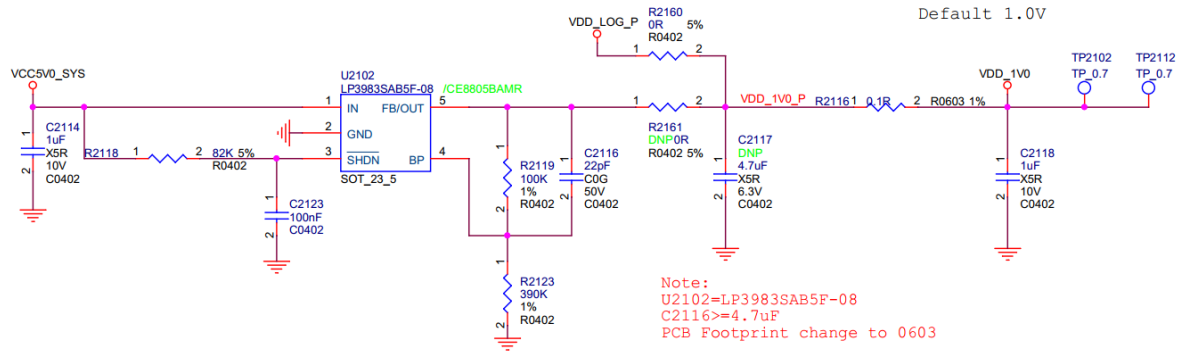
The circuit is consistent with old process chip, and the state after powered-on/standby is controlled by the software through the PWM pin, and the software configuration of frequency-voltage table (opp table) needs to be updated

The circuit is not adjusted and the same as old process chip.

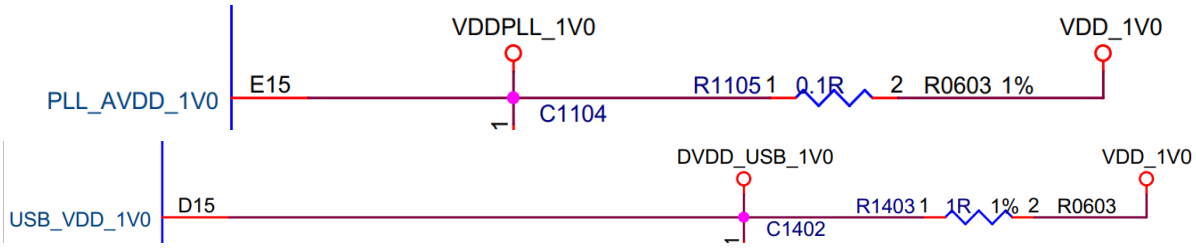
3) VDD_1V0 power supply (PLL_AVDD、USB_VDD)

By default, VDD_1V0 is powered from the VDD_LOG supply, that means the source of VDD_1V0 is the same buck DC-DC. VDD_1V0 takes power from VDD_LOG, and the voltage is the same as VDD_LOG. As shown below, LDO U2102 is only a reserved design and is not stuffed as default. For the design of separate power supply, please pay attention to the adjustment of the R2119 resistance value.

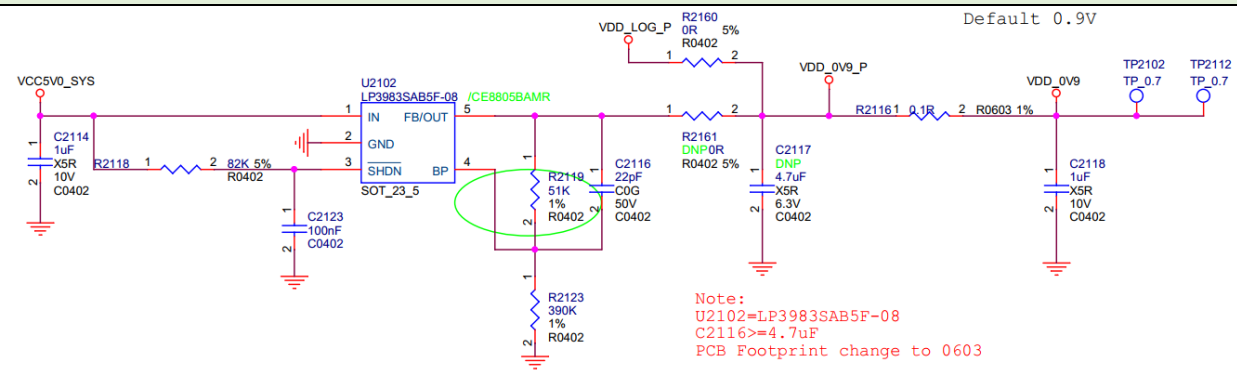
Old process chip PLL_AVDD, USB_VDD power supply circuit parameters are shown in the figure below, and the Typical value is 1.0V.



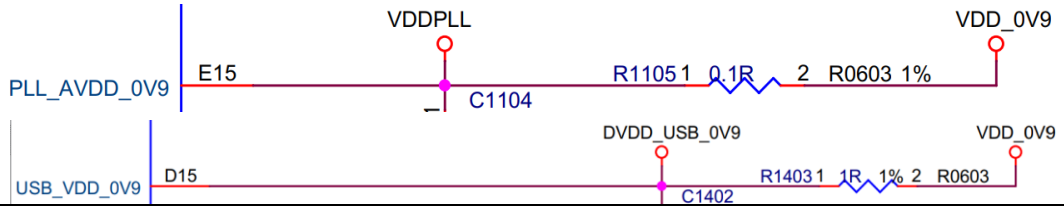
Following figure shows the related pins of old process chip power supply:



S-version chip PLL_AVDD, USB_VDD power supply circuit parameters are shown in the figure below, and the Typical value is 1.0V. The resistance of R2119 is changed to 51K 1%.



Following figure shows the related pins of S-version chip power supply:



5. RK816B-X PMIC Power Supply Scheme Parameter Comparison and Modification Example (take reference design/EVB as an example)

The timing and default voltage of RK816B-3 PMIC are applicable to old process chips: RK3308, RK3308G, RK3308B, RK3308H.

The timing and default voltage of RK816B-6 PMIC are applicable to S-version chips: RK3308B-S, RK3308H-S.

Please pay attention to the model distinction when placing an order and using it. No other peripheral components have been modified in the power supply part.

The differences are shown in the following table:

Name	Rate Current(A)	Application Usage	Default Status	RK816B-3		RK816B-6	
				Default Voltage(V)	Step(*2ms)	Default Voltage(V)	Step(*2ms)
BUCK1	2	VDD_CORE	ON	1.1	2	0.9	2
BUCK2	2	VDD_LOG&VDD_1V0	ON	1.1	1	0.9	1
BUCK3	1	VCC_DDR	ON	Adjust	3	Adjust	3
BUCK4	1	VCC_IO	ON	3.3	1	3.3	4
BOOST	2		OFF	5	OFF	5	OFF
LDO1	0.3	Reserved	OFF	1.8	OFF	1.8	OFF
LDO2	0.3	VCC_1V8	ON	1.8	1	1.8	2
LDO3	0.1	Reserved for VDD_1V0	ON	1.1	1	0.9	1
LDO4	0.3	Reserved	OFF	3.3	OFF	3.3	OFF
LDO5	0.3	Reserved	ON	3.3	4	3.3	4
LDO6	0.3	Reserved	ON	3.3	4	3.3	4

6. VDD_CORE/VDD_LOG Combined Discrete Power Supply Scheme Circuit Parameter Comparison and Modification Example

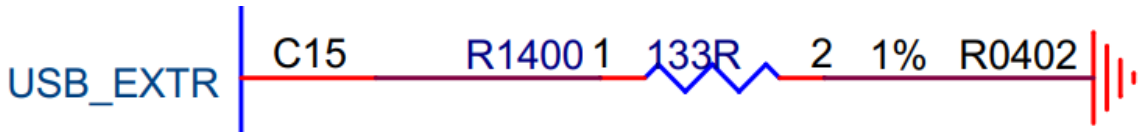
For some costdown schemes, VDD_CORE and VDD_LOG are combined. It should be noted that the voltage adjustment ranges of the two are related. Therefore, the upper limit of the voltage adjustment allowed by VDD_CORE is affected by VDD_LOG, which will limit the maximum frequency of the CPU.

The number of customers using this scheme is very small, relevant customers should consult Rockchip for modification suggestions.

The following table shows the maximum CPU frequency that can be supported by the discrete power supply solution combined with VDD_CORE/VDD_LOG:

Chip	The highest voltage of VDD_CORE/VDD_LOG supported	Corresponding to the highest frequency supported
Old process chip RK3308, RK3308G RK3308B, RK3308H	1.1V	912MHz
S-version chip RK3308B-S, RK3308H-S	1.0V	816MHz

7. USB_EXTR Circuit Parameter Comparison and Modification Example

Old process chip USB_EXTR(PIN C15) is connected with external 133R 1% reference resistor

PIN C15 of S-version chip is NC pin. Leave Pin C15 floating. The R1400 should not be stuffed.