Rockchip RK3308 Datasheet

Revision 1.0
Feb. 2018

Revision History

Date	Revision	Description
2018-02-27	1.0	Initial released

Table of Content

Figure Index

Table Index

Warranty Disclaimer

Rockchip Electronics Co., Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co., Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co., Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co., Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co., Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co., Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co., Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co., Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co., Ltd does not convey any license under its patent rights nor the rights of others.
All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co., Ltd's products are trademarks of Rockchip Electronics Co., Ltd. and are exclusively owned by Rockchip Electronics Co., Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Copyright © 2018 Rockchip Electronics Co., Ltd.

Chapter 1 Introduction

1.1 Overview

RK3308 is a high-performance Quad-core application processor designed for intelligent voice interaction, audio input/output processing, and other digital multimedia applications. Embedded rich audio interfaces, such as I2S, PCM, TDM, PDM, SPDIF, HDMI ARC and so on, can meet different audio application development, reduce hardware development complexity and development cost.
Embedded Voice Activity Detection function will monitor human voice at any time, respond to human voice request timely and fast setup intelligent voice interaction application, which will also reduce hardware system power consumption and improve battery endurance.
RK3308 has high-performance external memory interface (DDR2/DDR3/DDR3L/LPDDR2) capable of sustaining demanding memory bandwidths.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Quad-core ARM Cortex-A35 CPU
- Full implementation of the ARM architecture v8-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- In-order pipeline with symmetric dual-issue of most instructions
- 256KB unified system L2 cache
- Include VFP v3 hardware to support single and double-precision operations
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A35_0: 1st Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_1: 2nd Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_2: 3rd Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_3: 4th Cortex-A35 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM

- External off-chip memory①
  - DDR2/DDR3/DDR3L/LPDDR2
  - 8bits Async Nand Flash
  - eMMC
  - SPI Nor/Nand Flash
  - SD Card

1.2.3 Internal Memory

- Internal BootRom
  - Support system boot from the following device:

- Async Nand Flash
- eMMC interface
- SPI Flash interface
- SDMMC interface

- Support system code download by the following interface:
  - USB OTG interface (Device mode)

- Internal SRAM
  - Size: 256KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR2/DDR3/DDR3L/LPDDR2)
  - Compatible with JEDEC standards
  - Compatible with DDR2-1600/DDR3-1600/DDR3L-1600/LPDDR2-1066
  - Support 16-bit data width, 1 ranks (chip selects), max 512MB addressing space per rank; total addressing space is 512MB(max) also
  - Low power modes, such as power-down and self-refresh for SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- Nand Flash Interface
  - Support async nand flash
  - Data bus width is 8bits
  - Support up to 1 chip select
  - Support LBA nand flash
  - Up to 16bits/1KB hardware ECC
  - Support configurable interface timing

- eMMC Interface
  - Compatible with standard iNAND interface
  - Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
  - Support three data bus width: 1-bit, 4-bit or 8-bit
  - Support up to HS200; but not support CMD Queue

- Serial Flash Interface
  - Support transfer data from/to SPI flash device
  - Support x1,x2,x4 data bits mode
  - Support up to 1 chip select

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - 2 separate voltage domains(CORE_VDD/LOGIC_VDD)
  - 4 separate cpu power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or

automatic clock gating control or power domain on/off control

- Timer
  - Six 64bits timers with interrupt-based operation for non-secure application
  - Six 64bits timers with interrupt-based operation for secure application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - Four on-chip PWMs(PWM0~PWM3) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Optimized for IR application for PWM3

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Interrupt Controller
  - Support 4 PPI interrupt source and 89 SPI interrupt sources input from different components
  - Support 16 software-triggered interrupts
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A35, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controllers for peripheral system
  - DMAC0 features,
    - 6 channels totally
    - 10 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register configure, designated as secure and non-secure
    - Support TrustZone technology and programmable secure state for each DMA channel

- DMAC1 features,
  - 8 channels totally
  - 20 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configure, designated as secure and non-secure
  - Support TrustZone technology and programmable secure state for each DMA channel

- Trust Execution Environment system
  - Support TrustZone technology for the following components
    - Cortex-A35, support security and non-security mode, switch by software
    - System general DMAC, support some dedicated channels work only in security mode
    - Secure OTP, only can be accessed by Cortex-A35 in secure mode and secure key reader block
    - Internal SRAM, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)
    - Firewall is embedded to manage the other master/slave function components
  - Cipher engine
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support DES & TDES cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support DES/TDES ECB/CBC/OFB/CFB mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC
  - Support data scrambling for DDR2/DDR3/DDR3L/LPDDR2
  - Support up to 256 bits TRNG Output
  - Support secure OTP
  - Support secure boot
  - Support secure debug
  - Support secure OS

1.2.6 Video Output Processor (VOP)

- Display Interface
  - Support parallel RGB LCD output interface
    - 18-bit(RGB666)
    - 16-bit(RGB565)
  - Support MCU interface
  - Max output resolution 1080p
- Display process
  - Background layer: programmable 24-bit color
  - Win0 layer
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - RB/alpha/mid/uv swap
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - RB/alpha/endian swap
    - Support virtual display

  - 256 level alpha blending (pre-multiplied alpha support)
  - Transparency color key
  - RGB2YCbCr(BT601/BT709)
- Others
  - Win0 layer and Win1 layer overlay exchangeable
  - BCSH(Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH:YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
  - BCSH:RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust for PAD
  - Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable) RGB888to666
  - Blank and black display
  - Standby mode
  - Support RB/RG/BG/delta/dummy swap

1.2.7 Audio Interface

- I2S with 2 channel
  - Support 2 I2S_2CH components
  - I2S_2CH_0 support master tx/rx mode and slave tx/rx mode
  - I2S_2CH_0 is connected to chip IO
  - I2S_2CH_1 support slave rx mode
  - I2S_2CH_1 is connected with audio codec inside chip
  - Support I2S normal, left and right justified mode serial audio data transfer
  - Support PCM early, late1, late2, late3 mode serial audio data transfer
  - Support resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Support DMA transfer
  - Support separate transmit and receive DMA request mode
  - Support 1 common SCLK signal for receiving and transmitting
  - Support 1 common LRCK signal for receiving and transmitting
  - Support 2 independent LRCK signals for receiving and transmitting
  - Support configurable SCLK and LRCK polarity

- I2S with 8 channel
  - Support 4 I2S_8CH components
  - I2S_8CH_0 support master tx/rx mode and slave tx/rx mode
  - I2S_8CH_1 support master tx/rx mode and slave tx/rx mode
  - I2S_8CH_0/1 are connected to chip IO
  - I2S_8CH_0 support max 8ch in and max 8ch out simultaneously
  - I2S_8CH_1 support tx plus rx max 10ch simultaneously
  - I2S_8CH_2 support master tx/rx mode and slave tx/rx mode
  - I2S_8CH_3 support slave rx mode, can only works as 4CH mode
  - I2S_8CH_2/3 are connected with audio codec inside chip
  - Support I2S normal, left and right justified mode serial audio data transfer
  - Support PCM early, late1, late2, late3 mode serial audio data transfer
  - Support resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Support DMA transfer
  - Support separate transmit and receive DMA request mode
  - Support 1 common SCLK signal for receiving and transmitting
  - Support 2 independent SCLK signals for receiving and transmitting
  - Support 1 common LRCK signal for receiving and transmitting
  - Support 2 independent LRCK signals for receiving and transmitting
  - Support configurable SCLK and LRCK polarity

- I2S with 16 channel
  - Support one I2S_16CH by gathering I2S_8CH_0 and I2S_8CH_1

- Support master tx/rx mode and slave tx/rx mode

- PDM with 8 channel
  - Support PDM master receive mode
  - Support 5 wire PDM interface with one is clock and 4 data line
  - Support up to 8 mono microphones or 4 stereo microphones
  - Support each data path is enabled or disabled independently
  - Support DMA handshaking interface and configurable DMA water level
  - Support 16~24 bit sample resolution
  - Support sample rate up to 192KHz
  - Support programmable data sampling sensibility, rising or falling edge

- TDM with 8 channel
  - Support 4 TDM_8CH, share same I2S_8CH controller accordingly
  - Support I2S normal, left and right justified mode serial audio data transfer
  - Support PCM normal, 1/2 cycle left shift , 1 cycle left shift, 3/2 cycle left shift, 2 cycle left shift mode serial audio data transfer
  - Support TDM programmable slot bit width: 16~32bits
  - Support TDM programmable frame width: 32~512bits
  - Support TDM programmable FSYNC width
  - Sample rate up to 192KHz@2CH and 48KHz@8CH
  - Support DMA transfer
  - Support separate transmit and receive DMA request mode
  - Support 1 common SCLK signal for receiving and transmitting
  - Support 2 independent SCLK signals for receiving and transmitting
  - Support 1 common LRCK signal for receiving and transmitting
  - Support 2 independent LRCK signals for receiving and transmitting
  - Support configurable SCLK and LRCK polarity

- SPDIF
  - Support SPDIF TX x 1
  - Support SPDIF RX x 1
  - Support HDMI ARC
  - Support 16bits/20bits/24bits resolution
  - Support DMA transfer
  - Support linear PCM mode (IEC-60958)
  - Support non-linear PCM transfer(IEC-61937)
  - Sample rate up to 192KHz
  - Support SPDIF RX is bypassed to SPDIF TX directly

- Voice Activity Detection(VAD)
  - Support single Mic human voice detection
  - Support human voice frequency band filtering
  - Support human voice amplitude detection
  - Support Muti-Mic array data buffer before voice detection event or after voice detection event two modes, and also can support Muti-Mic array data is not buffered in voice detection process
  - Support Mic data from Analog Mic, I2S Digital Mic or PDM digital Mic
  - Buffer memory is shared with system internal memory

- Embedded Audio Codec
  - 24 bit DAC which support stereo headphone out and line out
  - 24 bit ADC which support max 8 channel microphone input and 2 channel line in
  - Support differential microphone input and can also be configured as single-end
  - Support Po=18mW for 16ohm and 9mW for 32ohm headphone output
  - Support Automatic Level Control (ALC)
  - Support programmable input/output analog gains

- Support two programmable microphone bias. The max programmable voltage can reach to 0.85*AVDD3V3
- Support I2S as the digital signal interface for both ADC and DAC
- Support both master and slave mode
- Support 16bits/24bits resolution
- Support I2S normal, left and right justified mode
- Support sample rate,
  - Group1: 8khz,16khz,32kHz,64kHz,128khz
  - Group2: 11.025khz,22.05khz,44.1khz,88.2khz,176.4khz
  - Group3: 12khz,24khz,48khz,96khz,192khz
  - Support ADC/DAC sample rate any combination of group1/group2/group3
- Support headphone jack detection input

1.2.8 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4bits data bus widths

- MAC 10/100 Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Handles automatic retransmission of Collision frames for transmission

- USB 2.0
  - Built-in 2 USB 2.0 interfaces, one supports OTG
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- SPI interface
  - Support three SPI Controller(SPI0/SPI1/SPI2)
  - Support one chip-select for each SPI Controller
  - Support serial-master and serial-slave mode, software-configurable

- I2C interface
  - Support four I2C interface(I2C0/I2C1/I2C2/I2C3)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- UART Controller
  - Support five UART interface(UART0/UART1/UART2/UART3/UART4)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART0/UART1/UART4

1.2.9 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt to CPU
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt

- Temperature Sensor(TS-ADC)
  - Up to 50KS/s sampling rate
  - Support two temperature sensor
  - -20~120℃ temperature range and 5℃ temperature resolution

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 6 single-ended input channels

- OTP
  - Support 4K bit Size, 3.5K bit for secure application
  - Support Program/Read/Idle mode

- Package Type
  - TFBGA355 (body: 13mm x 13mm; ball size: 0.3mm; ball pitch: 0.65mm)

Notes:
DDR2/DDR3/DDR3L/LPDDR2 are not used simultaneously

1.3 Block Diagram

The following diagram shows the basic block diagram.

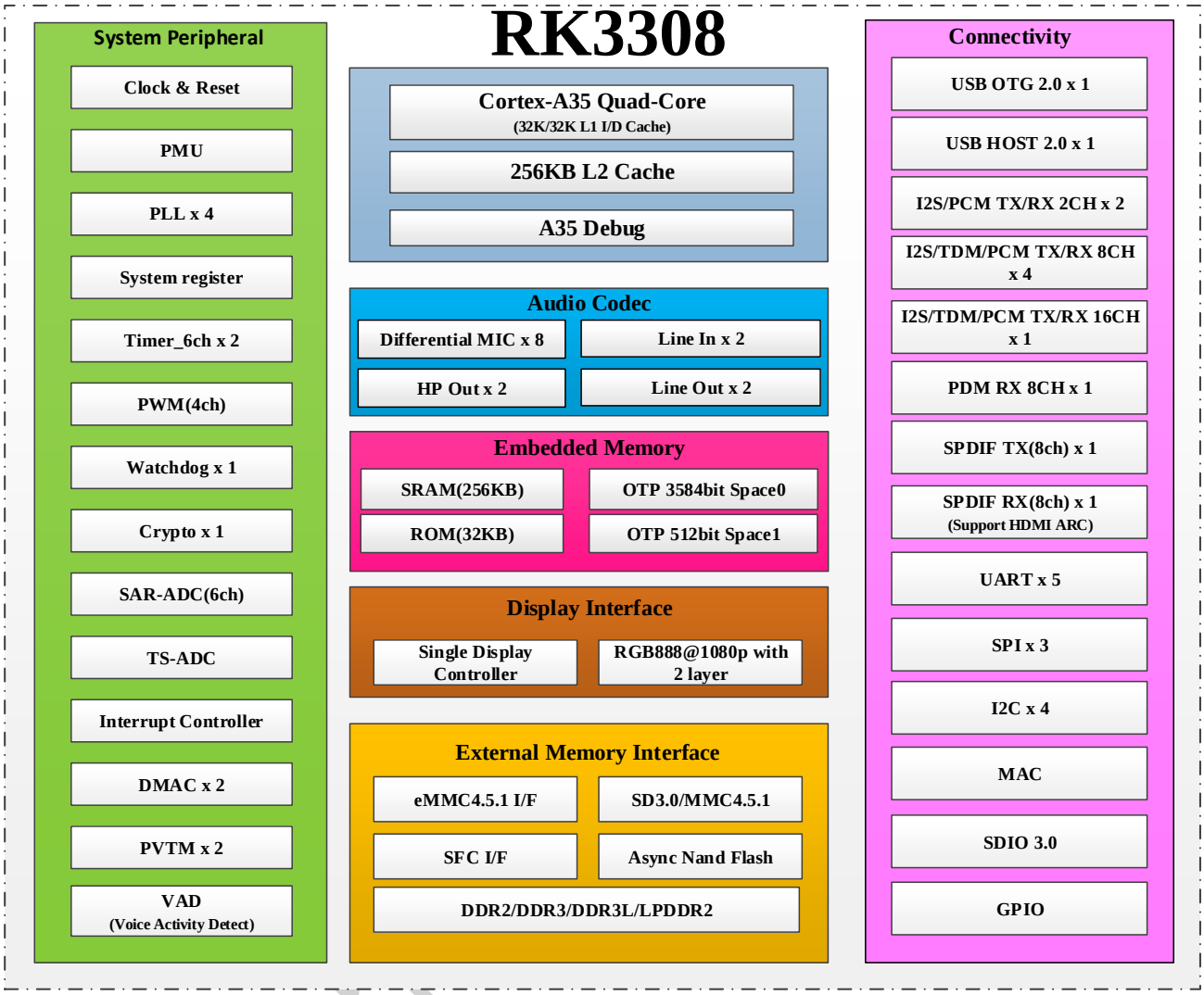


Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3308	RoHS	TFBGA355	TBD	Quad core application processor

2.2 Top Marking

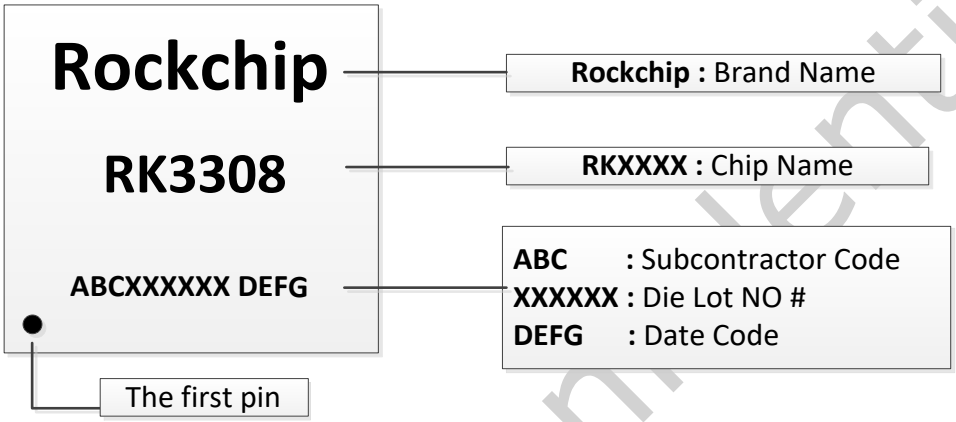


Fig.2-1 Package definition

2.3 TFBGA355 Dimension

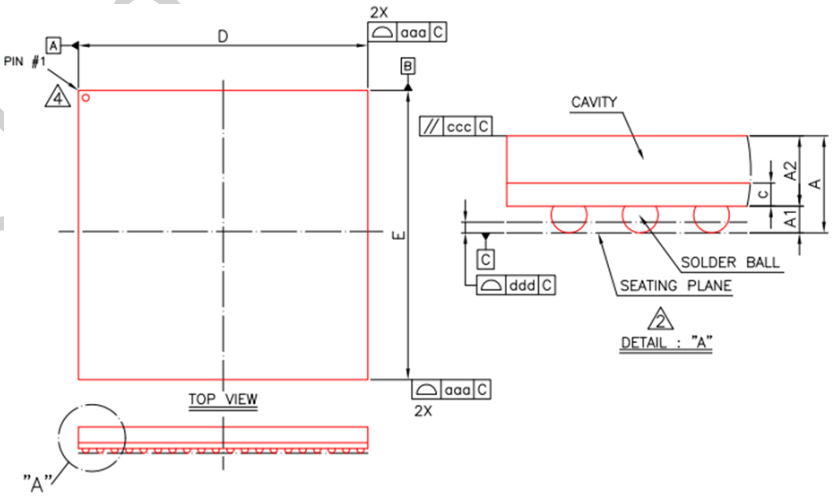


Fig.2-2 Package Top View and Side View

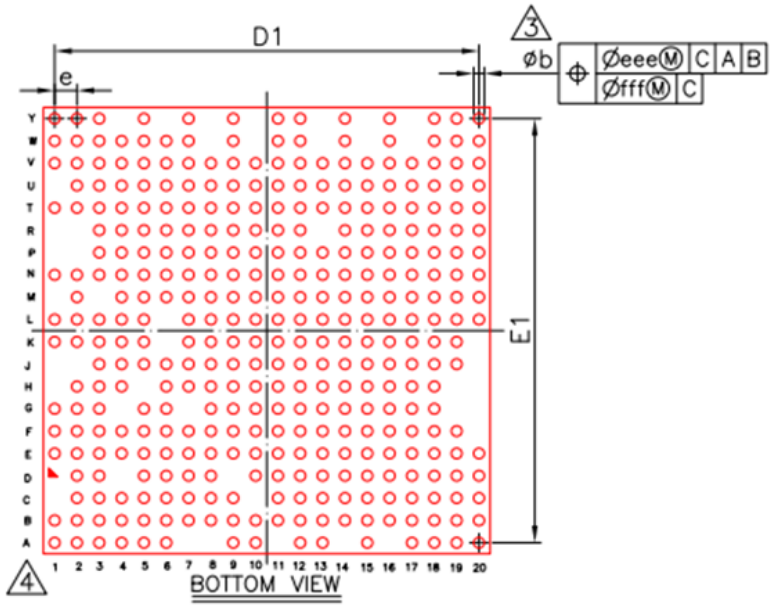


Fig.2-3 Package bottom view

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	12.90	13.00	13.10	0.508	0.512	0.516
E	12.90	13.00	13.10	0.508	0.512	0.516
D1	---	12.35	---	---	0.486	---
E1	---	12.35	---	---	0.486	---
e	---	0.65	---	---	0.026	---
b	0.26	0.31	0.36	0.010	0.012	0.014
aaa	0.15			0.006		
ccc	0.20			0.008		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	20 / 20					

Fig.2-4 Package dimension

Notes:
1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd
6. REFERANCE DOCUMENT: JEDEC PUBICATION 95 DESIGN GUIDE 4.5
7. PKG BALL DIAMETER IS 0.30+/-0.05 mm BEFORE REFLOW.

2.4 Ball Map

	1	2	3	4	5	6	7	8	9	10
A	VSS	DDR_A7	DDR_A2	VSS	DDR_A1	DDR_A6			VSS	DDR_A8
B	DDR_CS0N	DDR_BA0	DDR_A5	DDR_A0	DDR_A11	DDR_A12	DDR_A4	VSS	DDR_CKE	DDR_A14
C		DDR_CLKN	DDR_CLK	VSS	DDR_ODT0	VSS	VSS	DDR_BA1	DDR_A10	
D		VSS	DDR_DQ11		DDR_RASN	DDR_BA2	DDR_A13	DDR_CASN		FP_3
E	VSS	DDR_DQ4	DDR_DQ6	DDR_RESET	VSS	DDR_A3	DDR_A9	DDR_WEN	VSS	DDR_VDD
F	DDR_DQ5	VSS	DDR_DQ13	DDR_DQ8	FP_1	FP_2	DDR_VDD	DDR_VDD	DDR_VDD	LOGIC_VDD
G	DDR_DM0	DDR_DQ9	VSS		DDR_DQ1	DDR_VDD		VSS	VSS	LOGIC_VDD
H		DDR_DQS1	DDR_DQS1N	DDR_DQ2		DDR_VDD	VSS	VSS	VSS	VSS
J			DDR_DQS0	DDR_DQ0	VSS	DDR_VDD	VSS	VSS	VSS	VSS
K	VSS	DDR_DQ7	VSS	DDR_DQS0N	DDR_DQ15		VSS	VSS	VSS	VSS

Fig.2-5 Ball Map-1

	1	2	3	4	5	6	7	8	9	10
L	DDR_DQ3	DDR_DQ12	DDR_DM1	DDR_DQ10	VSS		VSS	VSS	VSS	VSS
M		DDR_DQ14		VSS	VSS	VSS	VSS	VSS	VSS	VSS
N	VSS	GPIO0_C5/OTG_DRVBUS	GPIO0_A0/SDIO_INT	GPIO0_A1/SDIO_WRPT	APIO0_VDD	CORE_VDD	CORE_VDD	CORE_VDD	VSS	VSS
P			GPIO0_A2/SDIO_PWR	GPIO0_A3/SDMMC_DET	CORE_VDD	CORE_VDD	CORE_VDD	VSS	VSS	VSS
R			GPIO0_A4/TEST_CLK	GPIO0_A5	CORE_VDD	CORE_VDD	VSS	CORE_VDD	GPIO1_C4/LCDC_D16/I2S1_SDO3_SDI1_M1/PDM_SDI1_M1/MAC_	GPIO3_B3/FLASH_ALE/EMMC_PWREN/SPI1_
T	GPIO0_C1/SPDIF_TX	GPIO0_C4	GPIO0_B0	GPIO0_A7	GPIO0_A6	GPIO1_B2/LCDC_D6/I2S1_SDO3_SDI1_M0/PDM_SDI	VSS	GPIO1_B5/LCDC_D9/I2S1_SCLK_TX_M1/MAC_MDC	GPIO1_C7/UART1_RTSN/UART2_TX_M0/SPI2_MOSI/JTAG_TMS	GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0
U		GPIO0_C0/PWM3/I2C3_SCL_	GPIO0_B2/TSADC_SH	GPIO1_A2/LCDC_VSYNC/I2S1_MCLK	GPIO1_A6/LCDC_D2/I2S1_LRCK_RX_M0	GPIO1_B1/LCDC_D5/I2S1_SDO2_SDI2_M0/PDM_SDI	GPIO1_B3/LCDC_D7/I2S1_SDI0_M0/PDM_SDI0_M0	GPIO1_C2/LCDC_D14/I2S1_SDO1_SDI3_M1/PDM_SDI3_M1/MAC_	GPIO1_C3/LCDC_D15/I2S1_SDO2_SDI2_M1/PDM_SDI2_M1/MAC_	GPIO3_A6/FLASH_D6/EMMC_D6
V	GPIO0_B4/I2C1_SCL	GPIO0_B3/I2C1_SDA	GPIO0_B5/PWM0	GPIO1_A1/LCDC_HSYNC	GPIO1_A5/LCDC_D1/I2S1_LRCK_TX_M0	GPIO1_B0/LCDC_D4/I2S1_SDO1_SDI3_M0/PDM_SDI	GPIO1_B4/LCDC_D8/I2S1_MCLK_M1/MAC_CLK	GPIO1_C1/LCDC_D13/I2S1_SDO0_M1/MAC_TXEN	GPIO1_C0/LCDC_D12/I2S1_LRCK_RX_M1/MAC_RXDV	GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK
W	GPIO0_B7/PWM2/I2C3_SDA	GPIO0_B6/PWM1	GPIO0_C2/SPDIF_RX	GPIO1_A3/LCDC_DEN/I2S1_SCLK_T	GPIO1_A4/LCDC_D0/I2S1_SCLK_RX_M0/PDM_CL	GPIO1_A7/LCDC_D3/I2S1_SDO0_M0	GPIO1_B6/LCDC_D10/I2S1_SCLK_RX_M1/PDM_CLK_M1/MAC_		GPIO1_C6/UART1_CTSN/UART2_RX_M0/SPI2_MISO/JTAG_TCK	
Y	VSS	GPIO0_C3/RTC_CLK	GPIO0_B1/PMIC_SLE		GPIO1_A0/LCDC_DCLK		GPIO1_B7/LCDC_D11/I2S1_LRCK_TX_M1/MAC_RXER		GPIO1_C5/LCDC_D17/I2S1_SDI0_M1/PDM_SDI0_M1/MAC_RXD1	

Fig.2-6 Ball Map-2

11	12	13	14	15	16	17	18	19	20	
	USB1_DM	USB0_DM		GPIO4_D3/ SDMMC_D3 /UART2_TX _M1		GPIO4_D1/ SDMMC_D1	ADC_IN3	ADC_IN0	VSS	A
VSS	USB1_DP	USB0_DP	GPIO4_D6/ SDMMC_PW REN	GPIO4_D2/ SDMMC_D2 /UART2_RX _M1	GPIO4_D5/ SDMMC_CL K	GPIO4_D0/ SDMMC_D0	ADC_IN4	ADC_IN1	NPOR	B
VSS	USB_ID	VSS	USB_VBUS	USB_EXTR	GPIO4_D4/ SDMMC_CM D	VSS	ADC_IN2	NPOR_BYPA SS	REF_CLKOU T	C
VSS	VSS	USB_AVDD _3V3	APIO5_VDD	USB_VDD_1 V0	USB_AVDD _1V8	SADC_AVD D_1V8	ADC_IN5	TVSS	VSS	D
VSS	VSS	VSS	NPOR_AVD D_3V3	PLL_AVDD_ 1V0	OTP_VCC_1 V8	PLL_AVDD_ 1V8	VSS	XIN_24M	XOUT_24M	E
LOGIC_VDD	LOGIC_VDD	VSS	VSS	VSS	VSS	GPIO4_B0/ UART4_RX	GPIO4_B5/I 2S0_2CH_S CLK	GPIO4_B3		F
LOGIC_VDD	LOGIC_VDD	VSS	VSS	PLL_VSS	GPIO4_B2	GPIO4_A3/ SDIO_D3	GPIO4_A2/ SDIO_D2			G
VSS	VSS	VSS	GPIO4_C0/I 2S0_2CH_S DI	GPIO4_B7/I 2S0_2CH_S DO	GPIO4_B4/I 2S0_2CH_M CLK	VSS	GPIO4_A4/ SDIO_CMD			H
VSS	VSS	VSS	APIO4_VDD	GPIO4_B6/I 2S0_2CH_L RCK_TX	GPIO4_B1/ UART4_TX	GPIO4_A1/ SDIO_D1	GPIO4_A5/ SDIO_CLK	GPIO4_A0/ SDIO_D0		J
VSS	VSS	VSS	VSS	VSS	VSS	VSS	GPIO4_A7/ UART4_RTS N	GPIO4_A6/ UART4_CTS N		K

Fig.2-7 Ball Map-3

VSS	VSS	VSS	VSS	VSS	VSS	CODEC_AVSS	CODEC_AVSS	CODEC_AVSS	CODEC_AVSS	L
VSS	VSS	VSS	VSS	VSS	CODEC_AVSS	CODEC_AVDD_1V8	CODEC_MICN6	CODEC_MICN8	CODEC_MICP8	M
VSS	VSS	VSS	VSS	VSS	CODEC_AVSS	CODEC_AVDD_1V8	CODEC_MICP6	CODEC_MICN7	CODEC_MICP7	N
VSS	VSS	VSS	VSS	VSS	CODEC_AVDD_3V3	CODEC_MICN3	CODEC_MICP3	CODEC_MICN5	CODEC_MICP5	P
APIO1_VDD	APIO3_VDD		VSS	GPIO2_A5/I2S0_SCLK_TX	GPIO2_B0/I2S0_LRCK_RX	CODEC_AVSS	CODEC_VCM	CODEC_MICN4	CODEC_MICP4	R
APIO2_VDD	GPIO3_B5/FLASH_CSN0/I2C3_SCL_M1/SPI1_CSN0/UART3_T	GPIO3_B1/FLASH_CLE/EMMC_CLK	GPIO2_B5/I2S0_SDI0/PDM_SDI0_M2	GPIO2_A4/I2S0_MCLK/PDM_CLK_M_M2	GPIO2_A6/I2S0_SCLK_RX/PDM_CLK_S_M2	GPIO2_B4/I2S0_SDO3	CODEC_VCMH	CODEC_LINE2	CODEC_LINE1	T
GPIO3_A0/FLASH_D0/EMMC_D0/SFC_SIO0	GPIO3_A7/FLASH_D7/EMMC_D7	GPIO3_B2/FLASH_RDN/SPI1_MISO	GPIO2_A0/UART0_RX/SPI0_MISO	GPIO2_B6/I2S0_SDI1/PDM_SDI1_M2	GPIO2_B3/I2S0_SDO2	VSS	CODEC_MICBIAS2	CODEC_MICN2	CODEC_MICP2	U
GPIO3_A5/FLASH_D5/EMMC_D5/SFC_CSN0	GPIO3_A1/FLASH_D1/EMMC_D1/SFC_SIO1	GPIO3_B0/FLASH_WRN/EMMC_CMD	GPIO2_B1/I2S0_SDO0	GPIO2_B2/I2S0_SDO1	GPIO2_A1/UART0_TX/SPI0_MOSI	GPIO2_A7/I2S0_LRCK_TX	CODEC_HPDET	CODEC_MICN1	CODEC_MICP1	V
GPIO3_A4/FLASH_D4/EMMC_D4/SFC_CLK	GPIO3_B4/FLASH_RDY/I2C3_SDA_M1/SPI1_MOSI/UART3_RX		GPIO2_B7/I2S0_SDI2/PDM_SDI2_M2		GPIO2_A3/UART0_RTSN/SPI0_CSN0/I2C2_SCL		CODEC_HPOUT_R	CODEC_LINEOUT_R	CODEC_LINEOUT_L	W
GPIO3_A3/FLASH_D3/EMMC_D3/SFC_HOLD_SIO3	GPIO3_A2/FLASH_D2/EMMC_D2/SFC_WP_SIO2		GPIO2_C0/I2S0_SDI3/PDM_SDI3_M2		GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA		CODEC_MICBIAS1	CODEC_HPOUT_L	CODEC_AVSS	Y
11	12	13	14	15	16	17	18	19	20	

Fig.2-8 Ball Map-4

2.5 Pin Number List

Table 2-1 Pin Number List Information

No.	Pin Name	No.	Pin Name
A1	VSS	L2	DDR_DQ12
A2	DDR_A7	L3	DDR_DM1
A3	DDR_A2	L4	DDR_DQ10
A4	VSS	L5	VSS
A5	DDR_A1	L7	VSS
A6	DDR_A6	L8	VSS
A9	VSS	L9	VSS
A10	DDR_A8	L10	VSS
A12	USB1_DM	L11	VSS
A13	USB0_DM	L12	VSS
A15	GPIO4_D3/SDMMC_D3/UART2_TX_M1	L13	VSS
A17	GPIO4_D1/SDMMC_D1	L14	VSS
A18	ADC_IN3	L15	VSS
A19	ADC_IN0	L16	VSS
A20	VSS	L17	CODEC_AVSS
B1	DDR_CS0N	L18	CODEC_AVSS
B2	DDR_BA0	L19	CODEC_AVSS
B3	DDR_A5	L20	CODEC_AVSS
B4	DDR_A0	M2	DDR_DQ14
B5	DDR_A11	M4	VSS
B6	DDR_A12	M5	VSS
B7	DDR_A4	M6	VSS
B8	VSS	M7	VSS
B9	DDR_CKE	M8	VSS
B10	DDR_A14	M9	VSS
B11	VSS	M10	VSS
B12	USB1_DP	M11	VSS
B13	USB0_DP	M12	VSS
B14	GPIO4_D6/SDMMC_PWREN	M13	VSS
B15	GPIO4_D2/SDMMC_D2/UART2_RX_M1	M14	VSS
B16	GPIO4_D5/SDMMC_CLK	M15	VSS
B17	GPIO4_D0/SDMMC_D0	M16	CODEC_AVSS
B18	ADC_IN4	M17	CODEC_AVDD_1V8
B19	ADC_IN1	M18	CODEC_MICN6
B20	NPOR	M19	CODEC_MICN8
C2	DDR_CLKN	M20	CODEC_MICP8
C3	DDR_CLK	N1	VSS
C4	VSS	N2	GPIO0_C5/OTG_DRVBUS
C5	DDR_ODT0	N3	GPIO0_A0/SDIO_INTN
C6	VSS	N4	GPIO0_A1/SDIO_WRPT
C7	VSS	N5	APIO0_VDD

No.	Pin Name	No.	Pin Name
C8	DDR_BA1	N6	CORE_VDD
C9	DDR_A10	N7	CORE_VDD
C11	VSS	N8	CORE_VDD
C12	USB_ID	N9	VSS
C13	VSS	N10	VSS
C14	USB_VBUS	N11	VSS
C15	USB_EXTR	N12	VSS
C16	GPIO4_D4/SDMMC_CMD	N13	VSS
C17	VSS	N14	VSS
C18	ADC_IN2	N15	VSS
C19	NPOR_BYPASS	N16	CODEC_AVSS
C20	REF_CLKOUT	N17	CODEC_AVDD_1V8
D2	VSS	N18	CODEC_MICP6
D3	DDR_DQ11	N19	CODEC_MICN7
D5	DDR_RASN	N20	CODEC_MICP7
D6	DDR_BA2	P3	GPIO0_A2/SDIO_PWREN
D7	DDR_A13	P4	GPIO0_A3/SDMMC_DET
D8	DDR_CASN	P5	CORE_VDD
D10	FP_3	P6	CORE_VDD
D11	VSS	P7	CORE_VDD
D12	VSS	P8	VSS
D13	USB_AVDD_3V3	P9	VSS
D14	APIO5_VDD	P10	VSS
D15	USB_VDD_1V0	P11	VSS
D16	USB_AVDD_1V8	P12	VSS
D17	SADC_AVDD_1V8	P13	VSS
D18	ADC_IN5	P14	VSS
D19	TVSS	P15	VSS
D20	VSS	P16	CODEC_AVDD_3V3
E1	VSS	P17	CODEC_MICN3
E2	DDR_DQ4	P18	CODEC_MICP3
E3	DDR_DQ6	P19	CODEC_MICN5
E4	DDR_RESET	P20	CODEC_MICP5
E5	VSS	R3	GPIO0_A4/TEST_CLKOUT
E6	DDR_A3	R4	GPIO0_A5
E7	DDR_A9	R5	CORE_VDD
E8	DDR_WEN	R6	CORE_VDD
E9	VSS	R7	VSS
E10	DDR_VDD	R8	CORE_VDD
E11	VSS	R9	GPIO1_C4/LCDC_D16/I2S1_SDO3_SDI1_M1/PDM_SDI1_M1/MAC_RXD0
E12	VSS	R10	GPIO3_B3/FLASH_ALE/EMMC_PWREN/SPI1_CLK
E13	VSS	R11	APIO1_VDD
E14	NPOR_AVDD_3V3	R12	APIO3_VDD
E15	PLL_AVDD_1V0	R14	VSS

No.	Pin Name	No.	Pin Name
E16	OTP_VCC_1V8	R15	GPIO2_A5/I2S0_SCLK_TX
E17	PLL_AVDD_1V8	R16	GPIO2_B0/I2S0_LRCK_RX
E18	VSS	R17	CODEC_AVSS
E19	XIN_24M	R18	CODEC_VCM
E20	XOUT_24M	R19	CODEC_MICN4
F1	DDR_DQ5	R20	CODEC_MICP4
F2	VSS	T1	GPIO0_C1/SPDIF_TX
F3	DDR_DQ13	T2	GPIO0_C4
F4	DDR_DQ8	T3	GPIO0_B0
F5	FP_1	T4	GPIO0_A7
F6	FP_2	T5	GPIO0_A6
F7	DDR_VDD	T6	GPIO1_B2/LCDC_D6/I2S1_SDO3_SDI1_M0/PDM_SDI1_M0
F8	DDR_VDD	T7	VSS
F9	DDR_VDD	T8	GPIO1_B5/LCDC_D9/I2S1_SCLK_TX_M1/MAC_MDC
F10	LOGIC_VDD	T9	GPIO1_C7/UART1_RTSN/UART2_TX_M0/SPI2_MOSI/JTAG_TMS
F11	LOGIC_VDD	T10	GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0
F12	LOGIC_VDD	T11	APIO2_VDD
F13	VSS	T12	GPIO3_B5/FLASH_CSN0/I2C3_SCL_M1/SPI1_CSN0/UART3_TX
F14	VSS	T13	GPIO3_B1/FLASH_CLE/EMMC_CLK
F15	VSS	T14	GPIO2_B5/I2S0_SDI0/PDM_SDI0_M2
F16	VSS	T15	GPIO2_A4/I2S0_MCLK/PDM_CLK_M_M2
F17	GPIO4_B0/UART4_RX	T16	GPIO2_A6/I2S0_SCLK_RX/PDM_CLK_S_M2
F18	GPIO4_B5/I2S0_2CH_SCLK	T17	GPIO2_B4/I2S0_SDO3
F19	GPIO4_B3	T18	CODEC_VCMH
G1	DDR_DM0	T19	CODEC_LINE2
G2	DDR_DQ9	T20	CODEC_LINE1
G3	VSS	U2	GPIO0_C0/PWM3/I2C3_SCL_M0
G5	DDR_DQ1	U3	GPIO0_B2/TSADC_SHUT
G6	DDR_VDD	U4	GPIO1_A2/LCDC_VSYNC/I2S1_MCLK_M0
G8	VSS	U5	GPIO1_A6/LCDC_D2/I2S1_LRCK_RX_M0
G9	VSS	U6	GPIO1_B1/LCDC_D5/I2S1_SDO2_SDI2_M0/PDM_SDI2_M0
G10	LOGIC_VDD	U7	GPIO1_B3/LCDC_D7/I2S1_SDI0_M0/PDM_SDI0_M0
G11	LOGIC_VDD	U8	GPIO1_C2/LCDC_D14/I2S1_SDO1_SDI3_M1/PDM_SDI3_M1/MAC_TXD0
G12	LOGIC_VDD	U9	GPIO1_C3/LCDC_D15/I2S1_SDO2_SDI2_M1/PDM_SDI2_M1/MAC_TXD1
G13	VSS	U10	GPIO3_A6/FLASH_D6/EMMC_D6
G14	VSS	U11	GPIO3_A0/FLASH_D0/EMMC_D0/SFC_SIO0
G15	PLL_VSS	U12	GPIO3_A7/FLASH_D7/EMMC_D7
G16	GPIO4_B2	U13	GPIO3_B2/FLASH_RDN/SPI1_MISO
G17	GPIO4_A3/SDIO_D3	U14	GPIO2_A0/UART0_RX/SPI0_MISO
G18	GPIO4_A2/SDIO_D2	U15	GPIO2_B6/I2S0_SDI1/PDM_SDI1_M2
H2	DDR_DQS1	U16	GPIO2_B3/I2S0_SDO2
H3	DDR_DQS1N	U17	VSS
H4	DDR_DQ2	U18	CODEC_MICBIAS2
H6	DDR_VDD	U19	CODEC_MICN2

No.	Pin Name	No.	Pin Name
H7	VSS	U20	CODEC_MICP2
H8	VSS	V1	GPIO0_B4/I2C1_SCL
H9	VSS	V2	GPIO0_B3/I2C1_SDA
H10	VSS	V3	GPIO0_B5/PWM0
H11	VSS	V4	GPIO1_A1/LCDC_HSYNC
H12	VSS	V5	GPIO1_A5/LCDC_D1/I2S1_LRCK_TX_M0
H13	VSS	V6	GPIO1_B0/LCDC_D4/I2S1_SDO1_SDI3_M0/PDM_SDI3_M0
H14	GPIO4_C0/I2S0_2CH_SDI	V7	GPIO1_B4/LCDC_D8/I2S1_MCLK_M1/MAC_CLK
H15	GPIO4_B7/I2S0_2CH_SDO	V8	GPIO1_C1/LCDC_D13/I2S1_SDO0_M1/MAC_TXEN
H16	GPIO4_B4/I2S0_2CH_MCLK	V9	GPIO1_C0/LCDC_D12/I2S1_LRCK_RX_M1/MAC_RXDV
H17	VSS	V10	GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK
H18	GPIO4_A4/SDIO_CMD	V11	GPIO3_A5/FLASH_D5/EMMC_D5/SFC_CSN0
J3	DDR_DQS0	V12	GPIO3_A1/FLASH_D1/EMMC_D1/SFC_SIO1
J4	DDR_DQ0	V13	GPIO3_B0/FLASH_WRN/EMMC_CMD
J5	VSS	V14	GPIO2_B1/I2S0_SDO0
J6	DDR_VDD	V15	GPIO2_B2/I2S0_SDO1
J7	VSS	V16	GPIO2_A1/UART0_TX/SPI0_MOSI
J8	VSS	V17	GPIO2_A7/I2S0_LRCK_TX
J9	VSS	V18	CODEC_HPDET
J10	VSS	V19	CODEC_MICN1
J11	VSS	V20	CODEC_MICP1
J12	VSS	W1	GPIO0_B7/PWM2/I2C3_SDA_M0
J13	VSS	W2	GPIO0_B6/PWM1
J14	APIO4_VDD	W3	GPIO0_C2/SPDIF_RX
J15	GPIO4_B6/I2S0_2CH_LRCK_TX	W4	GPIO1_A3/LCDC_DEN/I2S1_SCLK_TX_M0
J16	GPIO4_B1/UART4_TX	W5	GPIO1_A4/LCDC_D0/I2S1_SCLK_RX_M0/PDM_CLK_M0
J17	GPIO4_A1/SDIO_D1	W6	GPIO1_A7/LCDC_D3/I2S1_SDO0_M0
J18	GPIO4_A5/SDIO_CLK	W7	GPIO1_B6/LCDC_D10/I2S1_SCLK_RX_M1/PDM_CLK_M1/MAC_MDIO
J19	GPIO4_A0/SDIO_D0	W9	GPIO1_C6/UART1_CTSN/UART2_RX_M0/SPI2_MISO/JTAG_TCK
K1	VSS	W11	GPIO3_A4/FLASH_D4/EMMC_D4/SFC_CLK
K2	DDR_DQ7	W12	GPIO3_B4/FLASH_RDY/I2C3_SDA_M1/SPI1_MOSI/UART3_RX
K3	VSS	W14	GPIO2_B7/I2S0_SDI2/PDM_SDI2_M2
K4	DDR_DQS0N	W16	GPIO2_A3/UART0_RTSN/SPI0_CSN0/I2C2_SCL
K5	DDR_DQ15	W18	CODEC_HPOUT_R
K7	VSS	W19	CODEC_LINEOUT_R
K8	VSS	W20	CODEC_LINEOUT_L
K9	VSS	Y1	VSS
K10	VSS	Y2	GPIO0_C3/RTC_CLK
K11	VSS	Y3	GPIO0_B1/PMIC_SLEEP
K12	VSS	Y5	GPIO1_A0/LCDC_DCLK
K13	VSS	Y7	GPIO1_B7/LCDC_D11/I2S1_LRCK_TX_M1/MAC_RXER
K14	VSS	Y9	GPIO1_C5/LCDC_D17/I2S1_SDI0_M1/PDM_SDI0_M1/MAC_RXD1
K15	VSS	Y11	GPIO3_A3/FLASH_D3/EMMC_D3/SFC_HOLD_SIO3
K16	VSS	Y12	GPIO3_A2/FLASH_D2/EMMC_D2/SFC_WP_SIO2

No.	Pin Name	No.	Pin Name
K17	VSS	Y14	GPIO2_C0/I2S0_SDI3/PDM_SDI3_M2
K18	GPIO4_A7/UART4_RTSN	Y16	GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA
K19	GPIO4_A6/UART4_CTSN	Y18	CODEC_MICBIAS1
L1	DDR_DQ3	Y19	CODEC_HPOUT_L
Y20	CODEC_AVSS		

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	L1,L4,L9,L20, M8,M11, N4,N6,N7,N11,N13,N17, P2,P11,P12,P20, R1,R5,R9,R11,R12,R13,R18, T2,T13,T14,T15,T16, U3,U8,UI9,U13,U14, V7,V8,V9,V10,V11,V12,V13,V17, W5,W7,W8,W9,W10,W11,W12,W13, Y1,Y3,Y7,Y8,Y9,Y10,Y11,Y12,Y13,Y14,Y15,Y16,Y17	Digital Ground
CODEC_AVSS	L17,L18,L19,L20, M16, N16, R17, Y20	Audio Codec Analog Ground
PLL_VSS	G15	PLL Ground
CORE_VDD	N6,N7,N8, P5,P6,P7, R5,R6,R8	ARM Core Power
LOGIC_VDD	F10,F11,F12, G10,G11,G12	Logic Power
APIO0_VDD	N5	VCCIO0 Power Domain Power
APIO1_VDD	R11	VCCIO1 Power Domain Power
APIO2_VDD	T11	VCCIO2 Power Domain Power
APIO3_VDD	R12	VCCIO3 Power Domain Power
APIO4_VDD	J14	VCCIO4 Power Domain Power
APIO5_VDD	D14	VCCIO5 Power Domain Power
DDR_VDD	E10, F7,F8,F9, G6, H6, J6	DDR PHY Power

Group	Ball#	Descriptions
PLL_AVDD_1V0	E15	PLL Power
PLL_AVDD_1V8	E17	PLL Power
USB_VDD_1V0	D15	USB OTG2.0/Host2.0 PHY Power
USB_AVDD_1V8	D16	USB OTG2.0/Host2.0 PHY Power
USB_AVDD_3V3	D13	USB OTG2.0/Host2.0 PHY Power
CODEC_AVDD_1V8	M17, N17	Audio Codec Analog Power
CODEC_AVDD_3V3	P16	Audio Codec Analog Power
NPOR_AVDD_3V3	E14	NPOR Analog Power
SADC_AVDD_1V8	D17	SARADC Analog Power
OTP_VCC_1V8	E16	OTP Analog Power

2.7 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
E19	XIN_24M	XIN_24M					I	I	N/A	N/A		PLL_AVDD_1V8
E20	XOUT_24M	XOUT_24M					O	O	N/A	N/A		
B20	NPOR	NPOR					I	I	up	N/A		
D19	TVSS	TVSS					I	I	down	N/A		
C19	NPOR_BYPASS	NPOR_BYPASS					I/O	I	down	2mA		
C20	REF_CLKOUT	REF_CLKOUT					I/O	I	down	2mA		
N3	GPIO0_A0/SDIO_INTN	GPIO0_A0	SDIO_INTN				I/O	I	down	2mA	√	APIO0_VDD
N4	GPIO0_A1/SDIO_WRPT	GPIO0_A1	SDIO_WRPT				I/O	I	down	2mA	√	
P3	GPIO0_A2/SDIO_PWREN	GPIO0_A2	SDIO_PWREN				I/O	I	down	2mA	√	
P4	GPIO0_A3/SDMMC_DET	GPIO0_A3	SDMMC_DET				I/O	I	up	2mA	√	
R3	GPIO0_A4/TEST_CLKOUT	GPIO0_A4	TEST_CLKOUT				I/O	I	up	2mA	√	
R4	GPIO0_A5	GPIO0_A5					I/O	I	down	2mA	√	
T5	GPIO0_A6	GPIO0_A6					I/O	I	down	2mA	√	
T4	GPIO0_A7	GPIO0_A7					I/O	I	down	2mA	√	
T3	GPIO0_B0	GPIO0_B0					I/O	I	down	2mA	√	
Y3	GPIO0_B1/PMIC_SLEEP	GPIO0_B1	PMIC_SLEEP				I/O	I	down	2mA	√	
U3	GPIO0_B2/TSADC_SHUT	GPIO0_B2	TSADC_SHUT				I/O	I	down	2mA	√	
V2	GPIO0_B3/I2C1_SDA	GPIO0_B3	I2C1_SDA				I/O	I	up	2mA	√	
V1	GPIO0_B4/I2C1_SCL	GPIO0_B4	I2C1_SCL				I/O	I	up	2mA	√	
V3	GPIO0_B5/PWM0	GPIO0_B5	PWM0				I/O	I	down	2mA	√	
W2	GPIO0_B6/PWM1	GPIO0_B6	PWM1				I/O	I	down	2mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
W1	GPIO0_B7/PWM2/I2C3_SDA_M0	GPIO0_B7	PWM2	I2C3_SDA_M0			I/O	I	down	2mA	√	
U2	GPIO0_C0/PWM3/I2C3_SCL_M0	GPIO0_C0	PWM3	I2C3_SCL_M0			I/O	I	down	2mA	√	
T1	GPIO0_C1/SPDIF_TX	GPIO0_C1	SPDIF_TX				I/O	I	down	2mA	√	
W3	GPIO0_C2/SPDIF_RX	GPIO0_C2	SPDIF_RX				I/O	I	down	2mA	√	
Y2	GPIO0_C3/RTC_CLK	GPIO0_C3	RTC_CLK				I/O	I	high-z	2mA	√	
T2	GPIO0_C4	GPIO0_C4					I/O	I	down	2mA	√	
N2	GPIO0_C5/OTG_DRVBUS	GPIO0_C5	OTG_DRVBUS				I/O	I	down	2mA	√	
Y5	GPIO1_A0/LCDC_DCLK	GPIO1_A0	LCDC_DCLK				I/O	I	down	2mA	√	APIO1_VDD
V4	GPIO1_A1/LCDC_HSYNC	GPIO1_A1	LCDC_HSYNC				I/O	I	down	2mA	√	
U4	GPIO1_A2/LCDC_VSYNC/I2S1_MCLK_M0	GPIO1_A2	LCDC_VSYNC	I2S1_8CH_MCLK_M0			I/O	I	down	2mA	√	
W4	GPIO1_A3/LCDC_DEN/I2S1_SCLK_TX_M0	GPIO1_A3	LCDC_DEN	I2S1_8CH_SCLK_TX_M0			I/O	I	down	2mA	√	
W5	GPIO1_A4/LCDC_D0/I2S1_SCLK_RX_M0/PDM_CLK_M0	GPIO1_A4	LCDC_D0	I2S1_8CH_SCLK_RX_M0	PDM_CLK_M0		I/O	I	down	2mA	√	
V5	GPIO1_A5/LCDC_D1/I2S1_LRCK_TX_M0	GPIO1_A5	LCDC_D1	I2S1_8CH_LRCK_TX_M0			I/O	I	down	2mA	√	
U5	GPIO1_A6/LCDC_D2/I2S1_LRCK_RX_M0	GPIO1_A6	LCDC_D2	I2S1_8CH_LRCK_RX_M0			I/O	I	down	2mA	√	
W6	GPIO1_A7/LCDC_D3/I2S1_SDO0_M0	GPIO1_A7	LCDC_D3	I2S1_8CH_SDO0_M0			I/O	I	down	2mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
V6	GPIO1_B0/LCDC_D4/I2S1_SDO1_SDI3_M0/PDM_SDI3_M0	GPIO1_B0	LCDC_D4	I2S1_8CH_SDO1_SDI3_M0	PDM_SDI3_M0		I/O	I	down	2mA	√	
U6	GPIO1_B1/LCDC_D5/I2S1_SDO2_SDI2_M0/PDM_SDI2_M0	GPIO1_B1	LCDC_D5	I2S1_8CH_SDO2_SDI2_M0	PDM_SDI2_M0		I/O	I	down	2mA	√	
T6	GPIO1_B2/LCDC_D6/I2S1_SDO3_SDI1_M0/PDM_SDI1_M0	GPIO1_B2	LCDC_D6	I2S1_8CH_SDO3_SDI1_M0	PDM_SDI1_M0		I/O	I	down	2mA	√	
U7	GPIO1_B3/LCDC_D7/I2S1_SDI0_M0/PDM_SDI0_M0	GPIO1_B3	LCDC_D7	I2S1_8CH_SDI0_M0	PDM_SDI0_M0		I/O	I	down	2mA	√	
V7	GPIO1_B4/LCDC_D8/I2S1_MCLK_M1/MAC_CLK	GPIO1_B4	LCDC_D8	I2S1_8CH_MCLK_M1	MAC_CLK		I/O	I	down	2mA	√	
T8	GPIO1_B5/LCDC_D9/I2S1_SCLK_TX_M1/MAC_MDC	GPIO1_B5	LCDC_D9	I2S1_8CH_SCLK_TX_M1	MAC_MDC		I/O	I	down	2mA	√	
W7	GPIO1_B6/LCDC_D10/I2S1_SCLK_RX_M1/PDM_CLK_M1/MAC_MDIO	GPIO1_B6	LCDC_D10	I2S1_8CH_SCLK_RX_M1	PDM_CLK_M1	MAC_MDIO	I/O	I	down	2mA	√	
Y7	GPIO1_B7/LCDC_D11/I2S1_LRCK_TX_M1/MAC_RXER	GPIO1_B7	LCDC_D11	I2S1_8CH_LRCK_TX_M1	MAC_RXER		I/O	I	down	2mA	√	
V9	GPIO1_C0/LCDC_D12/I2S1_LRCK_RX_M1/MAC_RXDV	GPIO1_C0	LCDC_D12	I2S1_8CH_LRCK_RX_M1	MAC_RXDV		I/O	I	down	2mA	√	
V8	GPIO1_C1/LCDC_D13/I2S1_SDO0_M1/MAC_TXEN	GPIO1_C1	LCDC_D13	I2S1_8CH_SDO0_M1	MAC_TXEN		I/O	I	down	2mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
U8	GPIO1_C2/LCDC_D14/I2S1_SDO1_SDI3_M1/PDM_SDI3_M1/MAC_TXD0	GPIO1_C2	LCDC_D14	I2S1_8CH_SDO1_SDI3_M1	PDM_SDI3_M1	MAC_TXD0	I/O	I	down	2mA	√	
U9	GPIO1_C3/LCDC_D15/I2S1_SDO2_SDI2_M1/PDM_SDI2_M1/MAC_TXD1	GPIO1_C3	LCDC_D15	I2S1_8CH_SDO2_SDI2_M1	PDM_SDI2_M1	MAC_TXD1	I/O	I	down	2mA	√	
R9	GPIO1_C4/LCDC_D16/I2S1_SDO3_SDI1_M1/PDM_SDI1_M1/MAC_RXD0	GPIO1_C4	LCDC_D16	I2S1_8CH_SDO3_SDI1_M1	PDM_SDI1_M1	MAC_RXD0	I/O	I	down	2mA	√	
Y9	GPIO1_C5/LCDC_D17/I2S1_SDI0_M1/PDM_SDI0_M1/MAC_RXD1	GPIO1_C5	LCDC_D17	I2S1_8CH_SDI0_M1	PDM_SDI0_M1	MAC_RXD1	I/O	I	down	2mA	√	
W9	GPIO1_C6/UART1_CTSN/UART2_RX_M0/SPI2_MISO/JTAG_TCK	GPIO1_C6	UART1_CTSN	UART2_RX_M0	SPI2_MISO	JTAG_TCK	I/O	I	up	2mA	√	
T9	GPIO1_C7/UART1_RTSN/UART2_TX_M0/SPI2_MOSI/JTAG_TMS	GPIO1_C7	UART1_RTSN	UART2_TX_M0	SPI2_MOSI	JTAG_TMS	I/O	I	up	2mA	√	
V10	GPIO1_D0/UART1_RX/I2C0_SDA/SPI2_CLK	GPIO1_D0	UART1_RX	I2C0_SDA	SPI2_CLK		I/O	I	up	2mA	√	
T10	GPIO1_D1/UART1_TX/I2C0_SCL/SPI2_CSN0	GPIO1_D1	UART1_TX	I2C0_SCL	SPI2_CSN0		I/O	I	up	2mA	√	
U14	GPIO2_A0/UART0_RX/SPI0_MISO	GPIO2_A0	UART0_RX	SPI0_MISO			I/O	I	up	2mA	√	APIO2_VDD
V16	GPIO2_A1/UART0_TX/SPI0_MOSI	GPIO2_A1	UART0_TX	SPI0_MOSI			I/O	I	up	2mA	√	
Y16	GPIO2_A2/UART0_CTSN/SPI0_CLK/I2C2_SDA	GPIO2_A2	UART0_CTSN	SPI0_CLK	I2C2_SDA		I/O	I	up	2mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
W16	GPIO2_A3/UART0_RTSN/ SPI0_CSN0/I2C2_SCL	GPIO2_A3	UART0_RTSN	SPI0_CSN0	I2C2_SCL		I/O	I	up	2mA	√	
T15	GPIO2_A4/I2S0_MCLK/PDM_CLK_M_M2	GPIO2_A4	I2S0_8CH_MCLK	PDM_CLK_M_M2			I/O	I	down	2mA	√	
R15	GPIO2_A5/I2S0_SCLK_TX	GPIO2_A5	I2S0_8CH_SCLK_TX				I/O	I	down	2mA	√	
T16	GPIO2_A6/I2S0_SCLK_RX/PDM_CLK_S_M2	GPIO2_A6	I2S0_8CH_SCLK_RX	PDM_CLK_S_M2			I/O	I	down	2mA	√	
V17	GPIO2_A7/I2S0_LRCK_TX	GPIO2_A7	I2S0_8CH_LRCK_TX				I/O	I	down	2mA	√	
R16	GPIO2_B0/I2S0_LRCK_RX	GPIO2_B0	I2S0_8CH_LRCK_RX				I/O	I	down	2mA	√	
V14	GPIO2_B1/I2S0_SDO0	GPIO2_B1	I2S0_8CH_SDO0				I/O	I	down	2mA	√	
V15	GPIO2_B2/I2S0_SDO1	GPIO2_B2	I2S0_8CH_SDO1				I/O	I	down	2mA	√	
U16	GPIO2_B3/I2S0_SDO2	GPIO2_B3	I2S0_8CH_SDO2				I/O	I	down	2mA	√	
T17	GPIO2_B4/I2S0_SDO3	GPIO2_B4	I2S0_8CH_SDO3				I/O	I	down	2mA	√	
T14	GPIO2_B5/I2S0_SDI0/PDM_SDI0_M2	GPIO2_B5	I2S0_8CH_SDI0	PDM_SDI0_M2			I/O	I	down	2mA	√	
U15	GPIO2_B6/I2S0_SDI1/PDM_SDI1_M2	GPIO2_B6	I2S0_8CH_SDI1	PDM_SDI1_M2			I/O	I	down	2mA	√	
W14	GPIO2_B7/I2S0_SDI2/PDM_SDI2_M2	GPIO2_B7	I2S0_8CH_SDI2	PDM_SDI2_M2			I/O	I	down	2mA	√	
Y14	GPIO2_C0/I2S0_SDI3/PDM_SDI3_M2	GPIO2_C0	I2S0_8CH_SDI3	PDM_SDI3_M2			I/O	I	down	2mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
U11	GPIO3_A0/FLASH_D0/EMMC_D0/SFC_SIO0	GPIO3_A0	FLASH_D0	EMMC_D0	SFC_SIO0		I/O	I	up	8mA	√	APIO3_VDD
V12	GPIO3_A1/FLASH_D1/EMMC_D1/SFC_SIO1	GPIO3_A1	FLASH_D1	EMMC_D1	SFC_SIO1		I/O	I	up	8mA	√	
Y12	GPIO3_A2/FLASH_D2/EMMC_D2/SFC_WP_SIO2	GPIO3_A2	FLASH_D2	EMMC_D2	SFC_WP_SIO2		I/O	I	up	8mA	√	
Y11	GPIO3_A3/FLASH_D3/EMMC_D3/SFC_HOLD_SIO3	GPIO3_A3	FLASH_D3	EMMC_D3	SFC_HOLD_SIO3		I/O	I	up	8mA	√	
W11	GPIO3_A4/FLASH_D4/EMMC_D4/SFC_CLK	GPIO3_A4	FLASH_D4	EMMC_D4	SFC_CLK		I/O	I	up	8mA	√	
V11	GPIO3_A5/FLASH_D5/EMMC_D5/SFC_CSN0	GPIO3_A5	FLASH_D5	EMMC_D5	SFC_CSN0		I/O	I	up	8mA	√	
U10	GPIO3_A6/FLASH_D6/EMMC_D6	GPIO3_A6	FLASH_D6	EMMC_D6			I/O	I	up	8mA	√	
U12	GPIO3_A7/FLASH_D7/EMMC_D7	GPIO3_A7	FLASH_D7	EMMC_D7			I/O	I	up	8mA	√	
V13	GPIO3_B0/FLASH_WRN/EMMC_CMD	GPIO3_B0	FLASH_WRN	EMMC_CMD			I/O	I	up	8mA	√	
T13	GPIO3_B1/FLASH_CLE/EMMC_CLK	GPIO3_B1	FLASH_CLE	EMMC_CLK			I/O	I	down	8mA	√	
U13	GPIO3_B2/FLASH_RDN/SPI1_MISO	GPIO3_B2	FLASH_RDN	SPI1_MISO			I/O	I	up	8mA	√	
R10	GPIO3_B3/FLASH_ALE/EMMC_PWREN/SPI1_CLK	GPIO3_B3	FLASH_ALE	EMMC_PWREN	SPI1_CLK		I/O	I	down	8mA	√	
W12	GPIO3_B4/FLASH_RDY/I2C3_SDA_M1/SPI1_MOSI/UART3_RX	GPIO3_B4	FLASH_RDY	I2C3_SDA_M1	SPI1_MOSI	UART3_RX	I/O	I	up	8mA	√	

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
T12	GPIO3_B5/FLASH_CSN0/I2C3_SCL_M1/SPI1_CSN0/UART3_TX	GPIO3_B5	FLASH_CSN0	I2C3_SCL_M1	SPI1_CSN0	UART3_TX	I/O	I	up	8mA	√	
J19	GPIO4_A0/SDIO_D0	GPIO4_A0	SDIO_D0				I/O	I	up	2mA	√	APIO4_VDD
J17	GPIO4_A1/SDIO_D1	GPIO4_A1	SDIO_D1				I/O	I	up	2mA	√	
G18	GPIO4_A2/SDIO_D2	GPIO4_A2	SDIO_D2				I/O	I	up	2mA	√	
G17	GPIO4_A3/SDIO_D3	GPIO4_A3	SDIO_D3				I/O	I	up	2mA	√	
H18	GPIO4_A4/SDIO_CMD	GPIO4_A4	SDIO_CMD				I/O	I	up	2mA	√	
J18	GPIO4_A5/SDIO_CLK	GPIO4_A5	SDIO_CLK				I/O	I	down	2mA	√	
K19	GPIO4_A6/UART4_CTSN	GPIO4_A6	UART4_CTSN				I/O	I	up	2mA	√	
K18	GPIO4_A7/UART4_RTSN	GPIO4_A7	UART4_RTSN				I/O	I	up	2mA	√	
F17	GPIO4_B0/UART4_RX	GPIO4_B0	UART4_RX				I/O	I	up	2mA	√	
J16	GPIO4_B1/UART4_TX	GPIO4_B1	UART4_TX				I/O	I	up	2mA	√	
G16	GPIO4_B2	GPIO4_B2					I/O	I	down	2mA	√	
F19	GPIO4_B3	GPIO4_B3					I/O	I	down	2mA	√	
H16	GPIO4_B4/I2S0_2CH_MCLK	GPIO4_B4	I2S0_2CH_MCLK				I/O	I	down	2mA	√	
F18	GPIO4_B5/I2S0_2CH_SCLK	GPIO4_B5	I2S0_2CH_SCLK				I/O	I	down	2mA	√	
J15	GPIO4_B6/I2S0_2CH_LRCK_TX	GPIO4_B6	I2S0_2CH_LRCK_TX				I/O	I	down	2mA	√	
H15	GPIO4_B7/I2S0_2CH_SDO	GPIO4_B7	I2S0_2CH_SDO				I/O	I	down	2mA	√	
H14	GPIO4_C0/I2S0_2CH_SDI	GPIO4_C0	I2S0_2CH_SDI				I/O	I	down	2mA	√	
B17	GPIO4_D0/SDMMC_D0	GPIO4_D0	SDMMC_D0	PMU_ST0			I/O	I	up	8mA	√	APIO5_VDD

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
A17	GPIO4_D1/SDMMC_D1	GPIO4_D1	SDMMC_D1	PMU_ST1			I/O	I	up	8mA	√	
B15	GPIO4_D2/SDMMC_D2/UART2_RX_M1	GPIO4_D2	SDMMC_D2	UART2_RX_M1	PMU_ST2		I/O	I	up	8mA	√	
A15	GPIO4_D3/SDMMC_D3/UART2_TX_M1	GPIO4_D3	SDMMC_D3	UART2_TX_M1	PMU_ST3		I/O	I	up	8mA	√	
C16	GPIO4_D4/SDMMC_CMD	GPIO4_D4	SDMMC_CMD	PMU_ST4			I/O	I	up	8mA	√	
B16	GPIO4_D5/SDMMC_CLK	GPIO4_D5	SDMMC_CLK	PMU_DEBUGTX			I/O	I	down	8mA	√	
B14	GPIO4_D6/SDMMC_PWREN	GPIO4_D6	SDMMC_PWREN				I/O	I	down	8mA	√	
E2	DDR_DQ4	DDR_DQ4					A					DDR_VDD
E3	DDR_DQ6	DDR_DQ6					A					
K2	DDR_DQ7	DDR_DQ7					A					
F1	DDR_DQ5	DDR_DQ5					A					
K4	DDR_DQS0N	DDR_DQS0N					A					
J3	DDR_DQS0	DDR_DQS0					A					
G5	DDR_DQ1	DDR_DQ1					A					
L1	DDR_DQ3	DDR_DQ3					A					
H4	DDR_DQ2	DDR_DQ2					A					
J4	DDR_DQ0	DDR_DQ0					A					
G1	DDR_DM0	DDR_DM0					A					
L3	DDR_DM1	DDR_DM1					A					
F4	DDR_DQ8	DDR_DQ8					A					
L4	DDR_DQ10	DDR_DQ10					A					
D3	DDR_DQ11	DDR_DQ11					A					
G2	DDR_DQ9	DDR_DQ9					A					
H2	DDR_DQS1	DDR_DQS1					A					
H3	DDR_DQS1N	DDR_DQS1N					A					

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
F3	DDR_DQ13	DDR_DQ13					A					
K5	DDR_DQ15	DDR_DQ15					A					
M2	DDR_DQ14	DDR_DQ14					A					
L2	DDR_DQ12	DDR_DQ12					A					
B10	DDR_A14	DDR_A14					A					
D7	DDR_A13	DDR_A13					A					
E4	DDR_RESET	DDR_RESET					A					
A10	DDR_A8	DDR_A8					A					
A2	DDR_A7	DDR_A7					A					
A6	DDR_A6	DDR_A6					A					
E7	DDR_A9	DDR_A9					A					
B5	DDR_A11	DDR_A11					A					
A3	DDR_A2	DDR_A2					A					
B7	DDR_A4	DDR_A4					A					
B3	DDR_A5	DDR_A5					A					
A5	DDR_A1	DDR_A1					A					
E6	DDR_A3	DDR_A3					A					
B6	DDR_A12	DDR_A12					A					
B4	DDR_A0	DDR_A0					A					
C8	DDR_BA1	DDR_BA1					A					
D6	DDR_BA2	DDR_BA2					A					
B2	DDR_BA0	DDR_BA0					A					
B1	DDR_CS0N	DDR_CS0N					A					
E8	DDR_WEN	DDR_WEN					A					
C9	DDR_A10	DDR_A10					A					
C5	DDR_ODT0	DDR_ODT0					A					
B9	DDR_CKE	DDR_CKE					A					
D8	DDR_CASN	DDR_CASN					A					

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
C2	DDR_CLKN	DDR_CLKN					A					
C3	DDR_CLK	DDR_CLK					A					
D5	DDR_RASN	DDR_RASN					A					
A19	ADC_IN0	ADC_IN0					A					SARADC
C18	ADC_IN2	ADC_IN2					A					
B19	ADC_IN1	ADC_IN1					A					
A18	ADC_IN3	ADC_IN3					A					
B18	ADC_IN4	ADC_IN4					A					
D18	ADC_IN5	ADC_IN5					A					
B13	USB0_DP	USB0_DP					A					USB
A13	USB0_DM	USB0_DM					A					
C12	USB_ID	USB_ID					A					
C15	USB_EXTR	USB_EXTR					A					
C14	USB_VBUS	USB_VBUS					A					
B12	USB1_DP	USB1_DP					A					
A12	USB1_DM	USB1_DM					A					
W18	CODEC_HPOUT_R	CODEC_HPOUT_R					A					Audio Codec
W19	CODEC_LINEOUT_R	CODEC_LINEOUT_R					A					
V18	CODEC_HPDET	CODEC_HPDET					A					
W20	CODEC_LINEOUT_L	CODEC_LINEOUT_L					A					
Y19	CODEC_HPOUT_L	CODEC_HPOUT_L					A					
T18	CODEC_VCMH	CODEC_VCMH					A					
U18	CODEC_MICBIAS2	CODEC_MICBIAS2					A					

Pin	Pin Name	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def ③	Pull	Drive Strength②	INT ④	DIE Power Domain
Y18	CODEC_MICBIAS1	CODEC_MICBIAS1					A					
V19	CODEC_MICN1	CODEC_MICN1					A					
V20	CODEC_MICP1	CODEC_MICP1					A					
T20	CODEC_LINE1	CODEC_LINE1					A					
T19	CODEC_LINE2	CODEC_LINE2					A					
U20	CODEC_MICP2	CODEC_MICP2					A					
U19	CODEC_MICN2	CODEC_MICN2					A					
R18	CODEC_VCM	CODEC_VCM					A					
P18	CODEC_MICP3	CODEC_MICP3					A					
P17	CODEC_MICN3	CODEC_MICN3					A					
R20	CODEC_MICP4	CODEC_MICP4					A					
R19	CODEC_MICN4	CODEC_MICN4					A					
P20	CODEC_MICP5	CODEC_MICP5					A					
P19	CODEC_MICN5	CODEC_MICN5					A					
N18	CODEC_MICP6	CODEC_MICP6					A					
M18	CODEC_MICN6	CODEC_MICN6					A					
N20	CODEC_MICP7	CODEC_MICP7					A					
N19	CODEC_MICN7	CODEC_MICN7					A					
M20	CODEC_MICP8	CODEC_MICP8					A					
M19	CODEC_MICN8	CODEC_MICN8					A					

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②: Output Drive Unit is mA, only Digital IO has drive value;

③: Reset state: I = input, O = output;

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN_24M	I	Clock input of 24MHz crystal
	XOUT_24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset
	TVSS	I	Chip test mode enable
	NPOR_BYPASS	I	Chip internal NPOR module bypass control signal
	REF_CLKOUT	O	REF Clock Output for external function module
	TEST_CLKOUT	O	Chip internal clock output for measurement
	PMIC_SLEEP	O	Chip low power mode output indication signal
	TSADC_SHUT	O	Chip high temperature output indication signal
	RTC_CLK	I	32K RTC clock input
	PMU_ST*i*(*i*=0~4)	O	Chip low power mode state output signal
	PMU_DEBUGTX	O	Chip low power mode state output signal

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TCK	I	SWD interface clock input
	JTAG_TMS	I/O	SWD interface data input/output

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	SDMMC_CLK	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D[*i*] (*i*=0~3)	I/O	sdmmc card data input and output
	SDMMC_DET	I	sdmmc card detect signal, 0 represents presence of card

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLK	O	sdio card clock
	SDIO_CMD	I/O	sdio card command output and response input
	SDIO_D[*i*] (*i*=0~3)	I/O	sdio card data input and output

Interface	Pin Name	Direction	Description
	EMMC_CLK	O	emmc card clock

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_D[*i*] (*i*=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
Nand Flash Interface	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable signal
	FLASH_RDN	O	Flash read enable signal
	FLASH_D*i*(*i*=0~7)	I/O	Flash data input/output signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH_CSN*i*(*i*=0)	O	Flash chip enable signal for chip i, i=0

Interface	Pin Name	Direction	Description
SFC Controller	SFC_CLK	O	sfc serial clock
	SFC_CSN*i*(*i=0*)	O	sfc chip select signal, low active
	SFC_SIO*i*(*i=0~3*)	I/O	sfc serial data input/output signal

Interface	Pin Name	Direction	Description
LCDC	LCDC_DCLK	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_VSYNC	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LDCD_HSYNC	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	LCDC_DEN	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_D*i*(*i*=0~17)	O	LCDC data output

Interface	Pin Name	Direction	Description
DDR Interface	DDR_CLK	O	Active-high clock signal to the memory device.
	DDR_CLKN	O	Active-low clock signal to the memory device.
	DDR_CKE	O	Active-high clock enable signal to the memory device
	DDR_CS*i*N (*i*=0)	O	Active-low chip select signal to the memory device.
	DDR_RASN	O	Active-low row address strobe to the memory device.
	DDR_CASN	O	Active-low column address strobe to the memory device.
	DDR_WEN	O	Active-low write enable strobe to the memory device.
	DDR_BA*i*(*i*=0,1,2)	O	Bank address signal to the memory device.

Interface	Pin Name	Direction	Description
	DDR_A*i*(*i*=0~14)	O	Address signal to the memory device.
	DDR_DQ*i*(*i*=0~15)	I/O	Bidirectional data line to the memory device.
	DDR_DQS*i*(i=0~1)	I/O	Active-high bidirectional data strobes to the memory device.
	DDR_DQS*i*N(*i*=0~1)	I/O	Active-low bidirectional data strobes to the memory device.
	DDR_DM*i*(1=0~1)	O	Data mask signal to the memory device.
	DDR_ODT*i*(i=0)	O	On-Die Termination output signal.
	DDR_RESET	O	Reset signal to the memory device.

Interface	Pin Name	Direction	Description
I2S_8CH_0 Controller	I2S0_8CH_MCLK	O	I2S/PCM/TDM clock source
	I2S0_8CH_SCLK_RX	I/O	I2S/PCM/TDM receiving serial clock
	I2S0_8CH_SCLK_TX	I/O	I2S/PCM/TDM transmitting serial clock
	I2S0_8CH_LRCK_RX	I/O	I2S/PCM/TDM left & right channel signal for receiving serial data
	I2S0_8CH_LRCK_TX	I/O	I2S/PCM/TDM left & right channel signal for transmitting serial data
	I2S0_8CH_SDI*i* (*i*=1~3)	I	I2S/PCM/TDM serial data input
	I2S0_8CH_SDO*i* (*i*=1~3)	O	I2S/PCM/TDM serial data output

Interface	Pin Name	Direction	Description
I2S_8CH_1 Controller	I2S1_8CH_MCLK_M*i* (*i*=0~1)	O	I2S/PCM/TDM clock source
	I2S1_8CH_SCLK_RX_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM receiving serial clock
	I2S1_8CH_SCLK_TX_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM transmitting serial clock
	I2S1_8CH_LRCK_RX_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM left & right channel signal for receiving serial data
	I2S1_8CH_LRCK_TX_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM left & right channel signal for transmitting serial data
	I2S1_8CH_SDO0_M*i* (*i*=0~1)	O	I2S/PCM/TDM serial data output
	I2S1_8CH_SDO1_SDI3_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM serial data input/output
	I2S1_8CH_SDO2_SDI2_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM serial data input/output
	I2S1_8CH_SDO3_SDI1_M*i* (*i*=0~1)	I/O	I2S/PCM/TDM serial data input/output
	I2S1_8CH_SDI0_M*i* (*i*=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
I2S_2CH_0 Controller	I2S0_2CH_MCLK	O	I2S/PCM clock source
	I2S0_2CH_SCLK	I/O	I2S/PCM serial clock
	I2S0_2CH_LRCK_TX	I/O	I2S/PCM left & right channel signal for transmitting serial data
	I2S0_2CH_SDI	I	I2S/PCM serial data input
	I2S0_2CH_SDO	O	I2S/PCM serial data output

Interface	Pin Name	Direction	Description
PDM	PDM_CLK_M*i*(*i*=0~1)	O	PDM sampling clock

Interface	Pin Name	Direction	Description
	PDM_CLK_M_M2	O	PDM sampling clock
	PDM_CLK_S_M2	O	PDM sampling clock
	PDM_SDI0_M*i*(*i*=0~2)	I	PDM data
	PDM_SDI1_M*i*(*i*=0~2)	I	PDM data
	PDM_SDI2_M*i*(*i*=0~2)	I	PDM data
	PDM_SDI3_M*i*(*i*=0~2)	I	PDM data

Interface	Pin Name	Direction	Description
SPI	SPI*i*_CLK(*i*=0~2)	I/O	SPI serial clock
	SPI*i*_CSN0(*i*=0~2)	I/O	SPI chip select signal, low active
	SPI*i*_MISO(*i*=0~2)	I/O	SPI serial data input/output
	SPI*i*_MOSI(*i*=0~2)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input and output
	PWM1	I/O	Pulse Width Modulation input and output
	PWM2	I/O	Pulse Width Modulation input and output
	PWM3	I/O	Pulse Width Modulation input and output, used for IR application recommended

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA (*i*=0,1,2,3)	I/O	I2C data
	I2C*i*_SCL (*i*=0,1,2,3)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX (*i*=0,1,2,3,4)	I	UART serial data input
	UART*i*_TX (*i*=0,1,2,3,4)	O	UART serial data output
	UART*i*_CTSN (*i*=0,1,4)	I	UART clear to send modem status input
	UART*i*_RTSN (*i*=0,1,4)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
MAC	MAC_CLK	I/O	MAC REC_CLK output or external clock input
	MAC_MDC	O	MAC management interface clock
	MAC_MDIO	I/O	MAC management interface data
	MAC_TXD*i*(*i*=0~1)	O	MAC TX data
	MAC_RXD*i*(*i*=0~1)	I	MAC RX data

Interface	Pin Name	Direction	Description
	MAC_TXEN	O	MAC TX data enable
	MAC_RXER	I	MAC RX error signal
	MAC_RXDV	I	MAC RX data valid signal

Interface	Pin Name	Direction	Description
USB 2.0	USB0_DP	I/O	USB 2.0 Data signal DP
	USB0_DM	I/O	USB 2.0 Data signal DM
	USB1_DP	I/O	USB 2.0 Data signal DP
	USB1_DM	I/O	USB 2.0 Data signal DM
	USB_EXTR	O	Connect 133 ohm resistor to ground to generate reference current
	USB_VBUS	I	Insert detect when act as USB device
	USB_ID	I	USB Mini-Receptacle Identifier

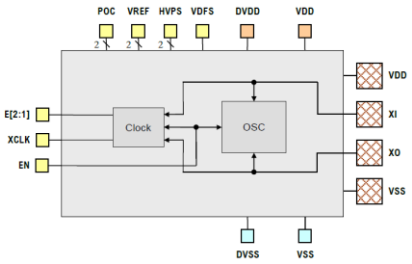
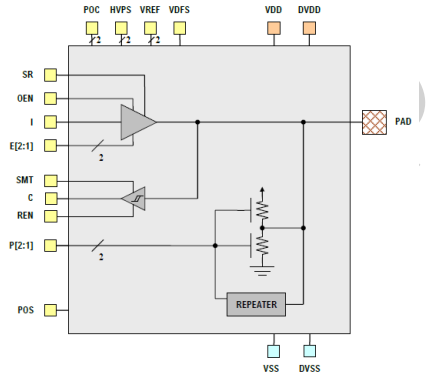
Interface	Pin Name	Direction	Description
Audio Codec	CODEC_HPOUT_R	O	Right DAC channel headphone output
	CODEC_HPOUT_L	O	Left DAC channel headphone output
	CODEC_LINEOUT_R	O	Right DAC channel line output
	CODEC_LINEOUT_L	O	Left DAC channel line output
	CODEC_MICBIAS1	O	Microphone bias voltage1
	CODEC_MICBIAS2	O	Microphone bias voltage2
	CODEC_VCMH	O	Reference voltage output for microphone bias voltage
	CODEC_LINE1	I	ADC channel 1 line input
	CODEC_LINE2	I	ADC channel 2 line input
	CODEC_MICN1	I	ADC channel 1 Microphone input
	CODEC_MICP1	I	ADC channel 1 Microphone input
	CODEC_MICN2	I	ADC channel 2 Microphone input
	CODEC_MICP2	I	ADC channel 2 Microphone input
	CODEC_MICN3	I	ADC channel 3 Microphone input
	CODEC_MICP3	I	ADC channel 3 Microphone input
	CODEC_MICN4	I	ADC channel 4 Microphone input
	CODEC_MICP4	I	ADC channel 4 Microphone input
	CODEC_MICN5	I	ADC channel 5 Microphone input
	CODEC_MICP5	I	ADC channel 5 Microphone input
	CODEC_MICN6	I	ADC channel 6 Microphone input

Interface	Pin Name	Direction	Description
	CODEC_MICP6	I	ADC channel 6 Microphone input
	CODEC_MICN7	I	ADC channel 7 Microphone input
	CODEC_MICP7	I	ADC channel 7 Microphone input
	CODEC_MICN8	I	ADC channel 8 Microphone input
	CODEC_MICP8	I	ADC channel 8 Microphone input
	CODEC_VCM	O	Reference voltage output
	CODEC_HPDET	I	Headphone insertion detection

2.9 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 IO Type List

Type	Diagram	Description	Pin Name
A		Crystal Oscillator with high enable	XIN_24M / XOUT_24M
B		Tri-state output pad with input, which pull-up/ pull-down, slew rate and drive strength is configurable	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CORE_VDD	-0.30	TBD	V
Supply voltage for Logic	LOGIC_VDD	-0.30	1.10	V
1.0V supply voltage		-0.30	1.10	V
1.8V supply voltage		-0.30	1.98	V
3.3V supply voltage		-0.30	3.63	V
Supply voltage for DDR IO		-0.30	1.89	V
Storage Temperature	Tstg	TBD	TBD	℃
Max Conjunction Temperature	Tj	TBD	TBD	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	CORE_VDD	0.95	1.00	1.35	V
Voltage for Logic	LOGIC_VDD	0.90	1.00	1.10	V
Max frequency of CPU	Frequency			TBD	GHz
Digital GPIO Power (3.3V/1.8V)	APIO0,APIO1,APIO2, APIO3,APIO4,APIO5	2.97 1.62	3.30 1.80	3.63 1.98	V
DDR2 IO power	DDR_VDD	1.71	1.80	1.89	V
DDR3 IO power	DDR_VDD	1.425	1.50	1.575	V
DDR3L IO Power	DDR_VDD	1.283	1.35	1.418	V
LPDDR2 IO Power	DDR_VDD	1.14	1.20	1.26	V
OTP Analog Power	OTP_VCC_1V8	1.62	1.80	1.98	V
PLL Analog Power(1.0V)	PLL_AVDD_1V0	0.90	1.00	1.10	V
PLL Analog Power(1.8V)	PLL_AVDD_1V8	1.62	1.80	1.98	V
SARADC Analog Power	SADC_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (1.0V)	USB_VDD_1V0	0.90	1.00	1.10	V
USB 2.0 OTG/Host Analog Power (1.8V)	USB_AVDD_1V8	1.62	1.80	1.98	V
USB 2.0 OTG/Host Analog Power (3.3V)	USB_AVDD_3V3	2.97	3.30	3.63	V

Parameters	Symbol	Min	Typ	Max	Unit
Audio Codec Analog Power (1.8V)	CODEC_AVDD_1V8	1.62	1.80	1.98	V
Audio Codec Analog Power (3.3V)	CODEC_AVDD_3V3	2.97	3.30	3.63	V
Internal NPOR Analog Power	NPOR_AVDD_3V3	2.97	3.30	3.63	V
OSC input clock frequency		N/A	24	N/A	MHz
Max CPU frequency of A35		N/A	N/A	TBD	GHz
Ambient Operating Temperature	T_A	N/A	25	80	℃

Notes:

① *Symbol name is same as the pin name in the io descriptions*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	3.3-0.4	NA	NA	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	1.8-0.4	NA	NA	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @ LPDDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	VREF + 0.13	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF-0.13	V
DDR IO @ DDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	VREF + 0.13	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF-0.13	V
DDR IO @ @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDD	V

Parameters		Symbol	Min	Typ	Max	Unit
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @ @DDR3L mode	Input High Voltage	Vih_ddr	VREF + 0.09	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_ddr	VREF + 0.09	NA	DDR_VDD	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.09	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pull down disabled	NA	NA	10	uA
			Vin = 3.3V, pull down enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	10	uA
			Vin = 1.8V, pull down enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	10	uA
			Vin = 0V, pull up enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @1.8V/1.0V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/1.0V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @1.8V/1.0V	800		3200	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @1.8V/1.0V	16		3200	MHz

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Lock time	T_{lt}	FREF=24M,REFDIV=1 @1.8V/1.0V		250	500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @1.8V Current scale as $(Fvco/1GHz)^{1.5}$		1.0	1.2	mA
	VDD Current consumption		VDD =1.0V		1.3	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		13		uA

Notes:

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
High input level	VIH		NA	1.1	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance		(seen at D+ or D-)	NA	NA	3	pF
Squelch threshold			100	112	150	mV

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.7 Electrical Characteristics for TSADC

Table 3-7 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution				+/-5		℃
Temperature Range			-20		120	℃
Analog power	IAVDD	Fs= 50KS/s		200		uA
Digital power	IVDD	Fs= 50KS/s		20		uA
Clock Frequency	Fclk	Fclk			50	KHz
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IVDD	Power down		2		uA

3.8 Electrical Characteristics for SARADC

Table 3-8 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Resolution				10		bit
Effective Number of Bit	ENOB			9		bit
Differential Nonlinearity	DNL		-1		+1	LSB
Integral Nonlinearity	INL		-2		+2	LSB
Input Voltage Range	VIN		0		1	AVDD
Input Capacitance	CIN			10		pF
Sampling Rate	fs				1	MS/s
Analog power	IAVDD	Fs= 1MS/s		450		uA
Digital power	IVDD	Fs= 1MS/s		50		uA
Power Down Current from Analog	IAVDD	Power down		1		uA
Power Down Current from Digital	IVDD	Power down		1		uA

3.9 Electrical Characteristics for Audio Codec

Table 3-9 Electrical Characteristics for Audio Codec

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Microphone Bias						
MICBIAS1 Voltage	V(MICBIAS1)		0.5*AVDD3V3		0.85*AVDD3V3	V
MICBIAS2	V(MICBIAS2)		0.5*AVDD3V3		0.85*AVDD3V3	V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Voltage						
Bias Step Size				0.05*AVDD3V3		V
Bias Current	I(MICBIAS)				3	mA
Microphone Gain Boost PGA						
Programmable Gain	G(BST)		0		20	dB
Gain Step Size				20		dB
Input Resistance	RIN	G(BST)=0db		110		Kohm
		G(BST)=20db		20		Kohm
Input Capacitance	CIN			10		pF
ALC PGA						
Programmable Gain	G(ALC)		-18		28.5	dB
Gain Step Size				1.5		dB
ADC						
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	(-3dBFS) input		-80		dB
Channel Separation				80		dB
Power Supply Rejection	PSRR	1KHZ		80		dB
A/D Digital Filter Pass Band Ripple			0.1	0.125	0.125	(+/-)dB
Output Driver						
Programmable Gain	G(DRV)		-39		6	dB
Gain Step Size				1.5		dB
Output Resistance	ROUT			1		Kohm
Output Capacitance	COUT			20		pF
Power Supply Rejection	PSRR	1KHZ		55		dB
Line Output						
Signal to Noise Ratio	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	(-3dBFS) output 600ohm load		-84		dB
Channel Separation				85		dB
Headphone Output						
Signal to Noise Ratio	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	16ohm load Po=18mW		-70		dB
		32ohm load Po=9mW		-75		dB
Power Consumption						
Standby				0.01 @AVDD1V8		mA
Mono Recording				2.5 @AVDD1V8		mA
Mono Playback				3 @AVDD1V8		mA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	TBD	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	TBD	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	TBD	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 4 layers, 95mmx95mm, 1.6mm thickness, Ambient temperature is 25℃.