



# Radxa Sirider S1

Schematic

V1.2

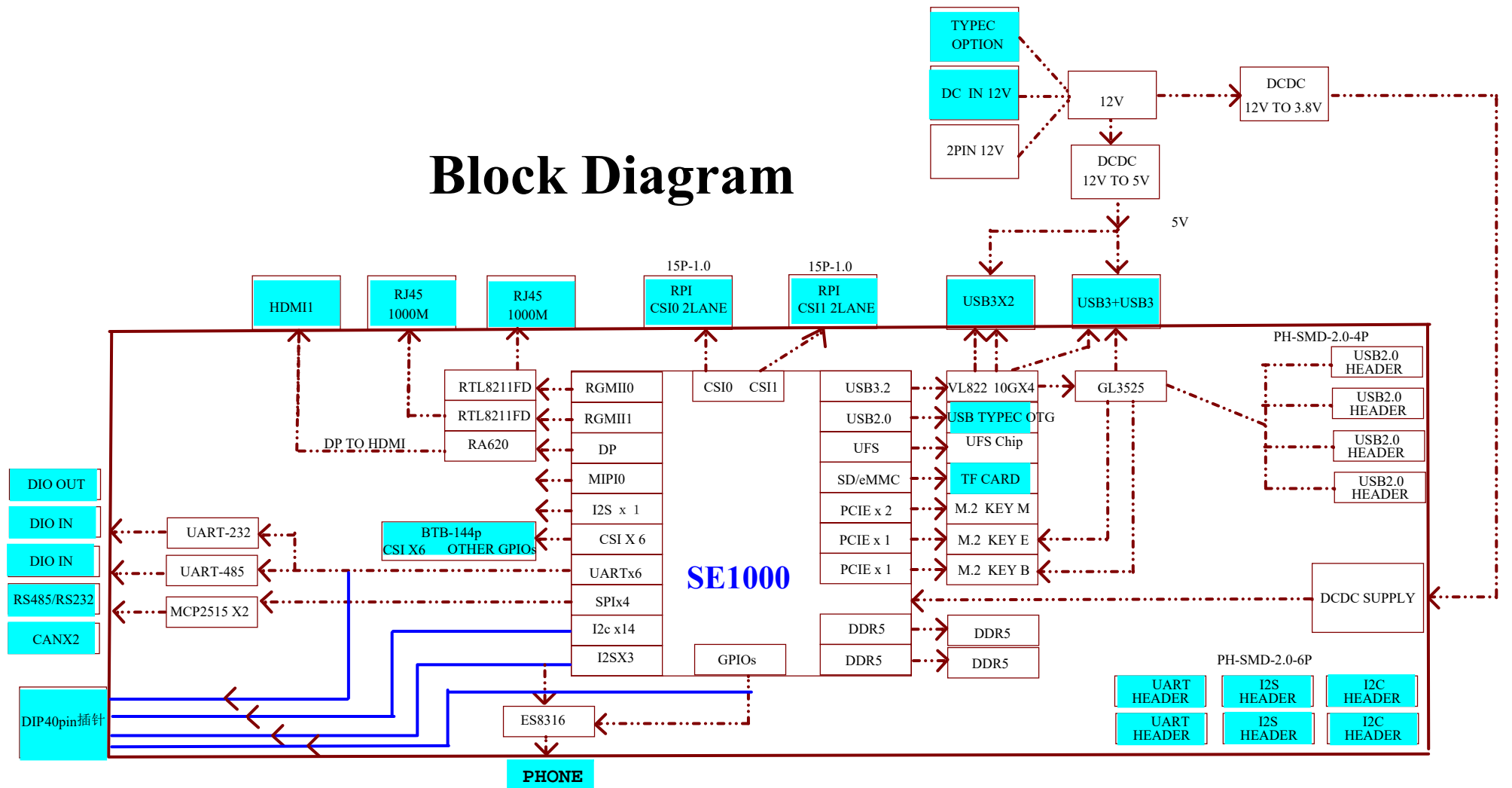
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# Block Diagram

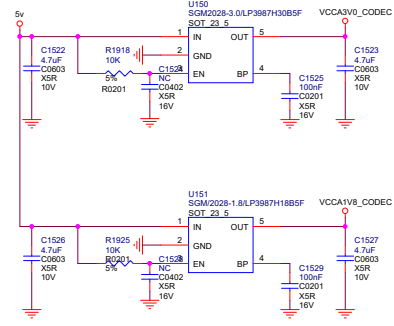
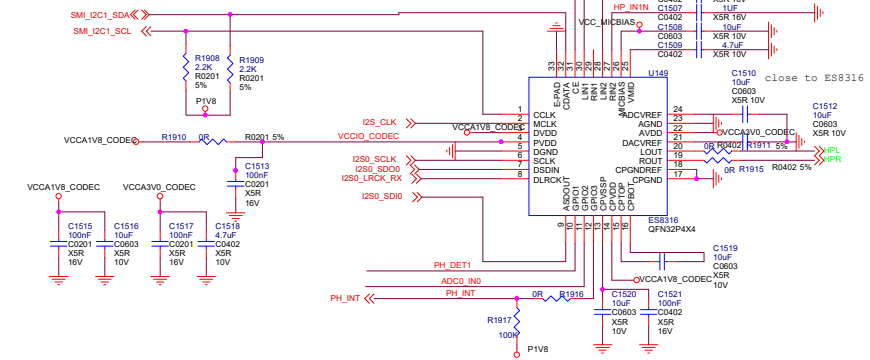


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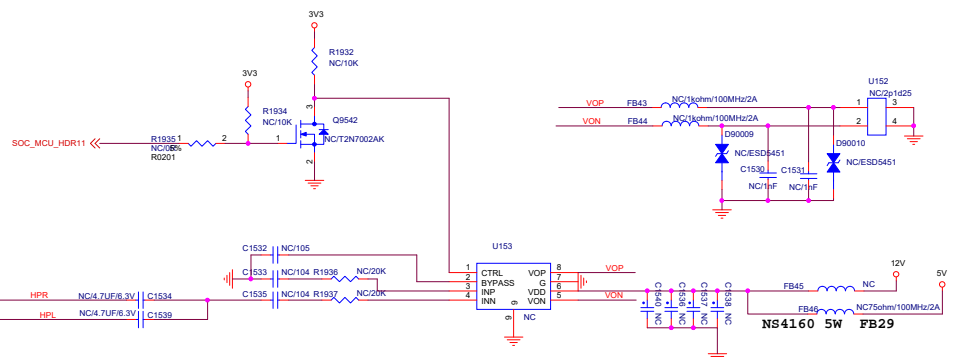
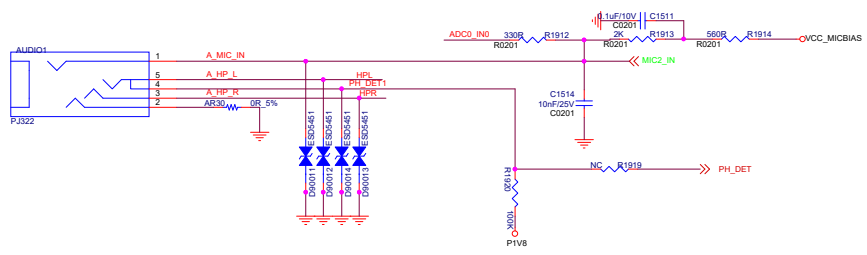


I2S

[32] A2B\_B\_TDM0\_SCK MCLKW R1995 33R C125\_CLK  
 [32] A2B\_B\_TDM0\_WS R1996 33R C125\_SCLK  
 [32] A2B\_B\_TDM0\_DIN R1997 33R C125\_LRCK\_RX  
 [32] A2B\_B\_TDM0\_DOUT R1998 33R C125\_SDO0



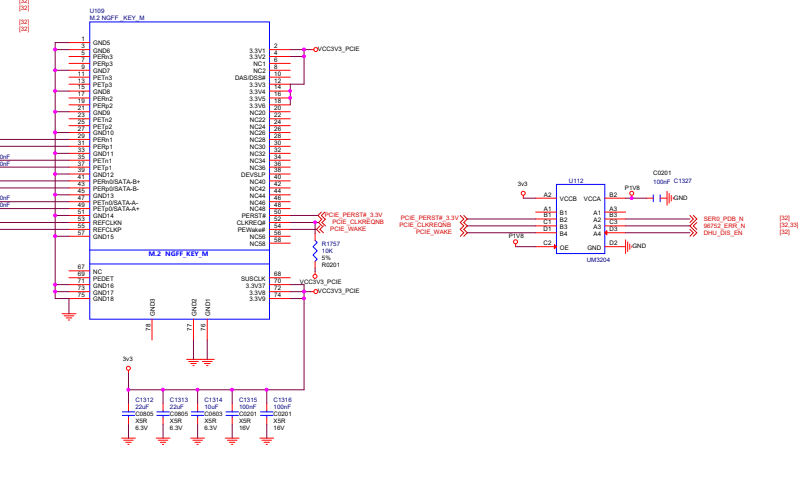
AUDIO



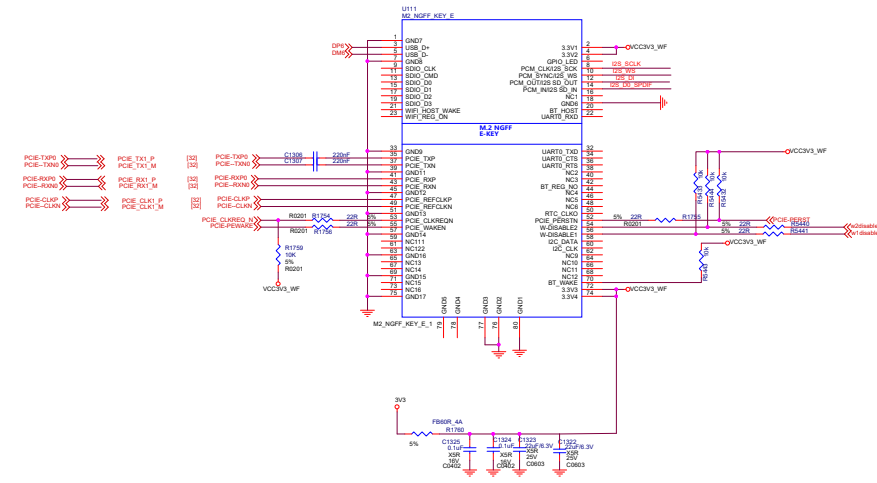
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	REV 1.2

PCE_RX0N1	→	PCE_RX0_M	(S2)
PCE_RX0P1	→	PCE_RX0_P	(S2)
PCE_TX0N1	→	PCE_TX0_M	(S2)
PCE_TX0P1	→	PCE_TX0_P	(S2)
PCE_RX0N2	→	PCE_RX0_M	(S2)
PCE_RX0P2	→	PCE_RX0_P	(S2)
PCE_TX0N2	→	PCE_TX0_M	(S2)
PCE_TX0P2	→	PCE_TX0_P	(S2)
PCE_REF_CLK0	→	PCE_CLK0_M	(S2)
PCE_REF_CLKP0	→	PCE_CLK0_P	(S2)

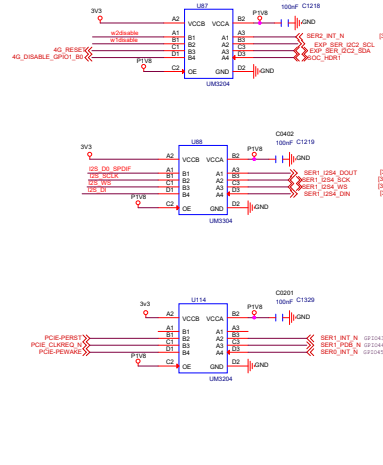
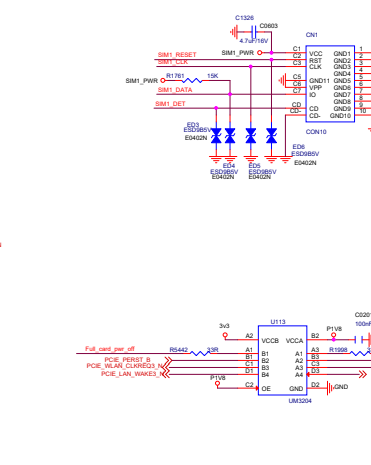
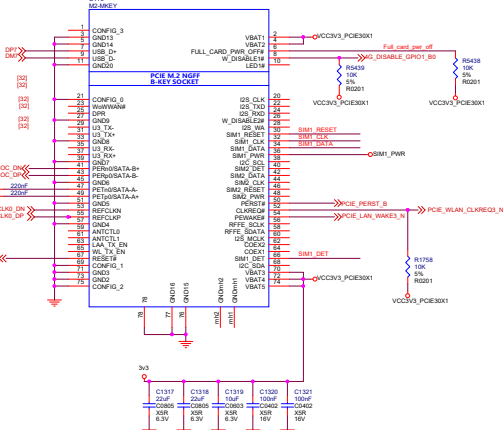
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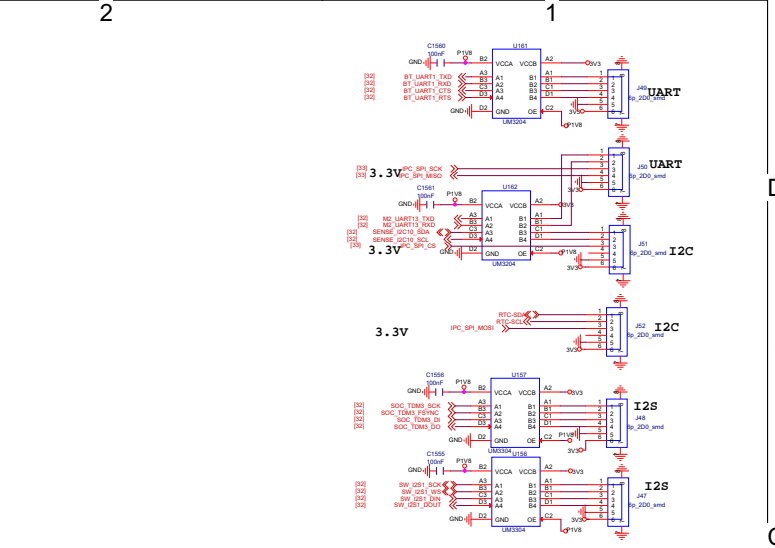
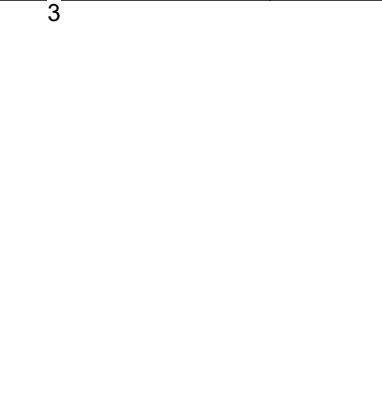
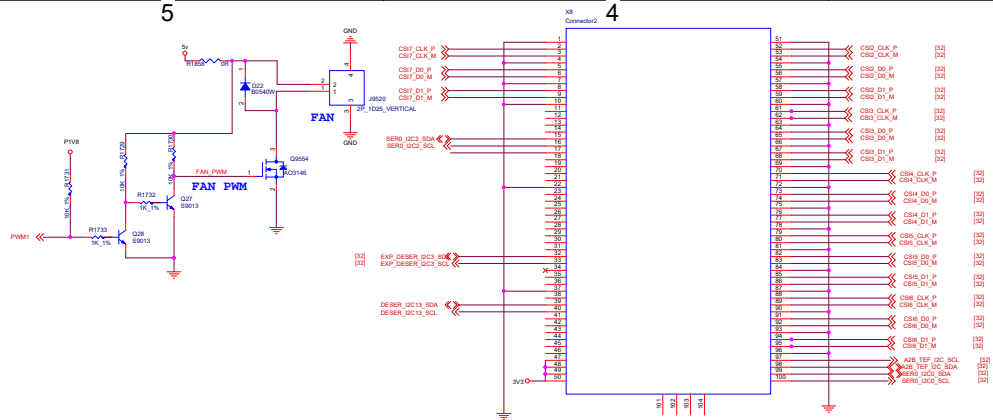


## E-KEY

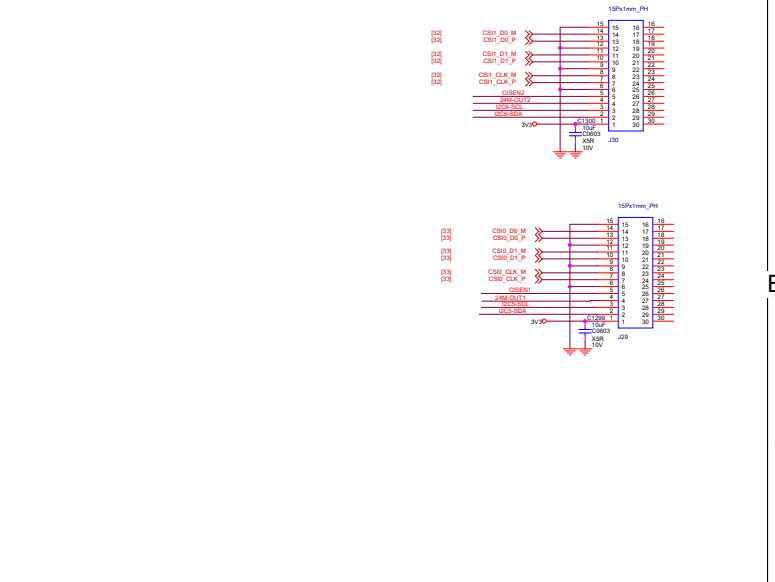
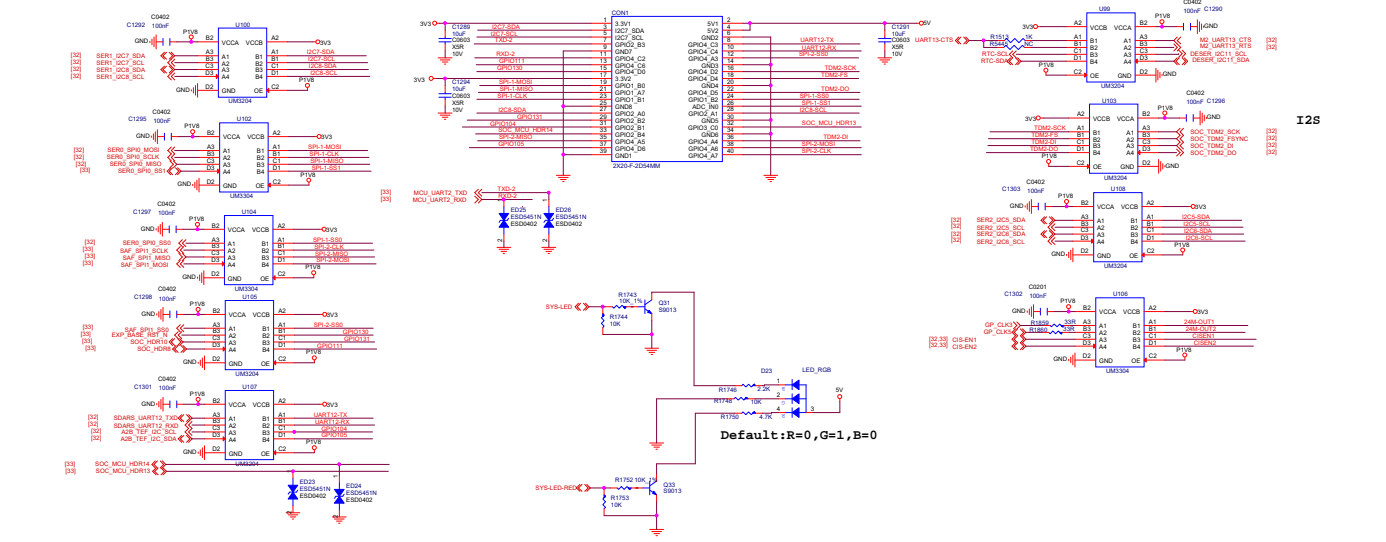


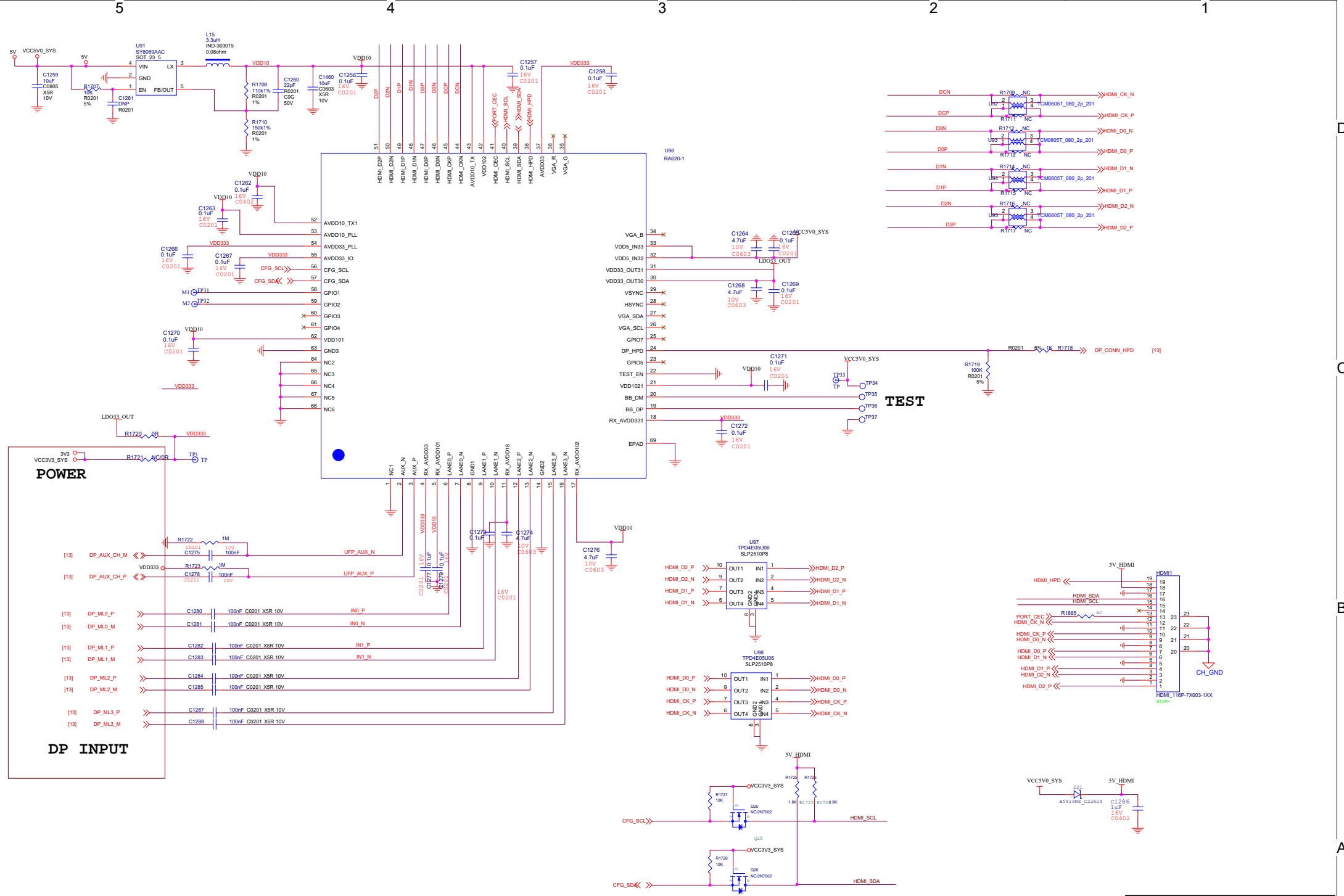
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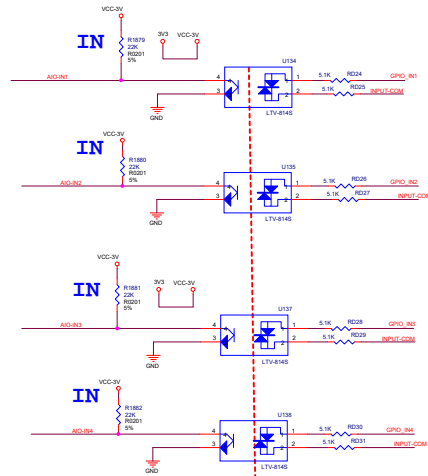
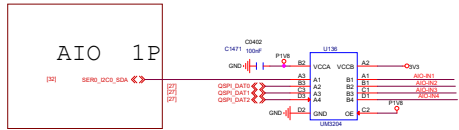


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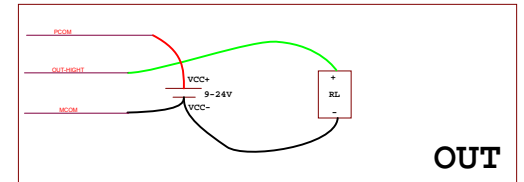
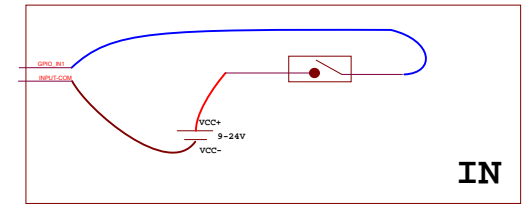
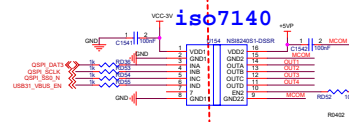
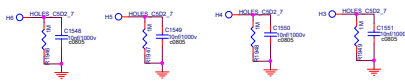
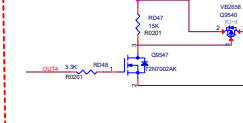
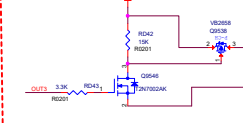
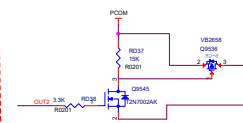
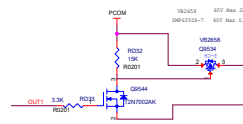
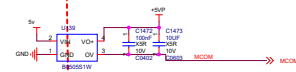




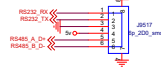
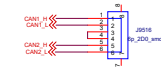
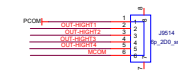
DIO X 8  
Isolated

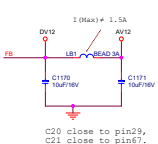
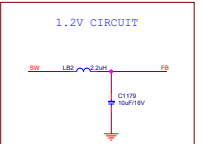
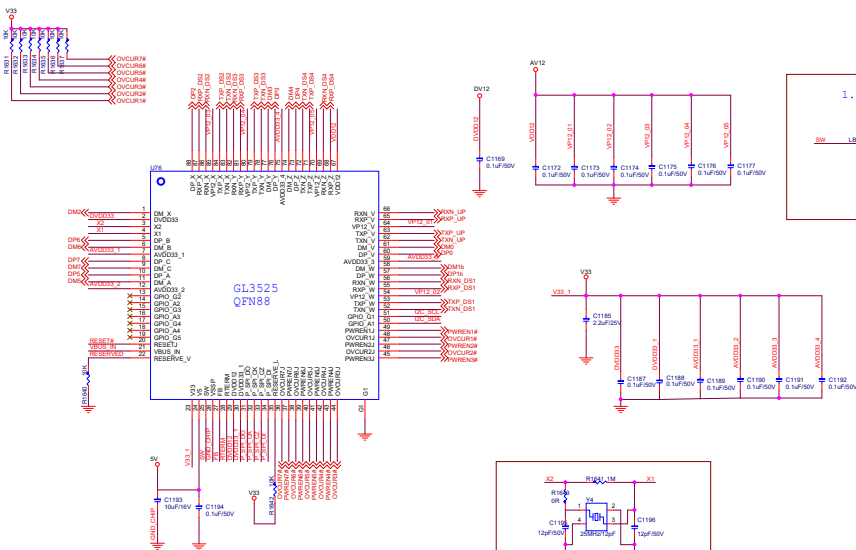
max 1A

OUT

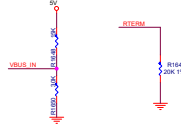
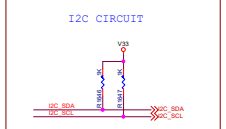
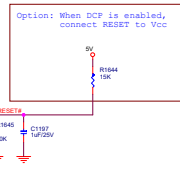
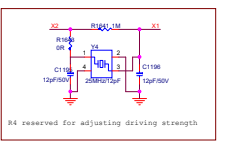
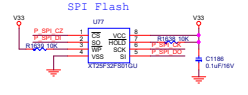
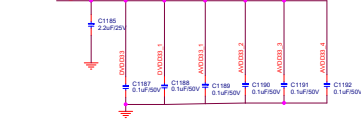


PCOM-POWER  
9-24V  
MCOM-GND

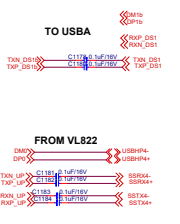
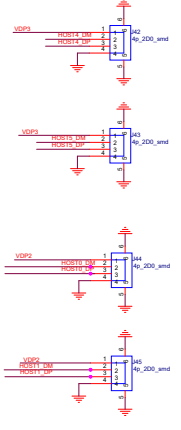
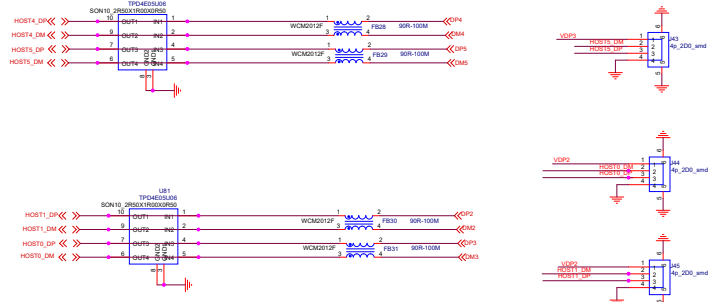
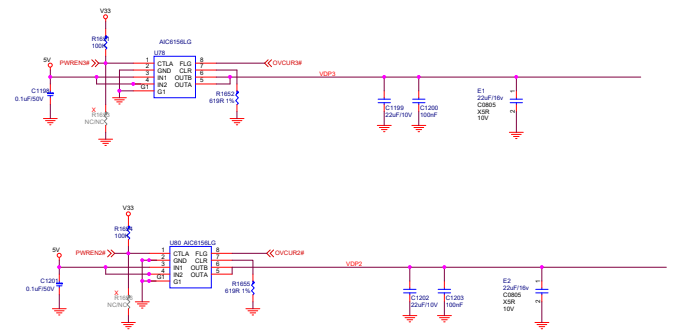


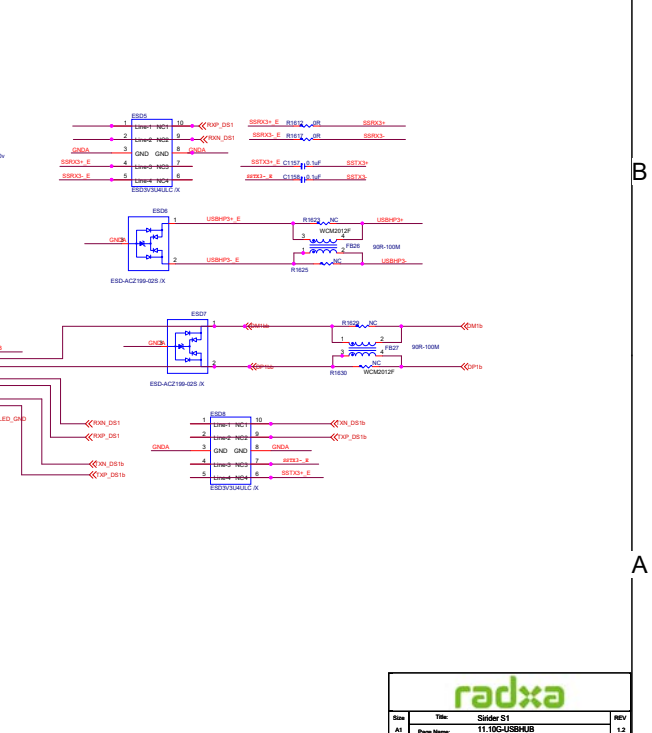
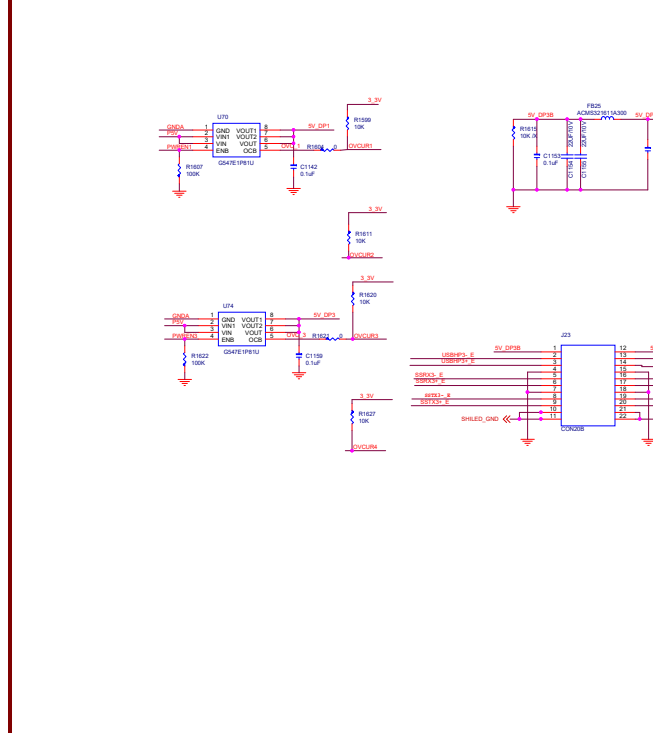
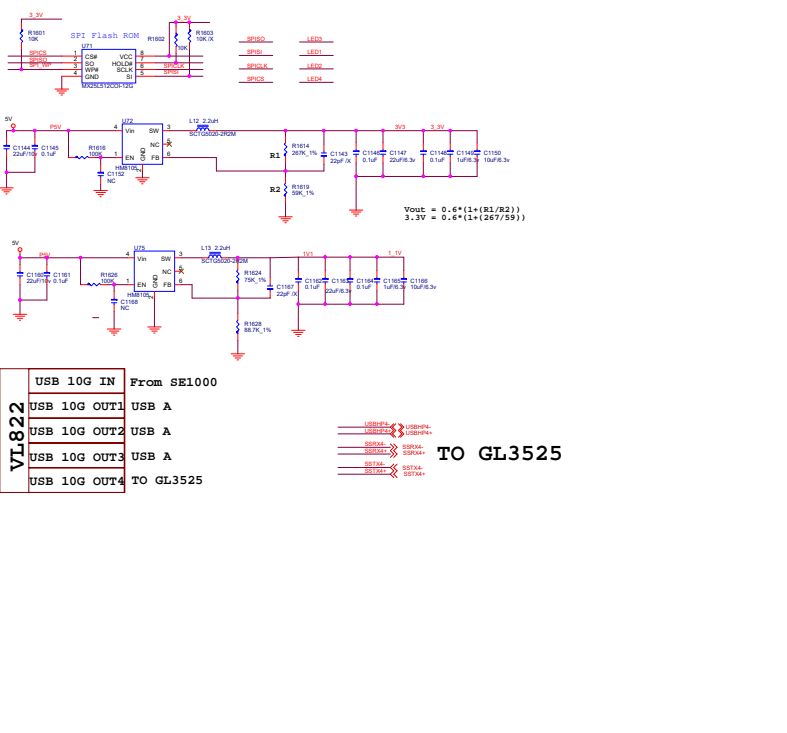
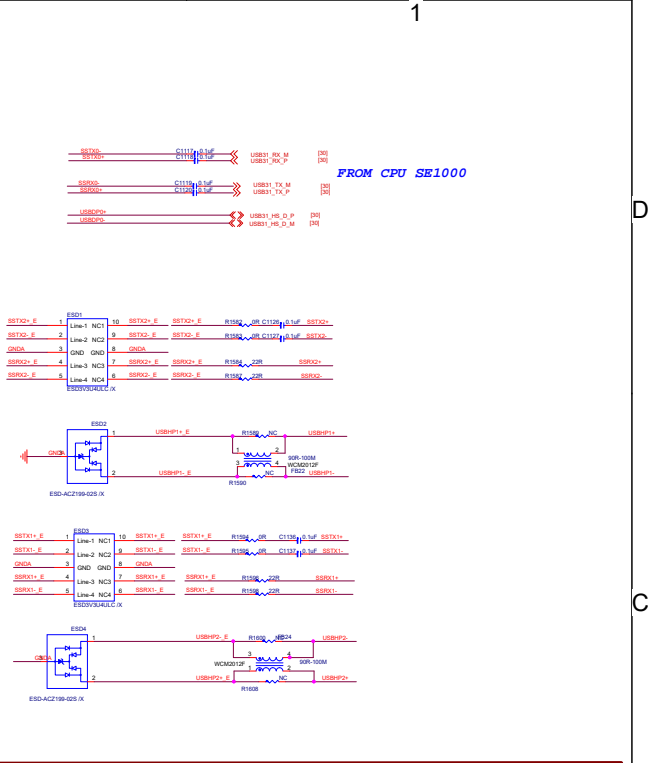
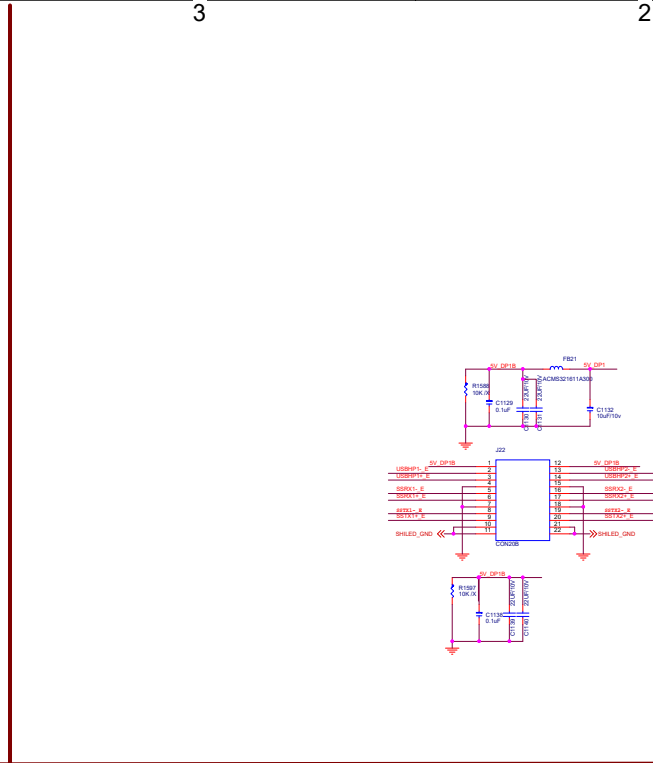
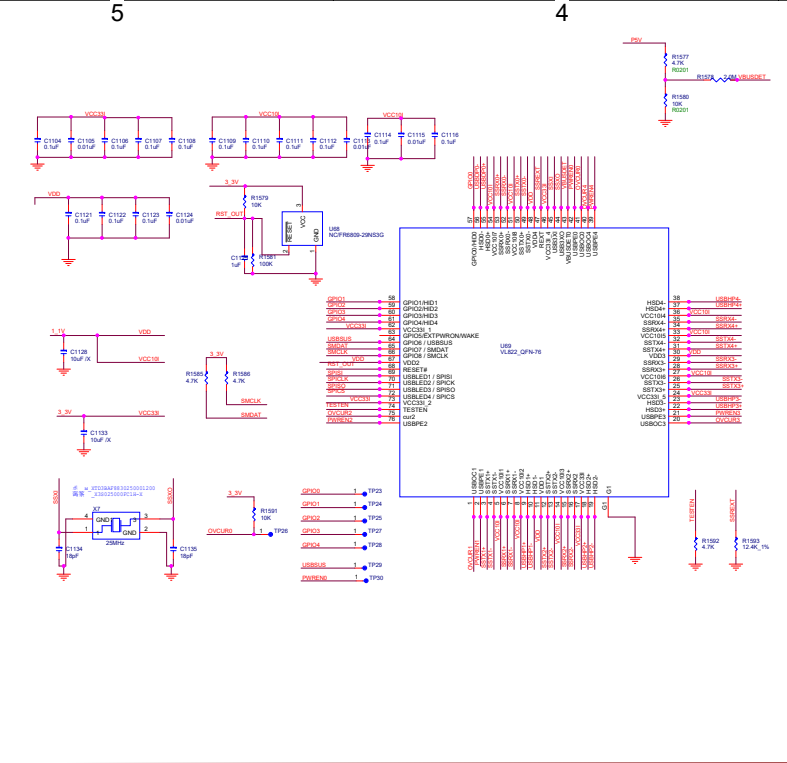


C20 close to pin29,  
C21 close to pin67.



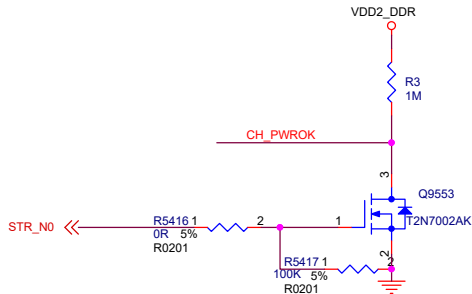
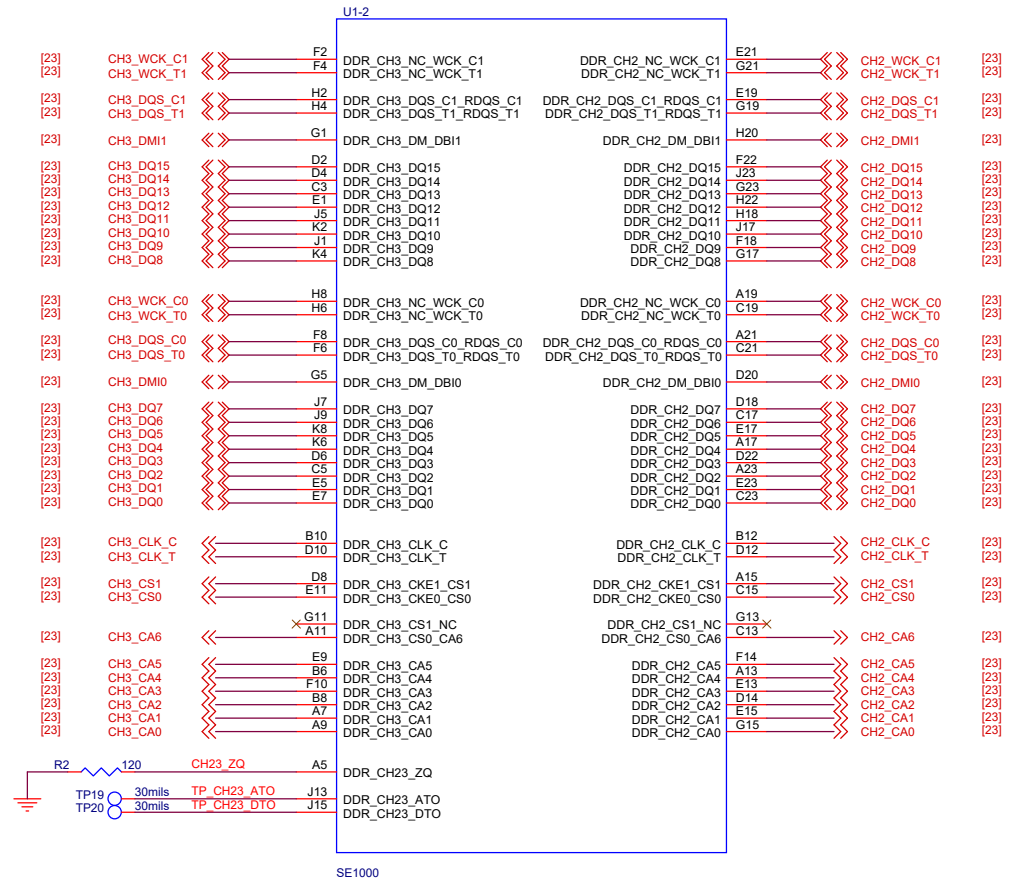
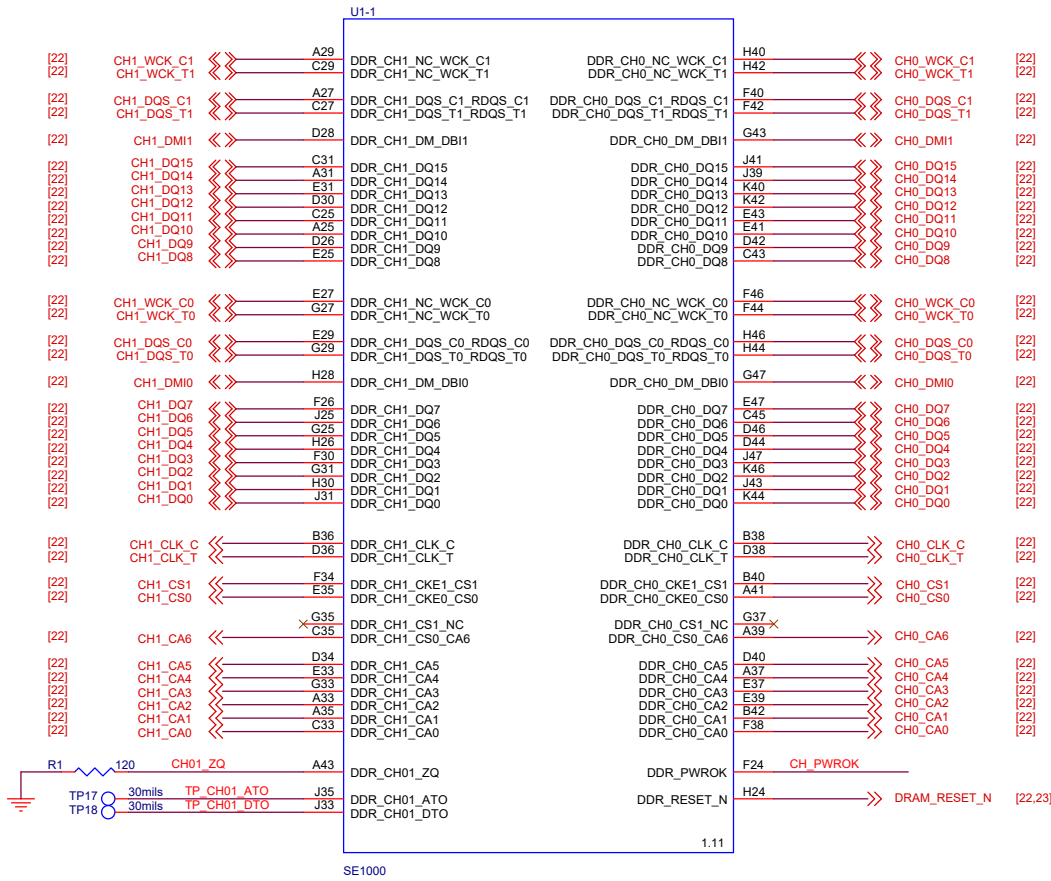
GL3525 QFN88 schematic  
USB3.1 Gen1 HUB

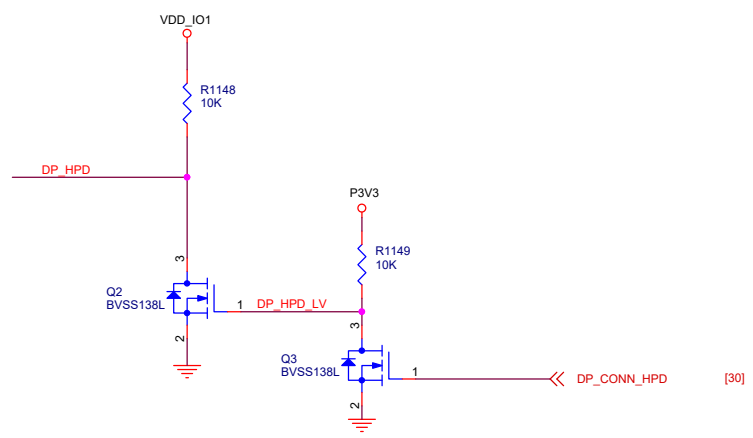
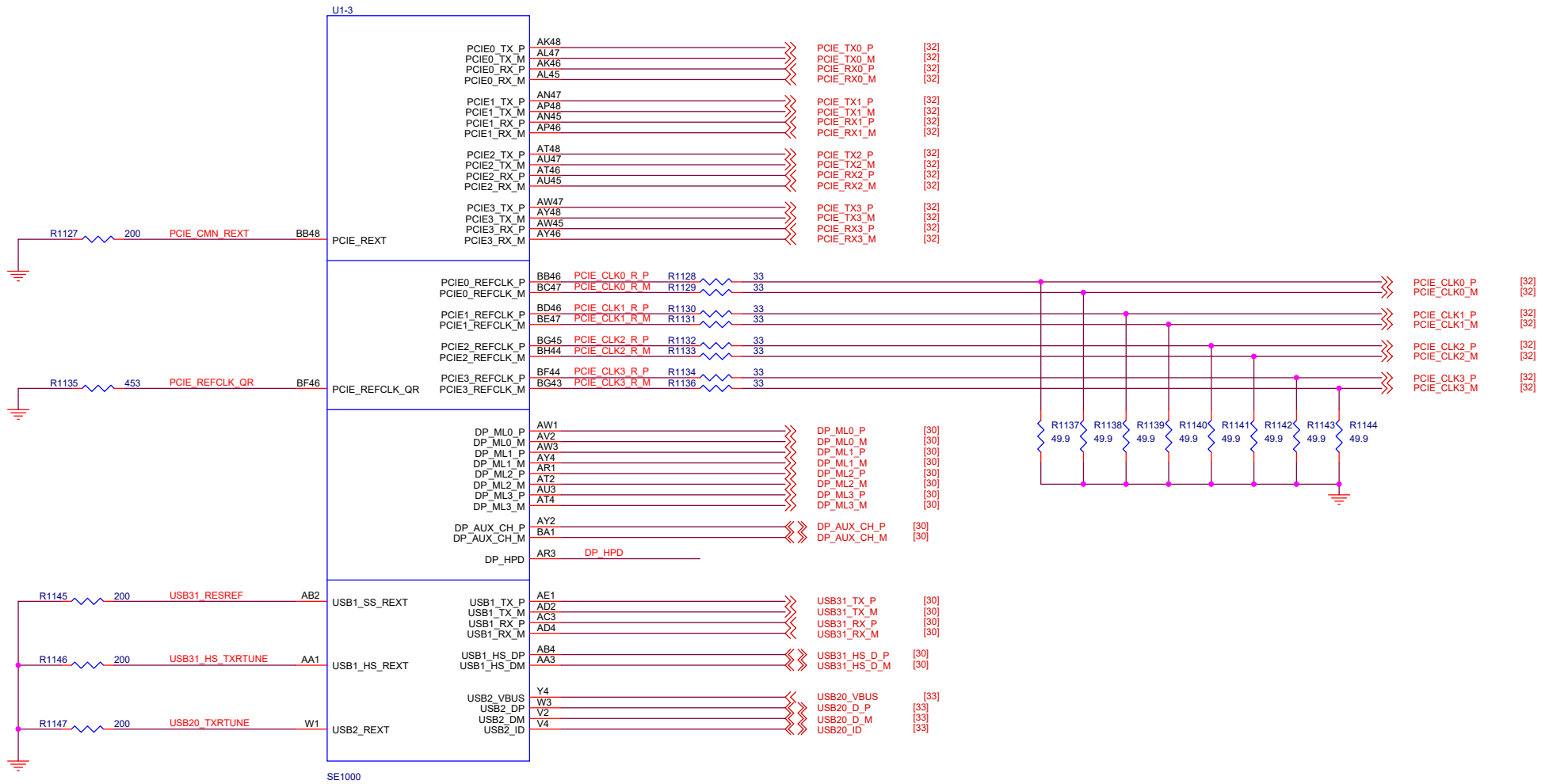




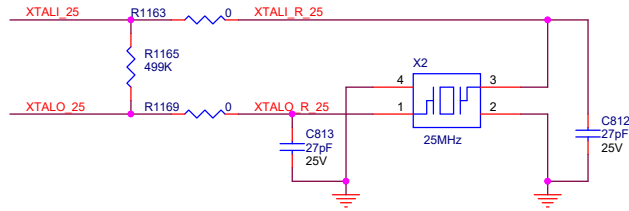
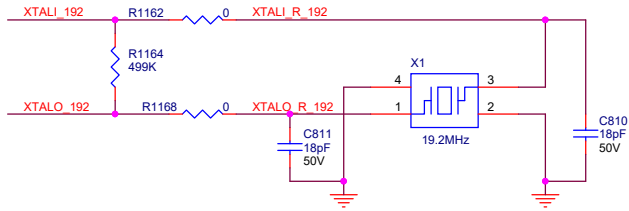
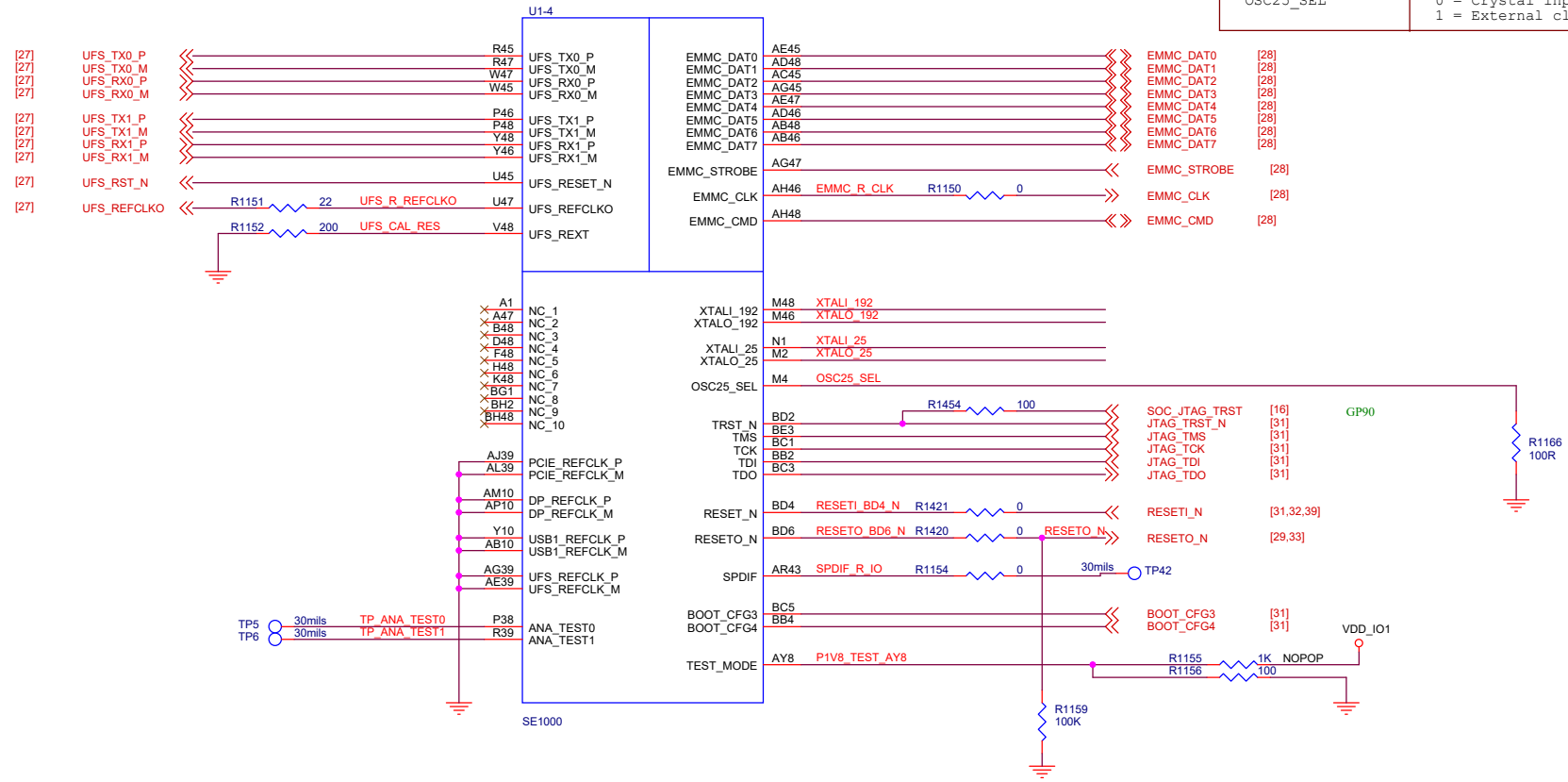
USB 10G IN	From SE1000
USB 10G OUT1	USB A
USB 10G OUT2	USB A
USB 10G OUT3	USB A
USB 10G OUT4	TO GL3525

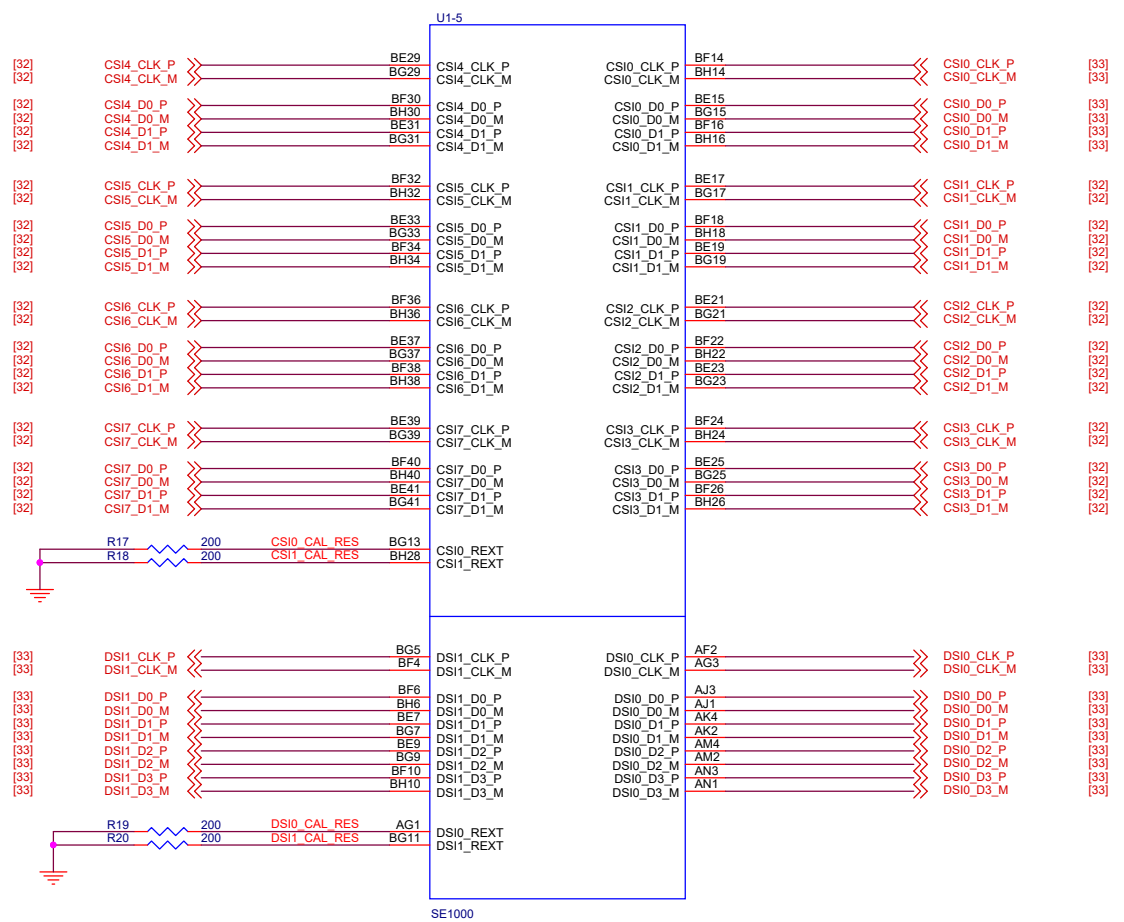
TO GL3525

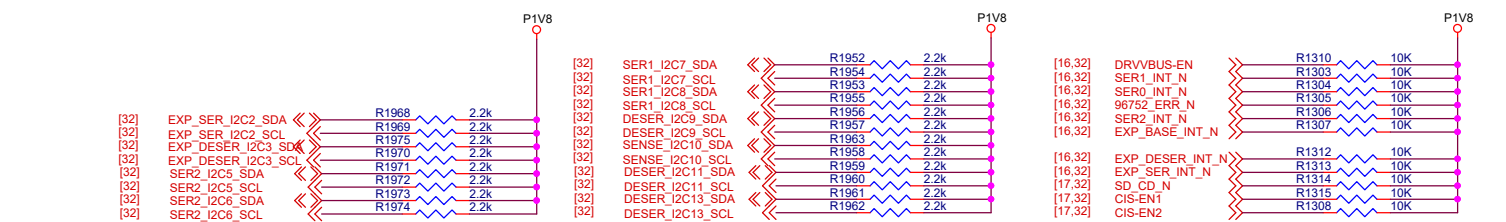




Strap Pin name	Description	Internal PU/PD
TEST_MODE	0 = Normal mode 1 = Test mode	N/A
OSC25_SEL	0 = Crystal input 1 = External clock input	N/A



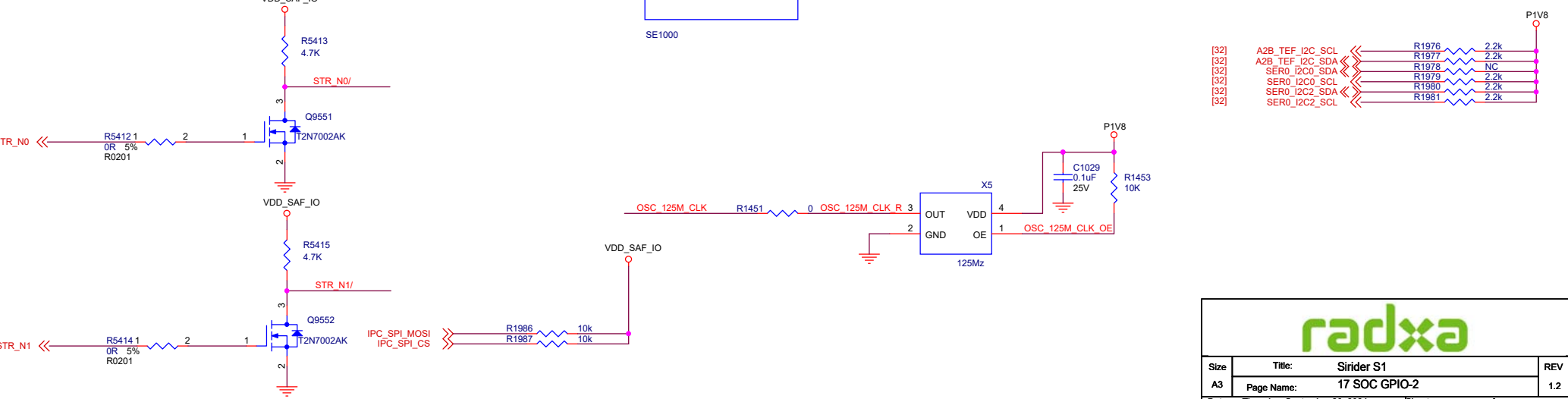
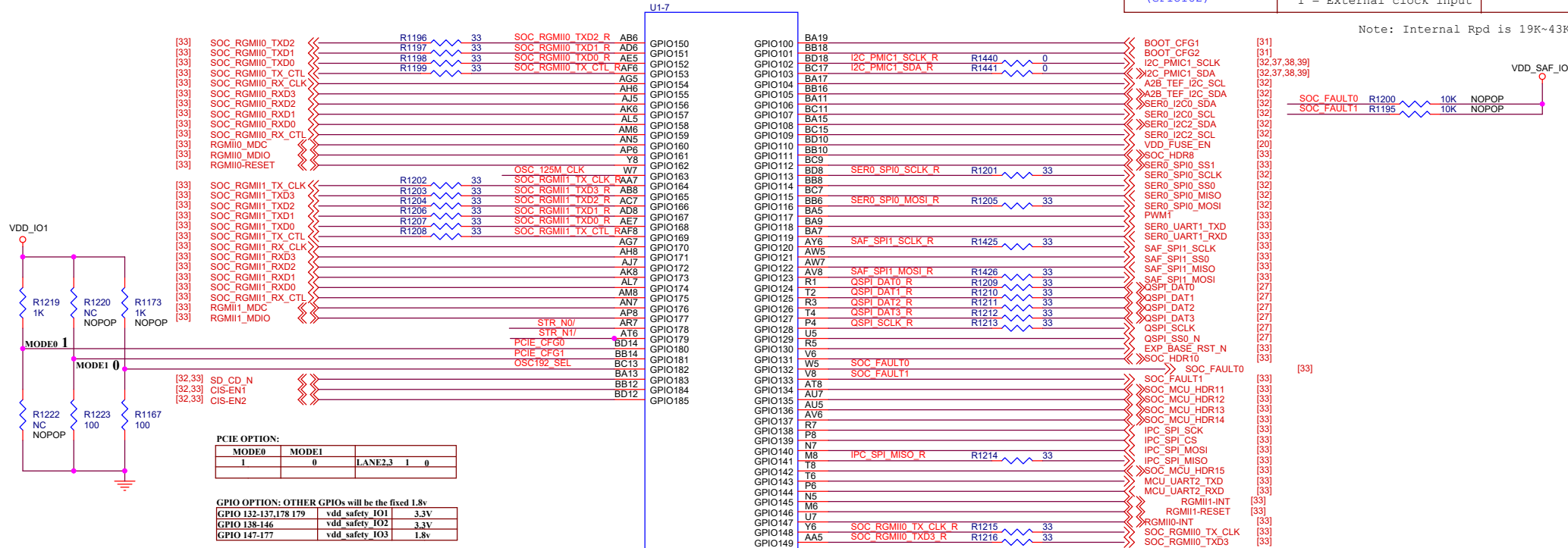






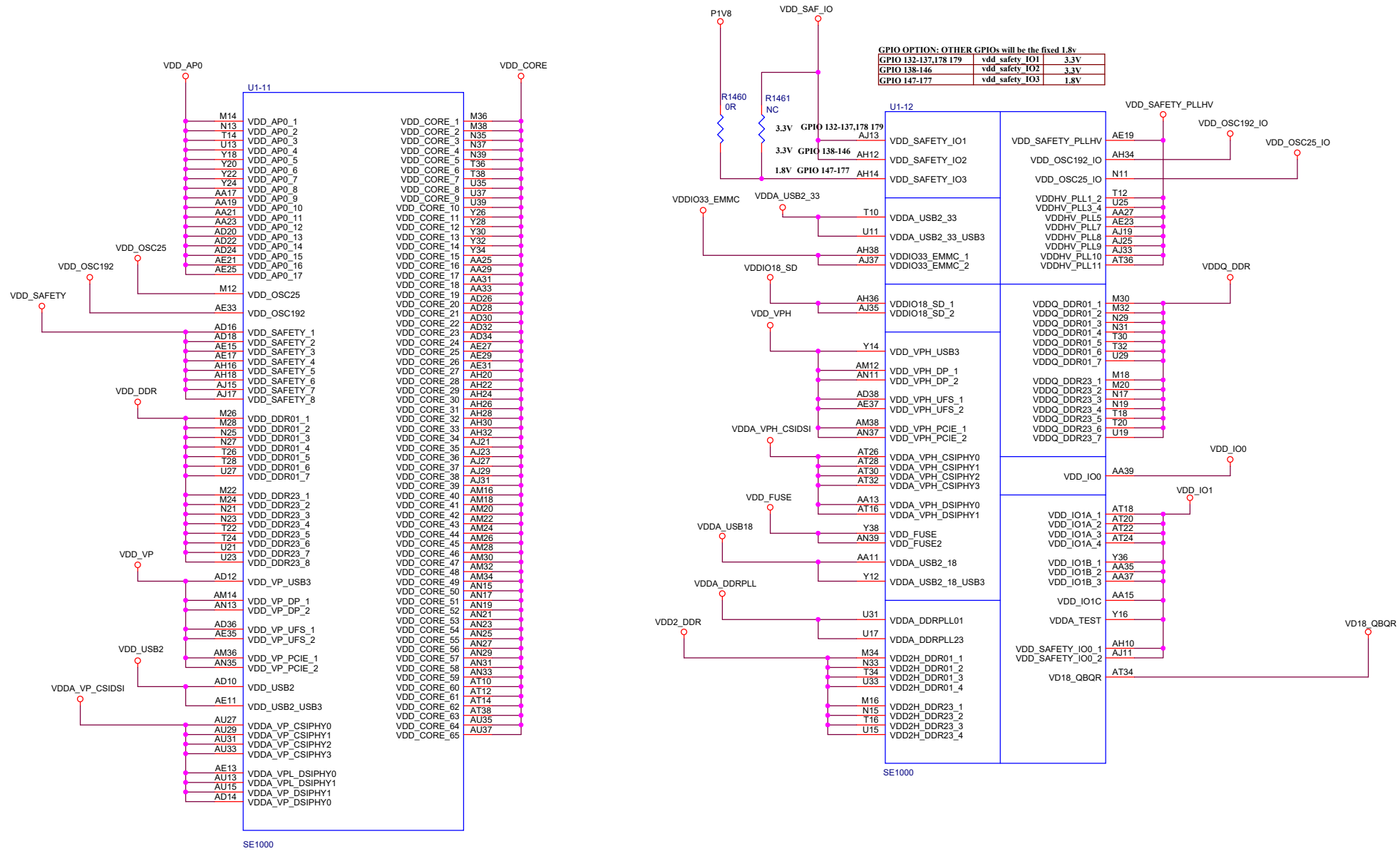
Strap Pin name	Description	Internal PU/PD
STR_N0 (GPIO178)	0 = STR boot 1 = Normal boot	PD
STR_N1 (GPIO179)	RSVD	PD
PCIE_CFG[1:0] (GPIO181/180)	Mode = Lane[3:0] 00 = x2, x2 01 = x2, x1, x1 10 = x1, x1, x2 11 = x1, x1, x1, x1	N/A
OSC192_SEL (GPIO182)	0 = Crystal input 1 = External clock input	PD

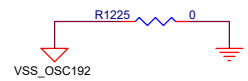
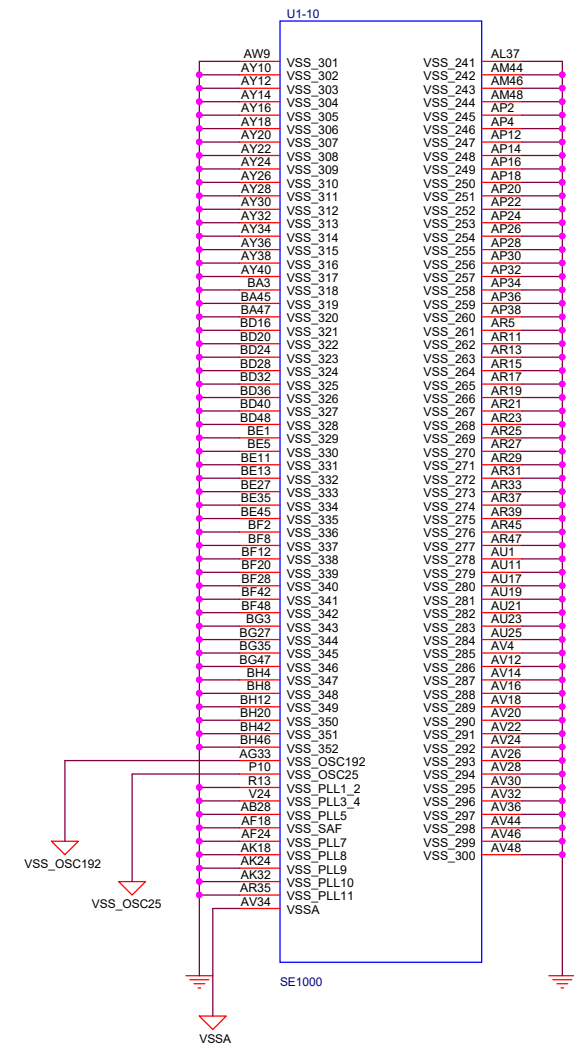
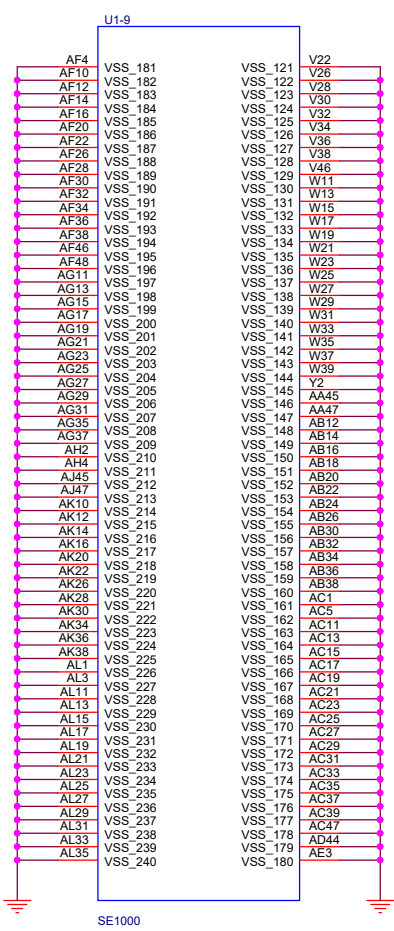
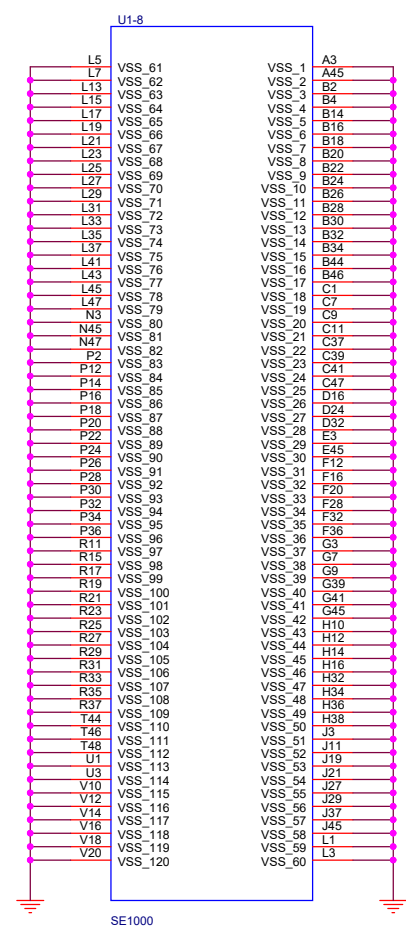
Note: Internal Rpd is 19K-43K.

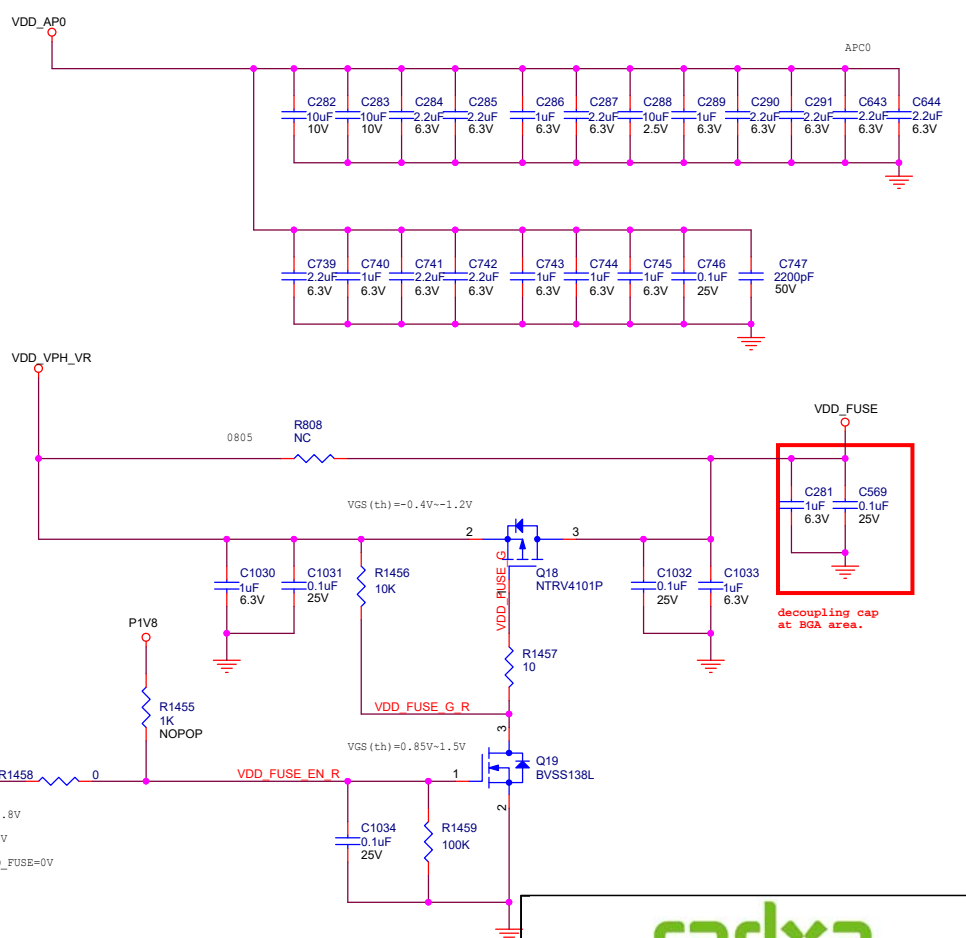
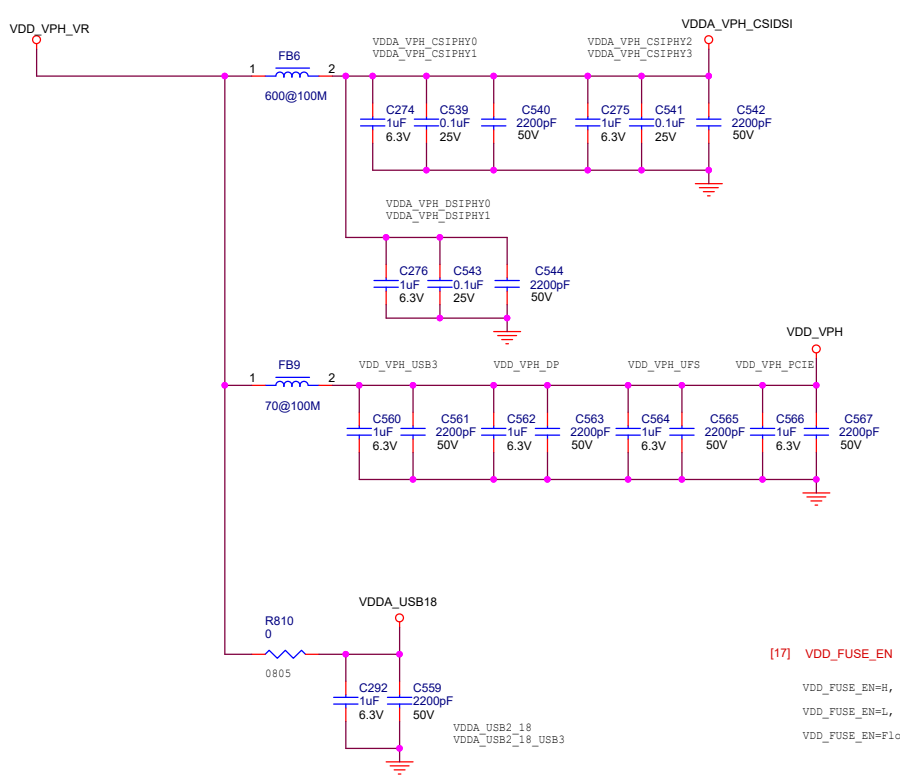
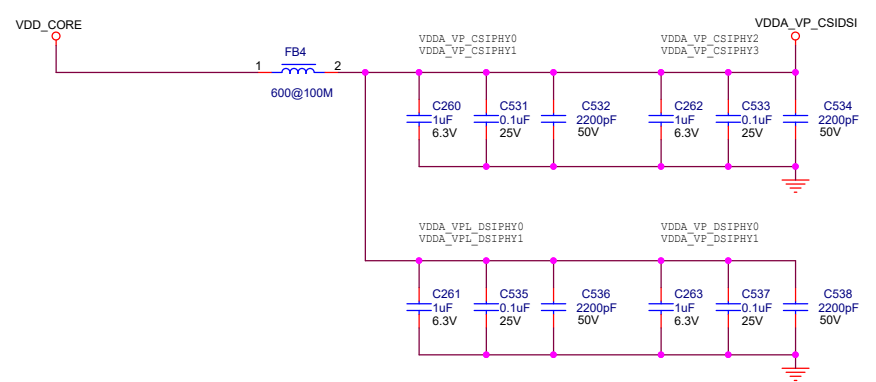
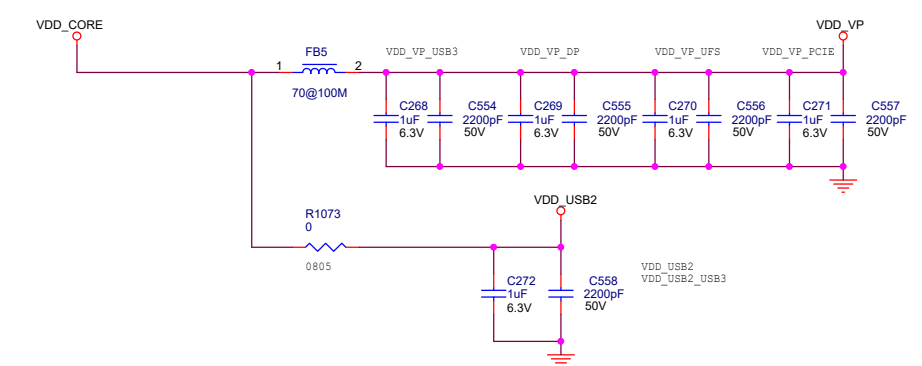


**radxa**

Size	Title: Sirider S1	REV
A3	Page Name: 17 SOC GPIO-2	1.2
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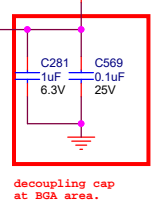




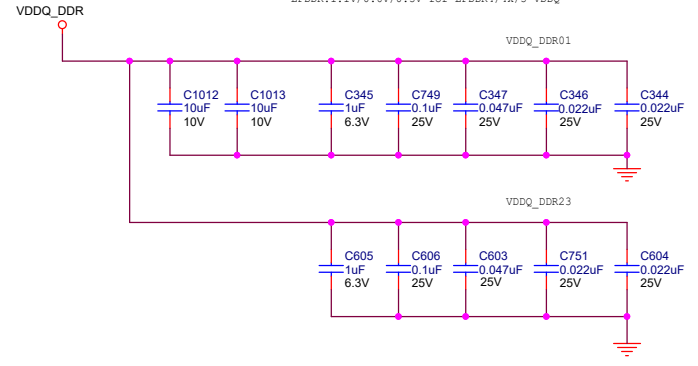
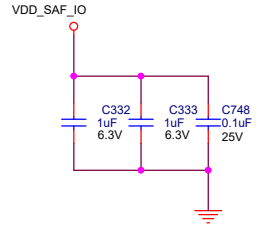
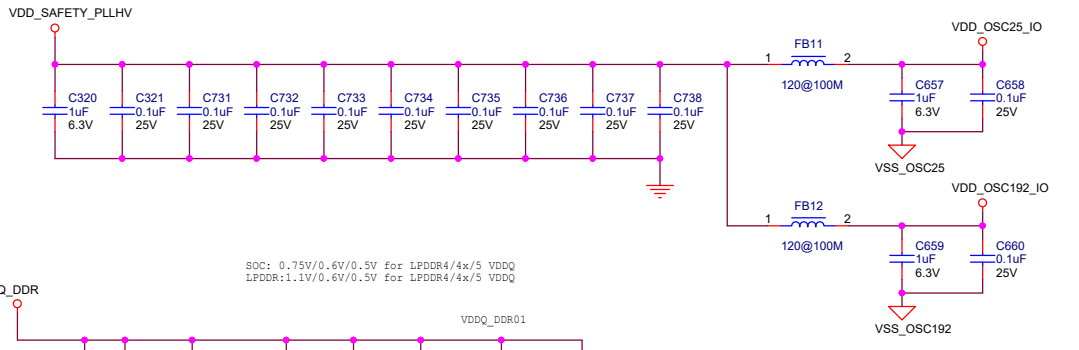
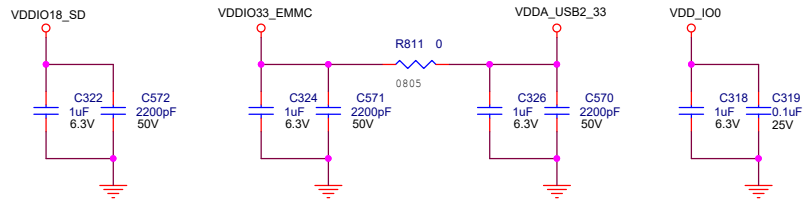


[17] VDD\_FUSE\_EN >>> R1458 0

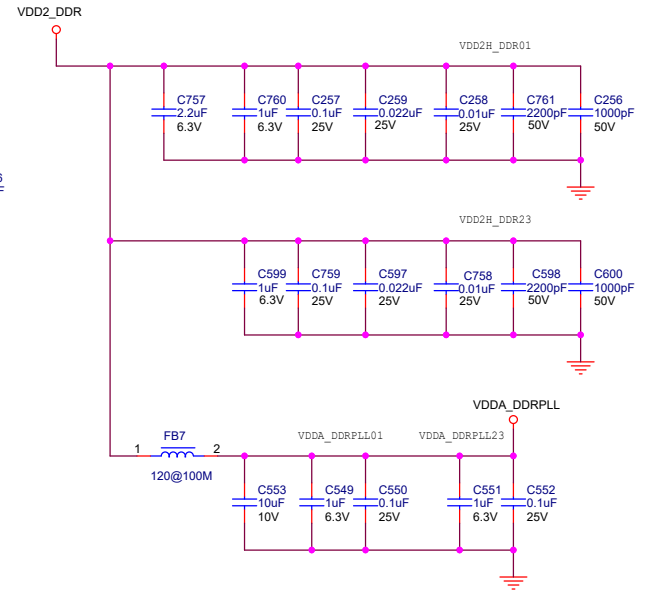
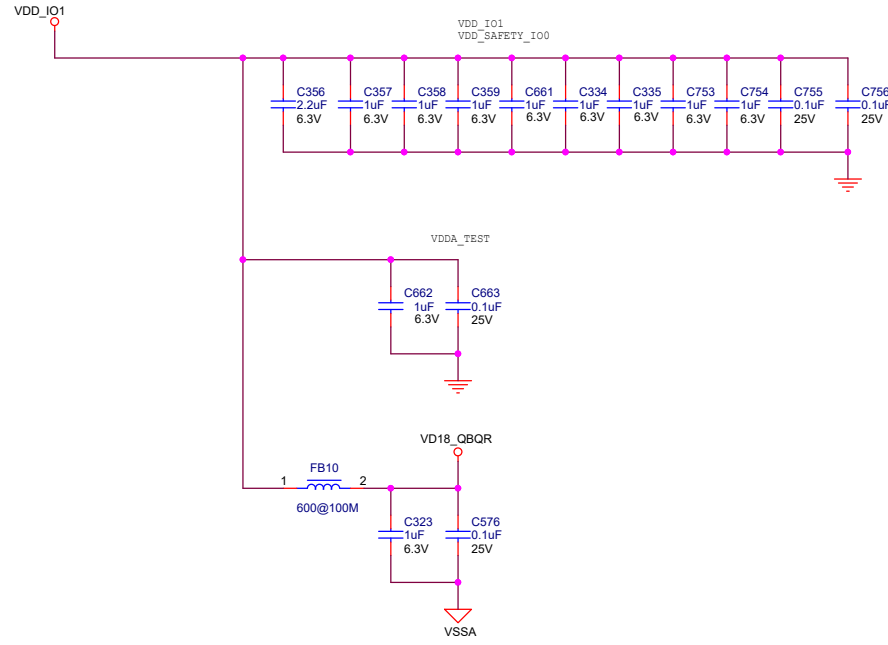
VDD\_FUSE\_EN=H, VDD\_FUSE=1.8V  
 VDD\_FUSE\_EN=L, VDD\_FUSE=0V  
 VDD\_FUSE\_EN=Floating, VDD\_FUSE=0V

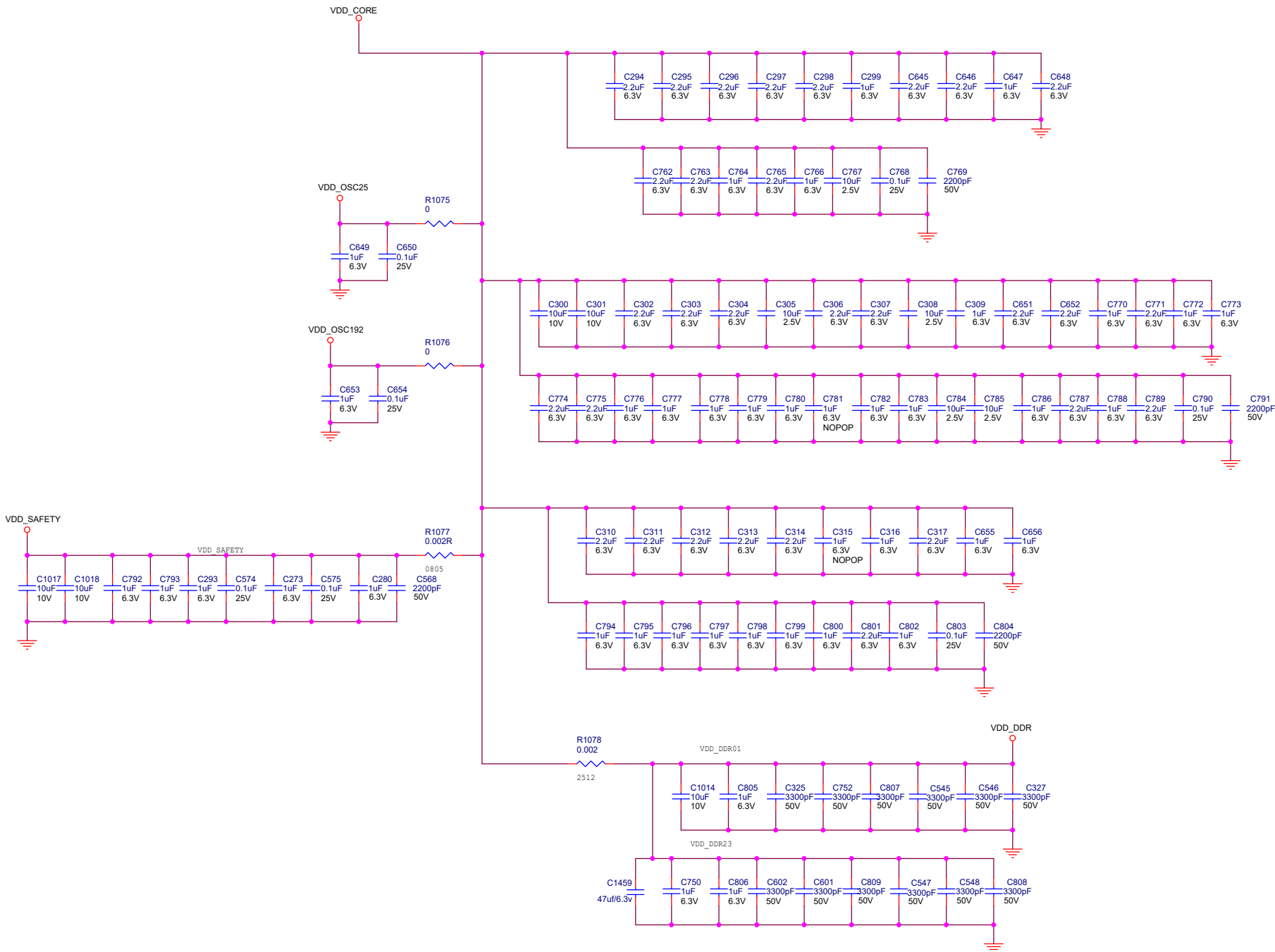


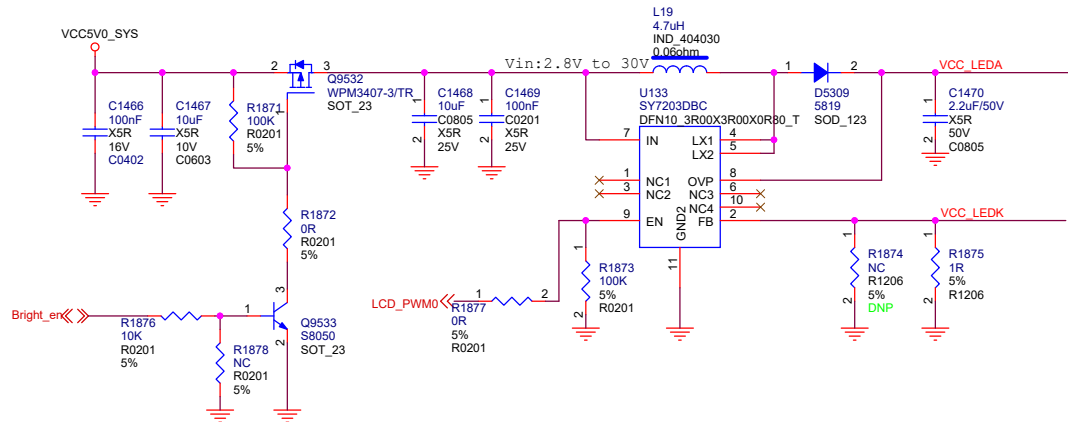
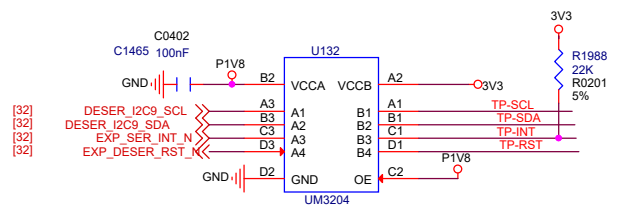
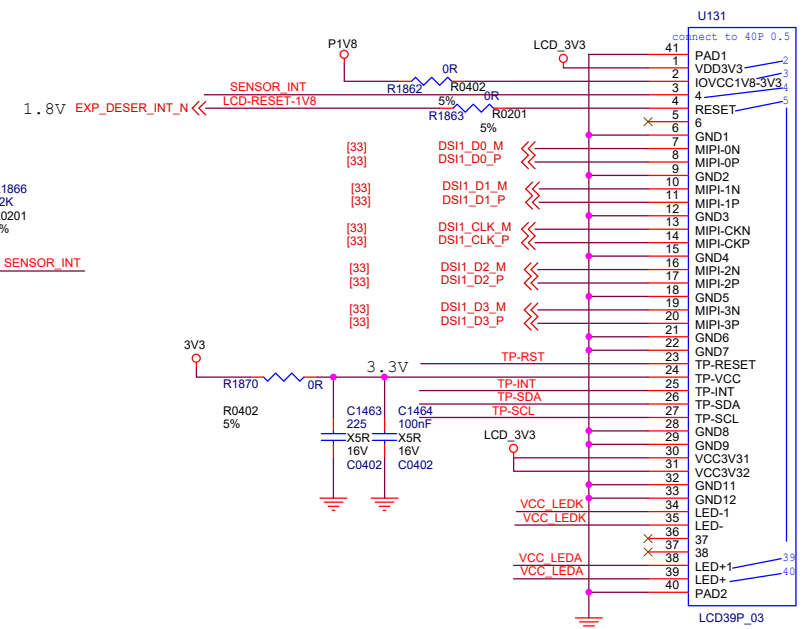
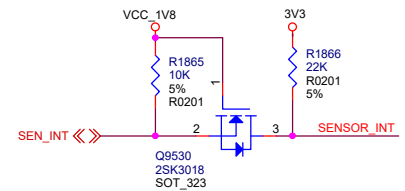
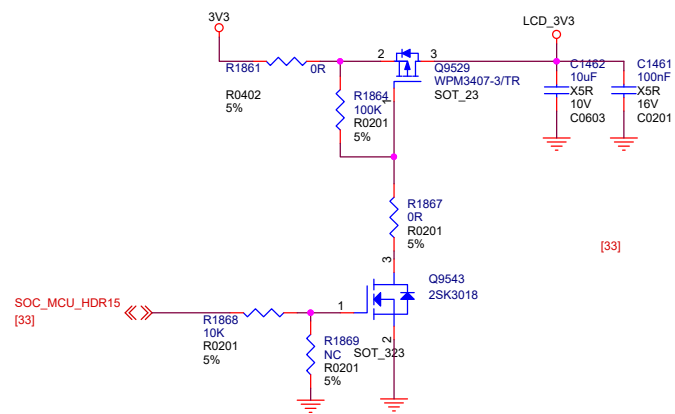
Note:  
 1 The caps used here are for reference only.  
 2 Capacitor with smallest capacitance value should be placed as close as possible to package power and ground pins.



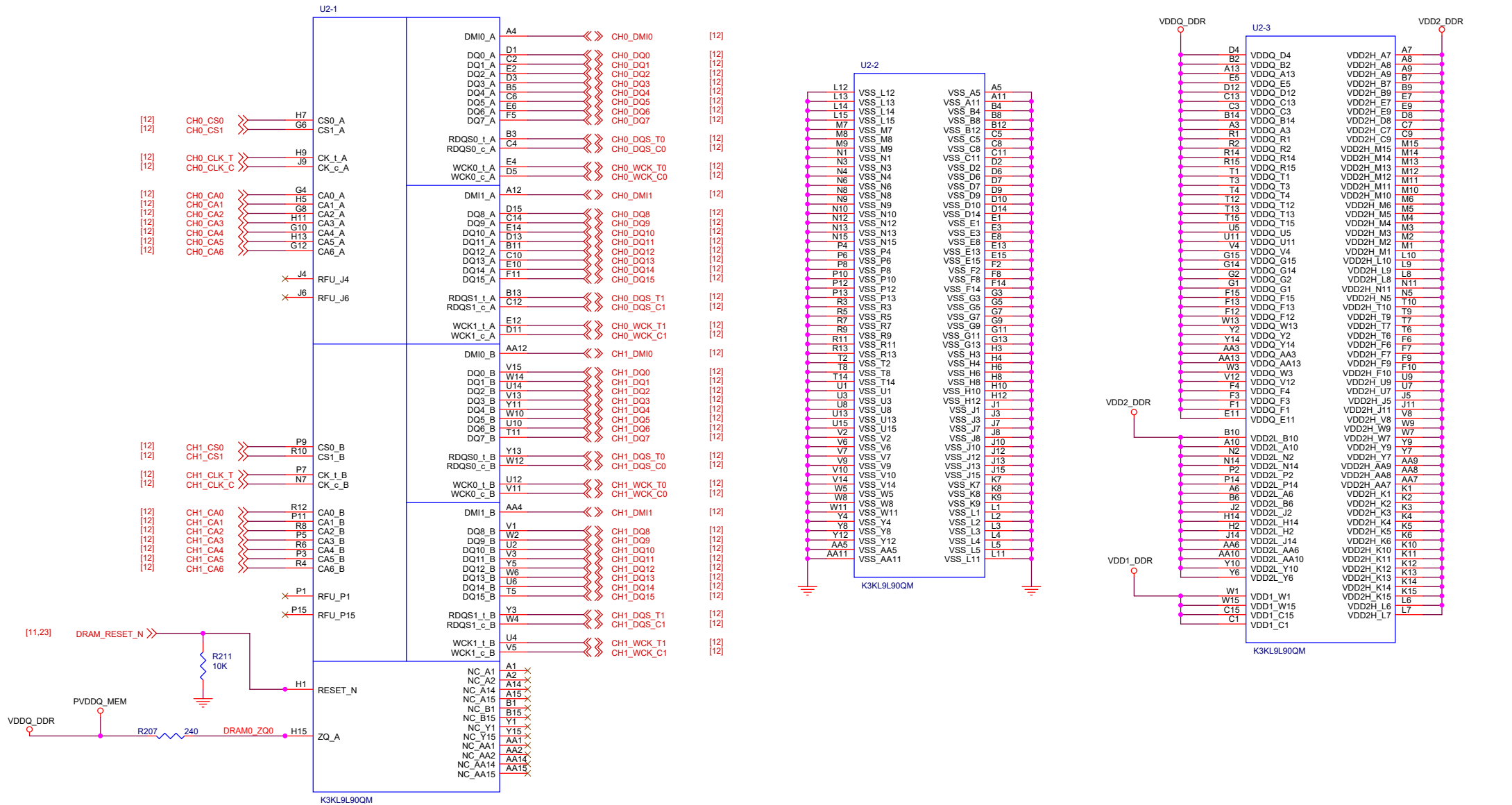
SOC: 0.75V/0.6V/0.5V for LPDDR4/4x/5 VDDQ  
 LPDDR: 1.1V/0.6V/0.5V for LPDDR4/4x/5 VDDQ





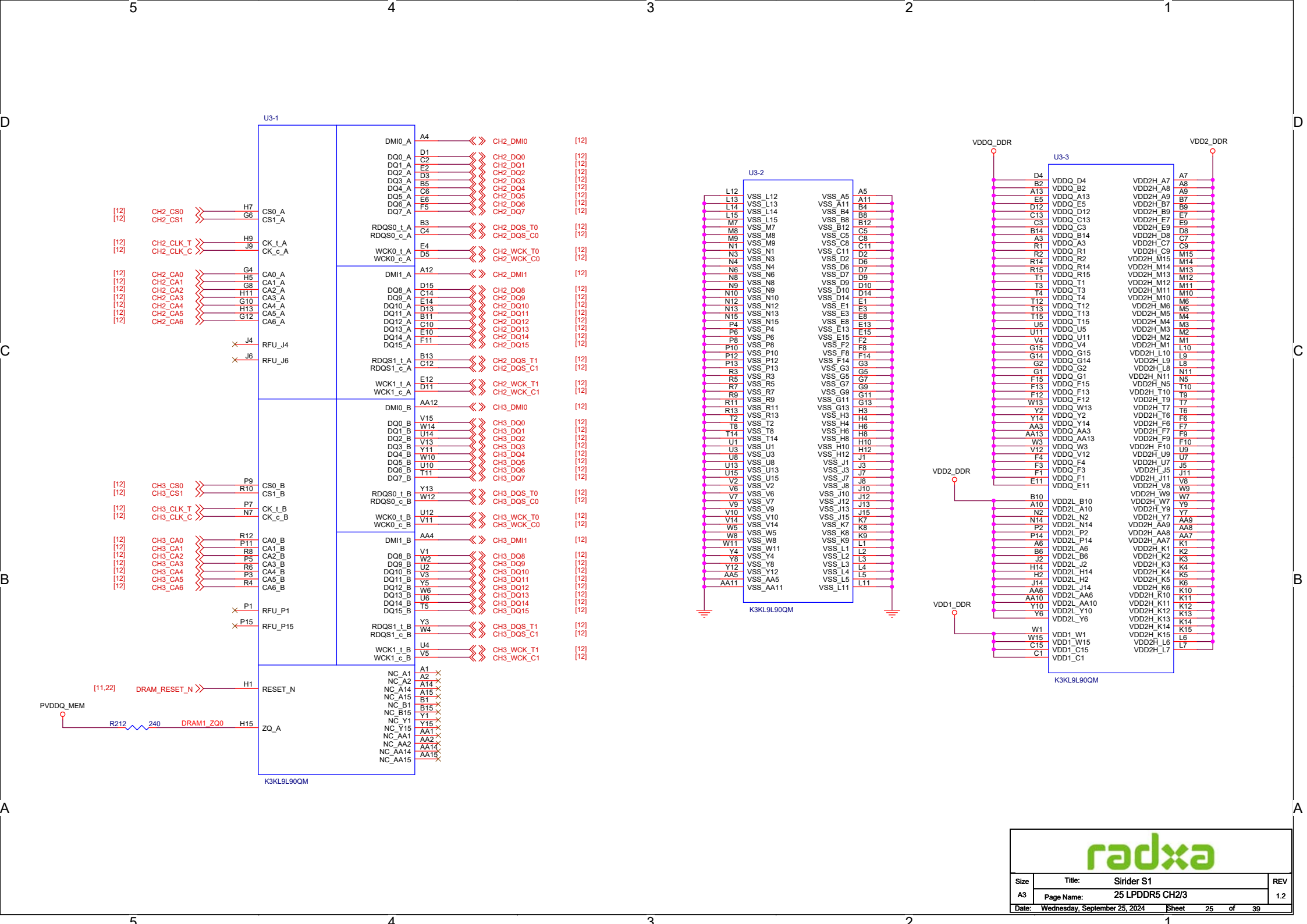


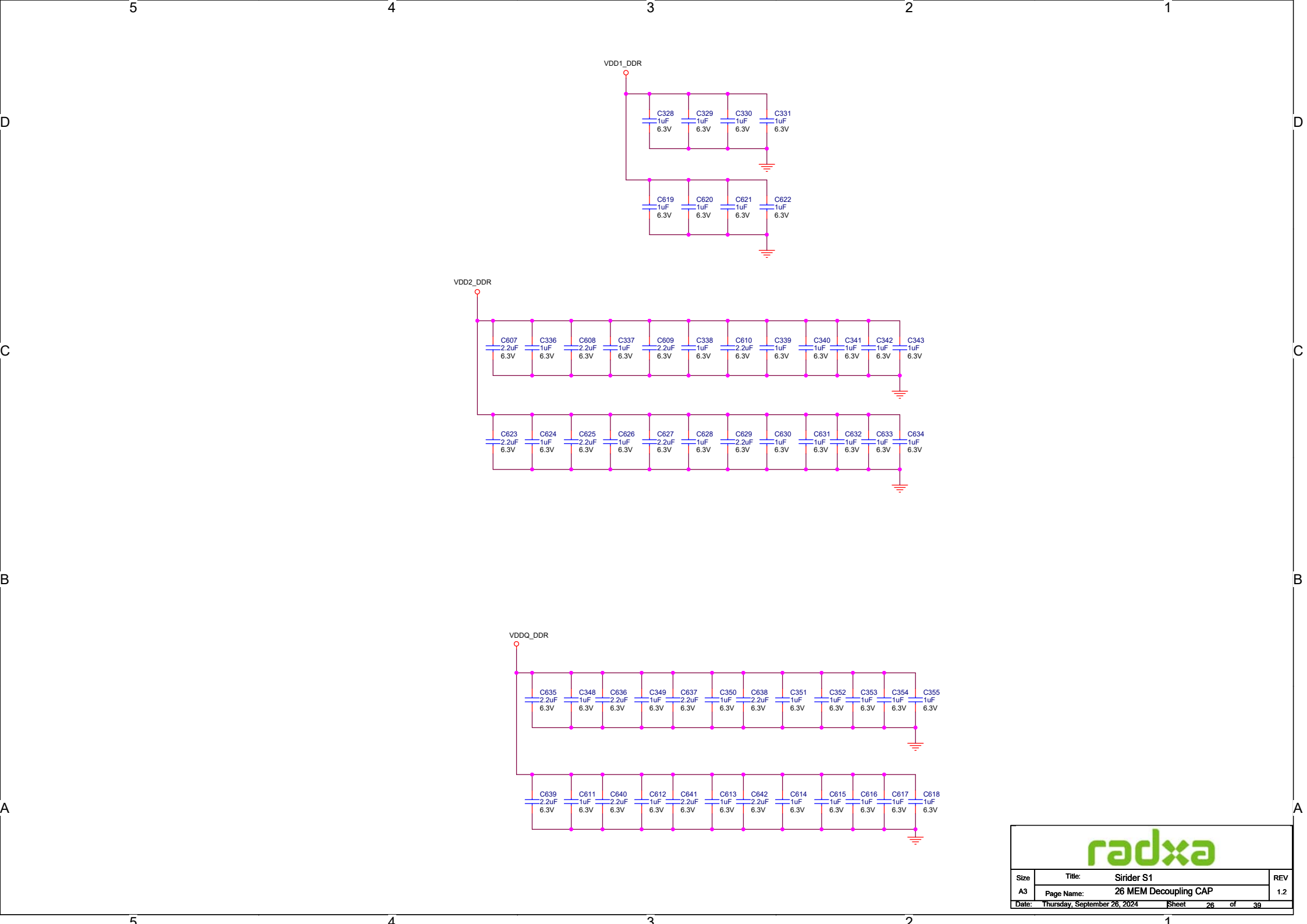
# LCD



Size	Title:	Sirider S1	REV
A3	Page Name:	24 LPDDR5 CH0/1	1.2
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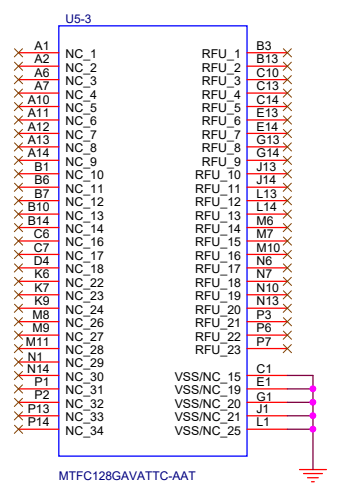
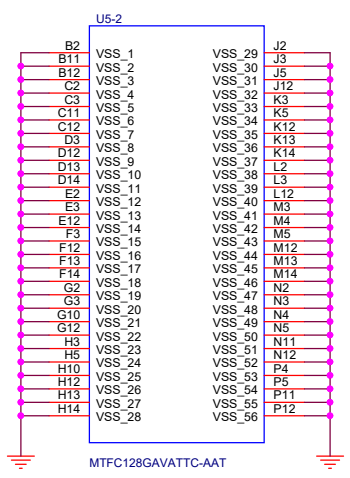
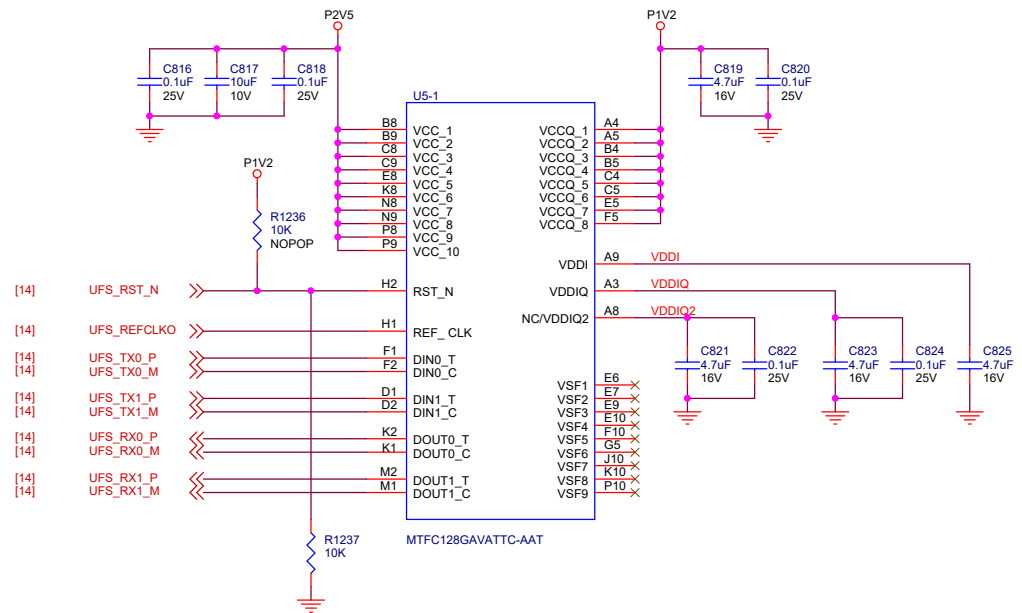


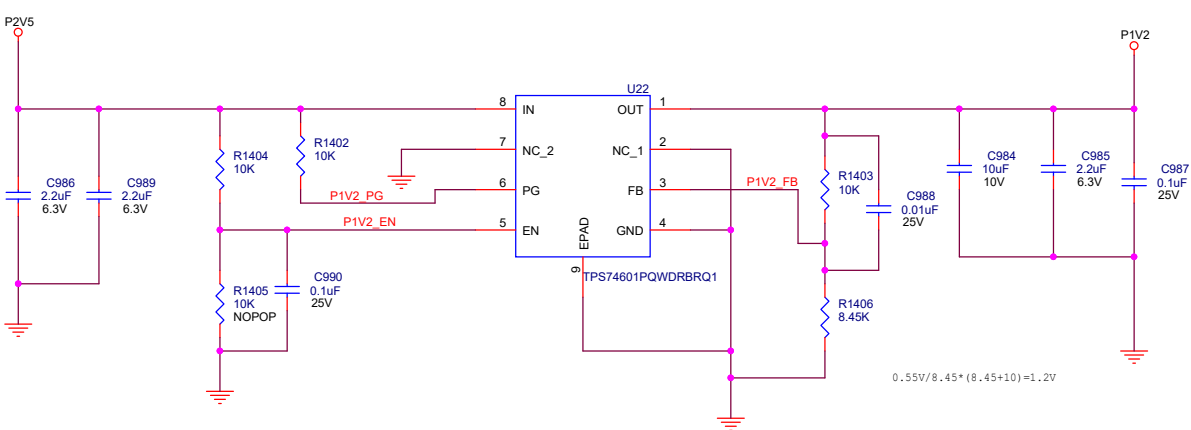
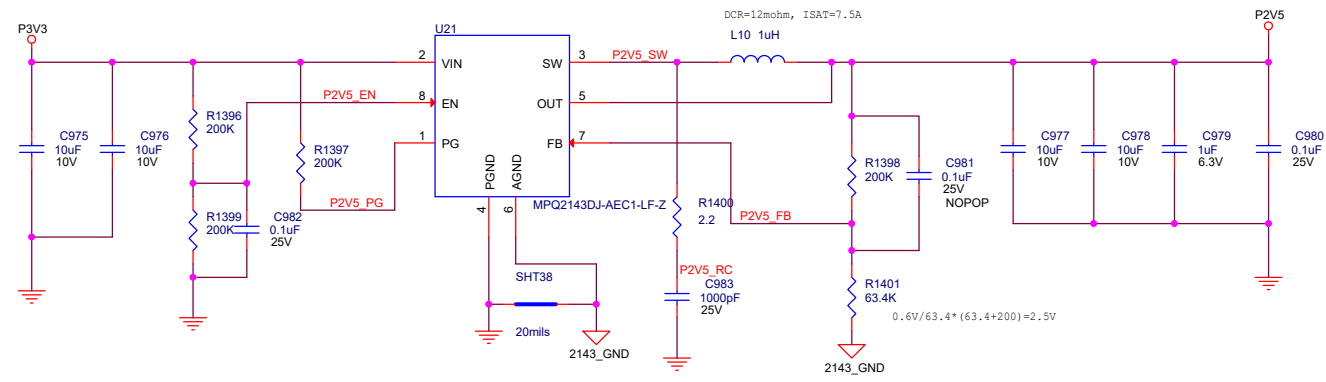




Size	Title: Sirider S1	REV
A3	Page Name: 26 MEM Decoupling CAP	1.2
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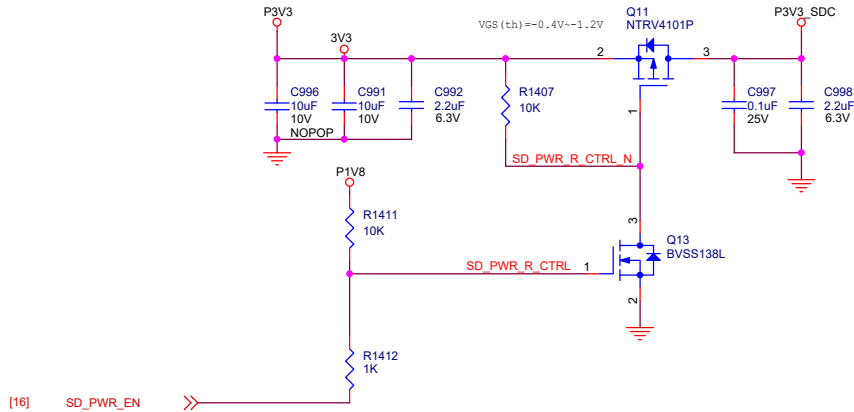
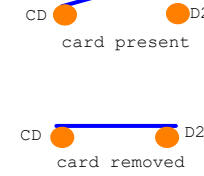
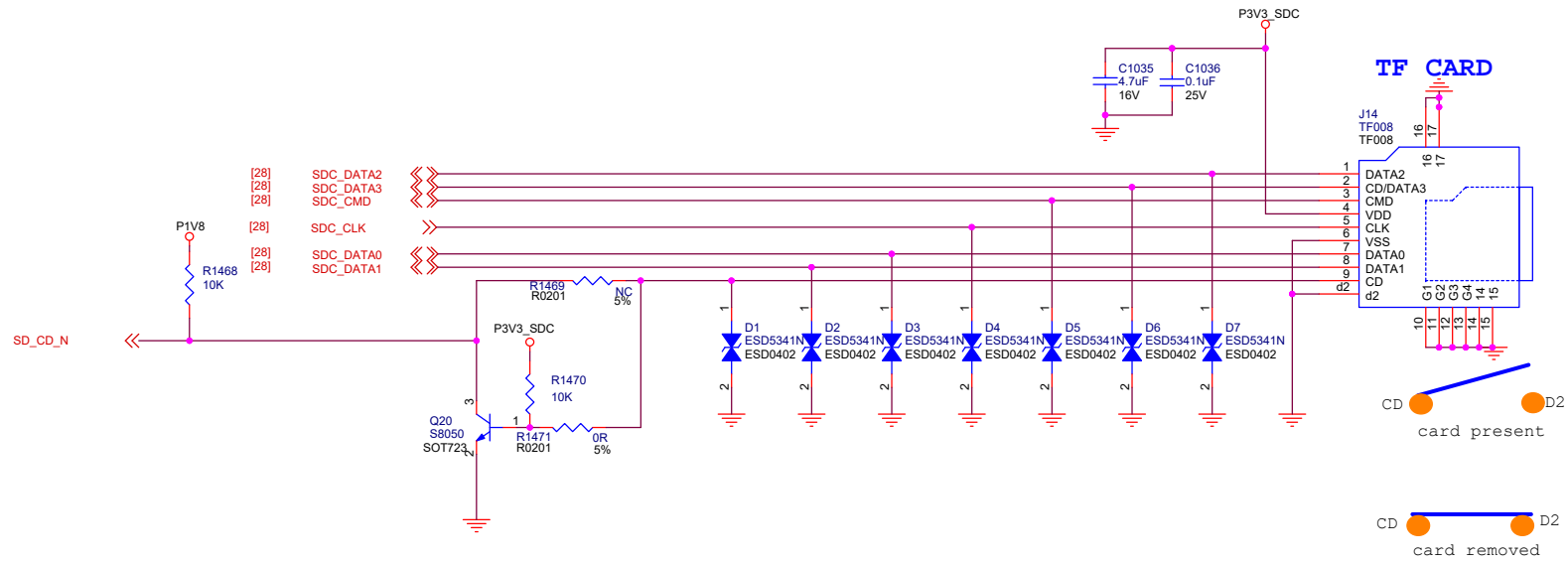
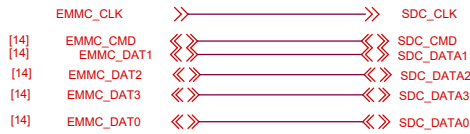
# UFS



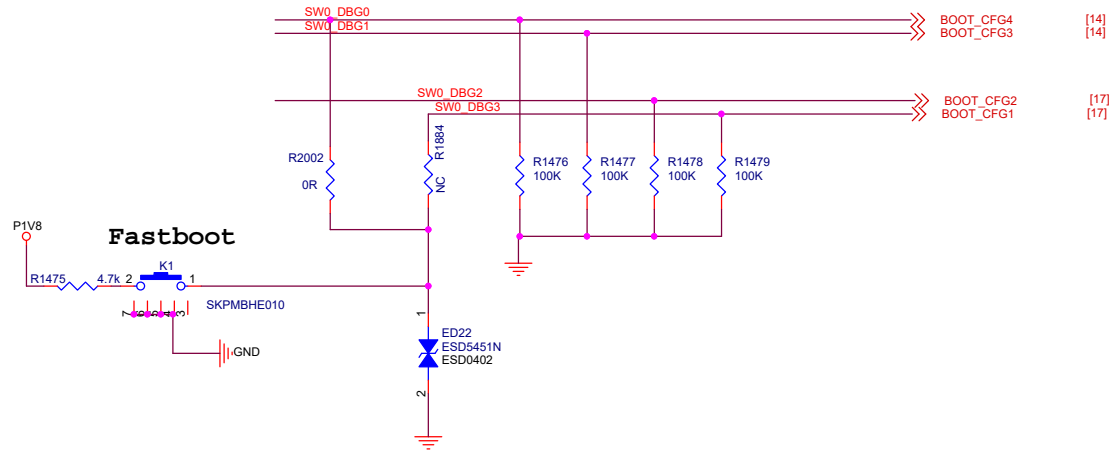


If purchased TPS74601, Please NOPOP MAX25301A/B related circuit  
 If purchased MAX25301A/B, Please NOPOP TPS74601 related circuit

PN	RA1	RA2	RB1	RB2	RF1	RF2
MAX25301A	NOPOP	NOPOP	POP	NOPOP	POP	NOPOP
MAX25301B	NOPOP	POP	10K	NOPOP	10.2K	POP

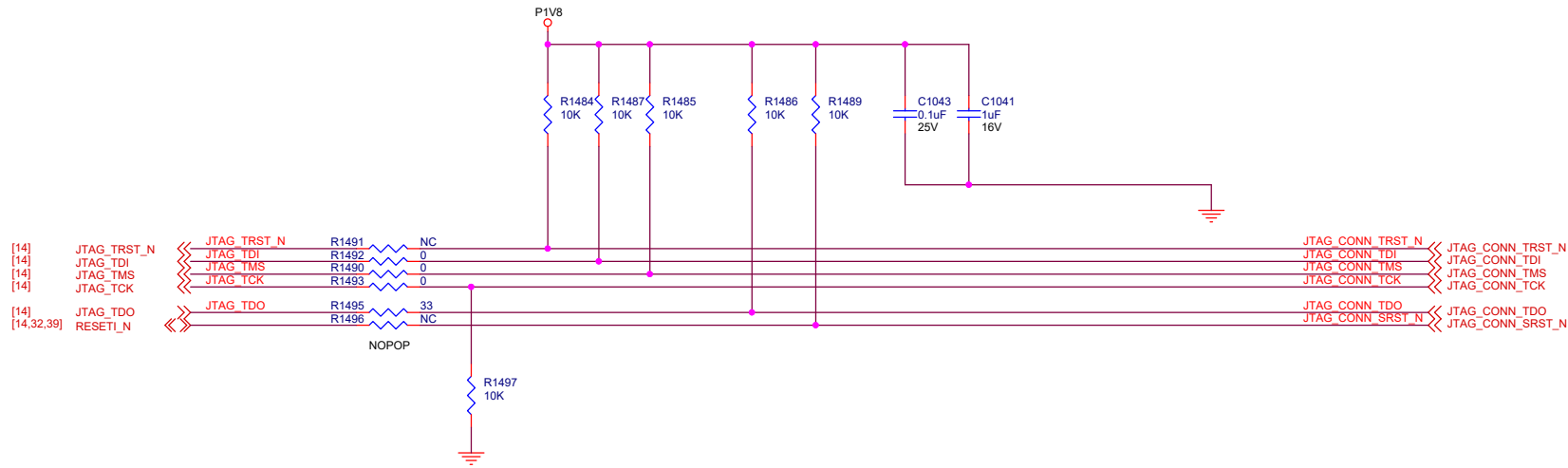


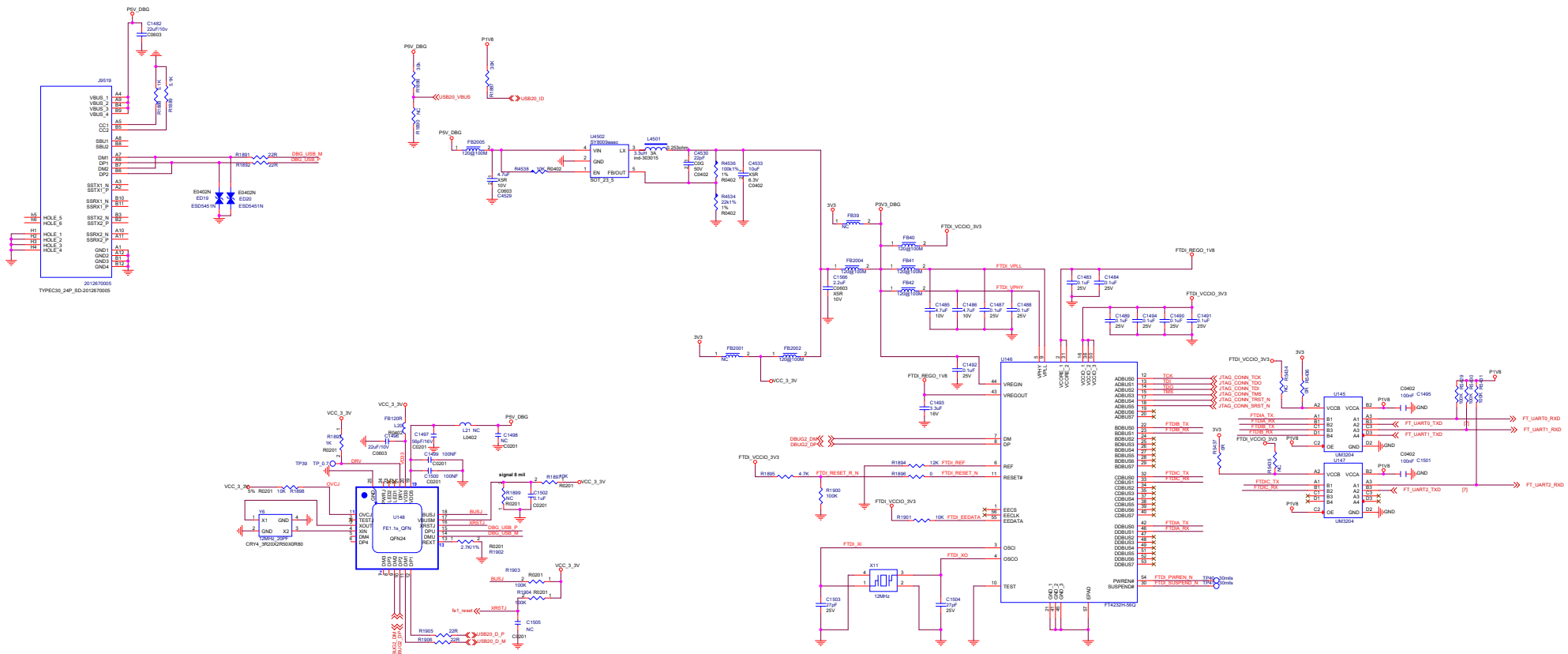




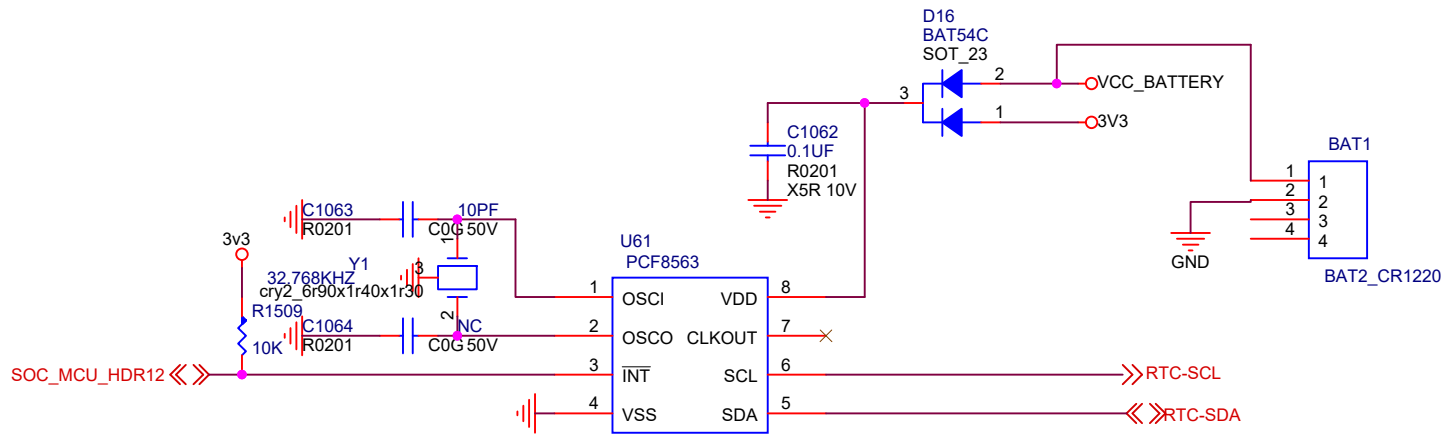
Strap Pin name	Description	Internal PU/PD
BOOT_CFG4	0 = Normal boot 1 = Rescue boot	PD
BOOT_CFG3	0 = UFS boot 1 = eMMC boot	PD
BOOT_CFG2 (GPIO101)	Secure boot enablement 0 = Open boot 1 = Secure boot	PD
BOOT_CFG1 (GPIO100)	Fastboot enablement 0 = Disable 1 = Enable	PD

Note: Internal Rpu is 19K~46K; Rpd is 19K~43K.

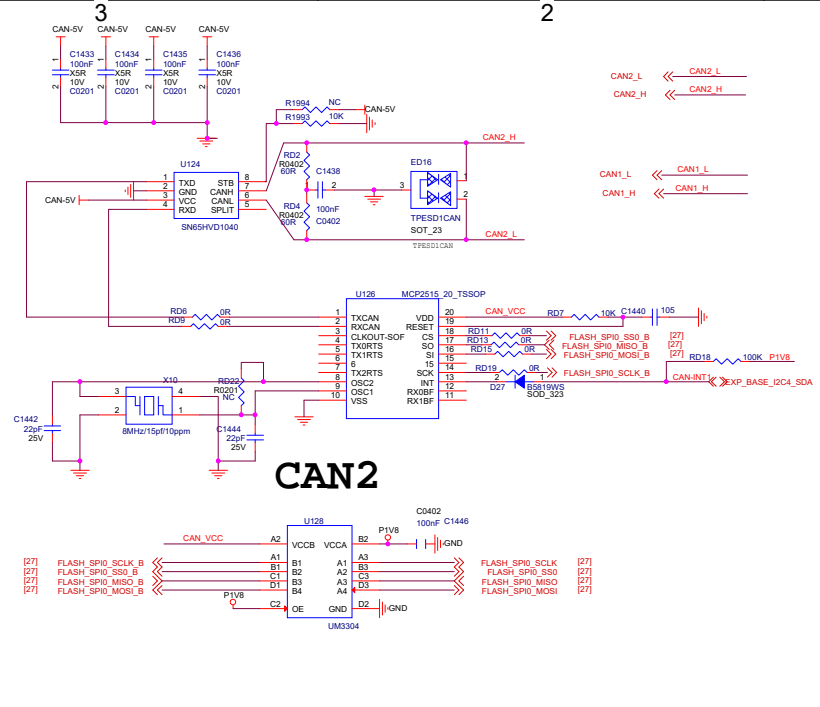
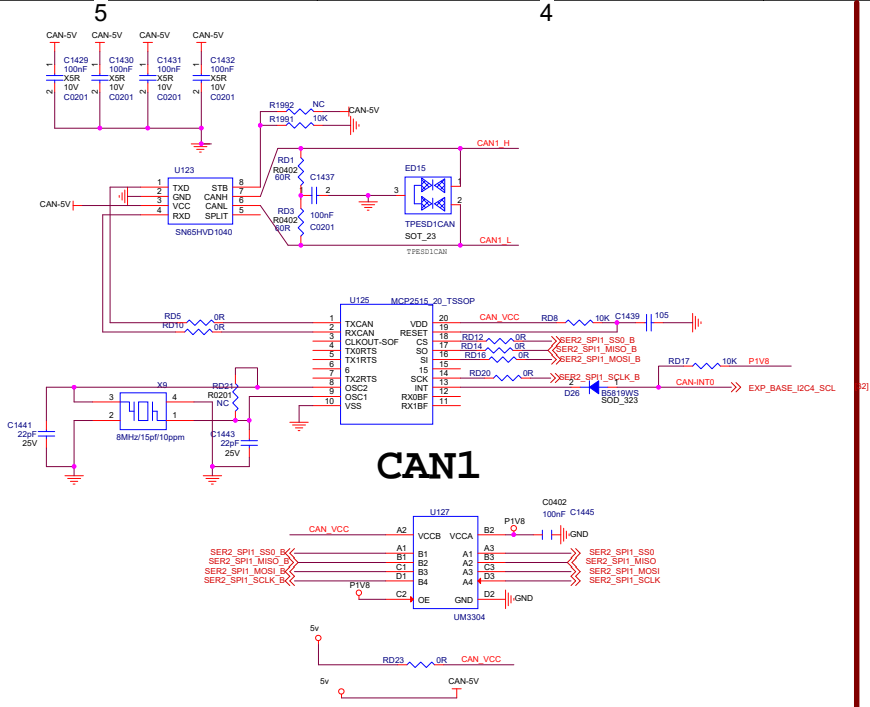




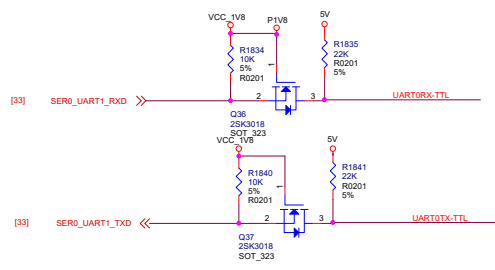




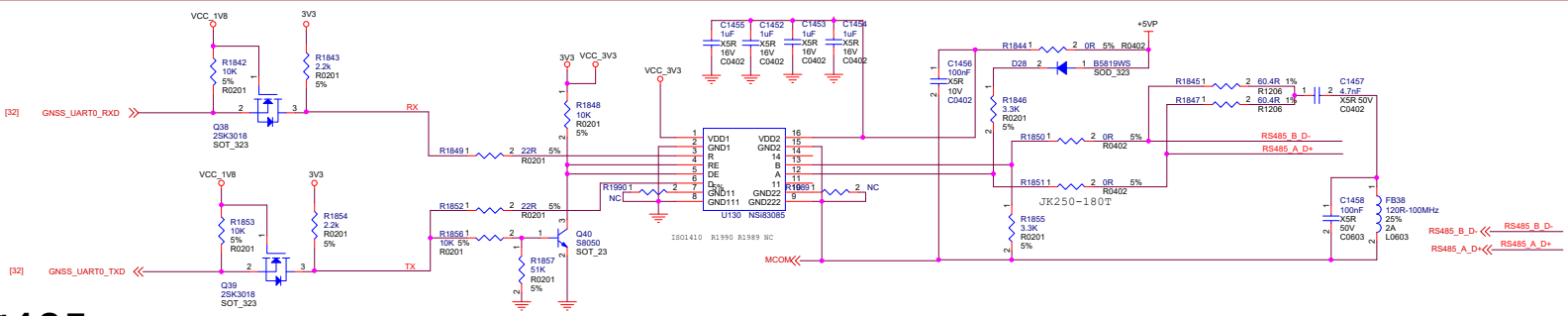
Size	Title: Sirider S1	REV
Custom	Page Name: 33.RTC	1.2
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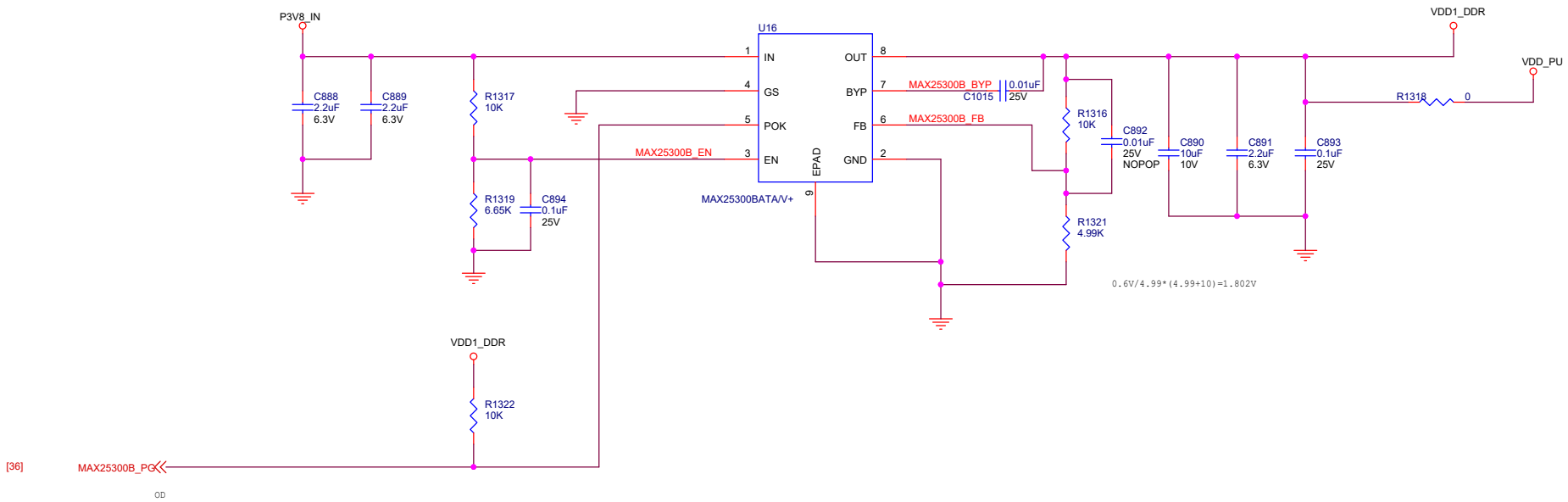
**CAN**



**RS232**



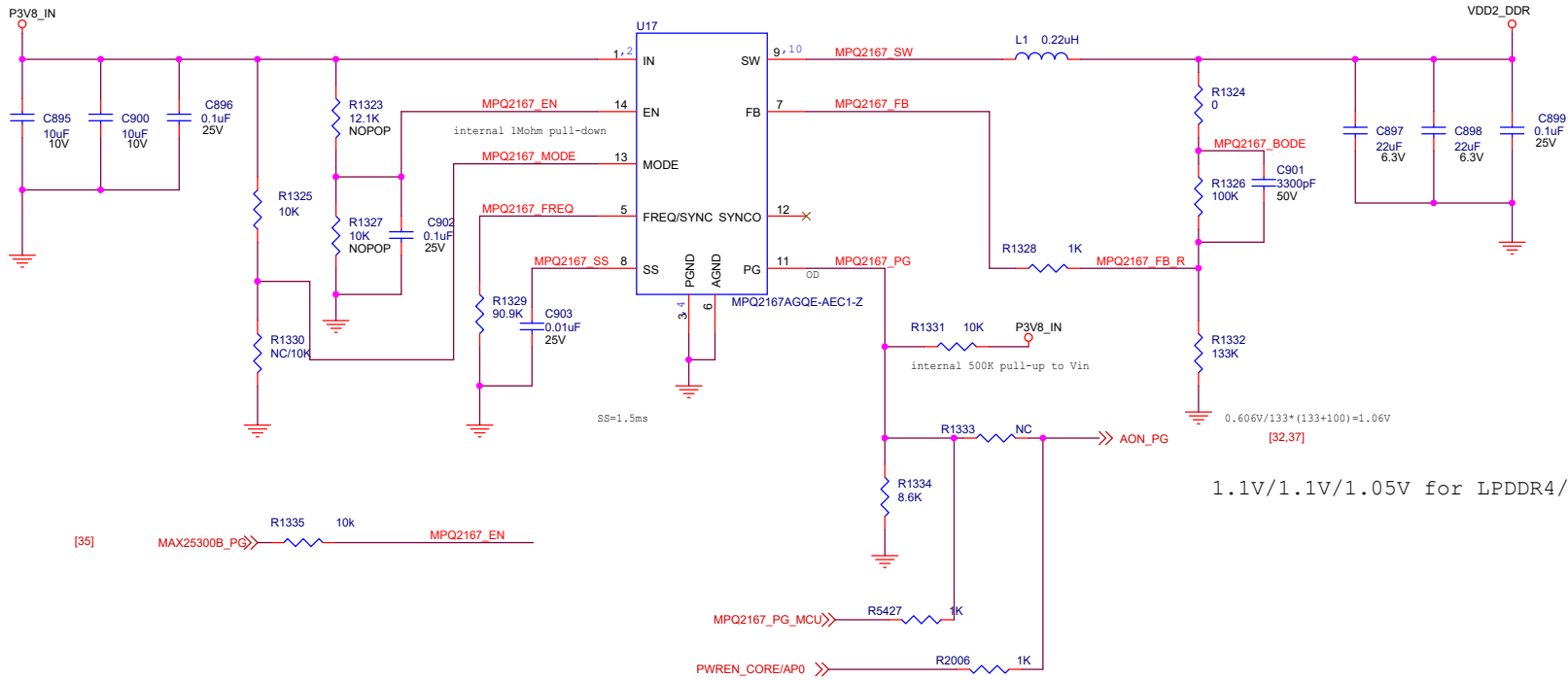
**RS485**



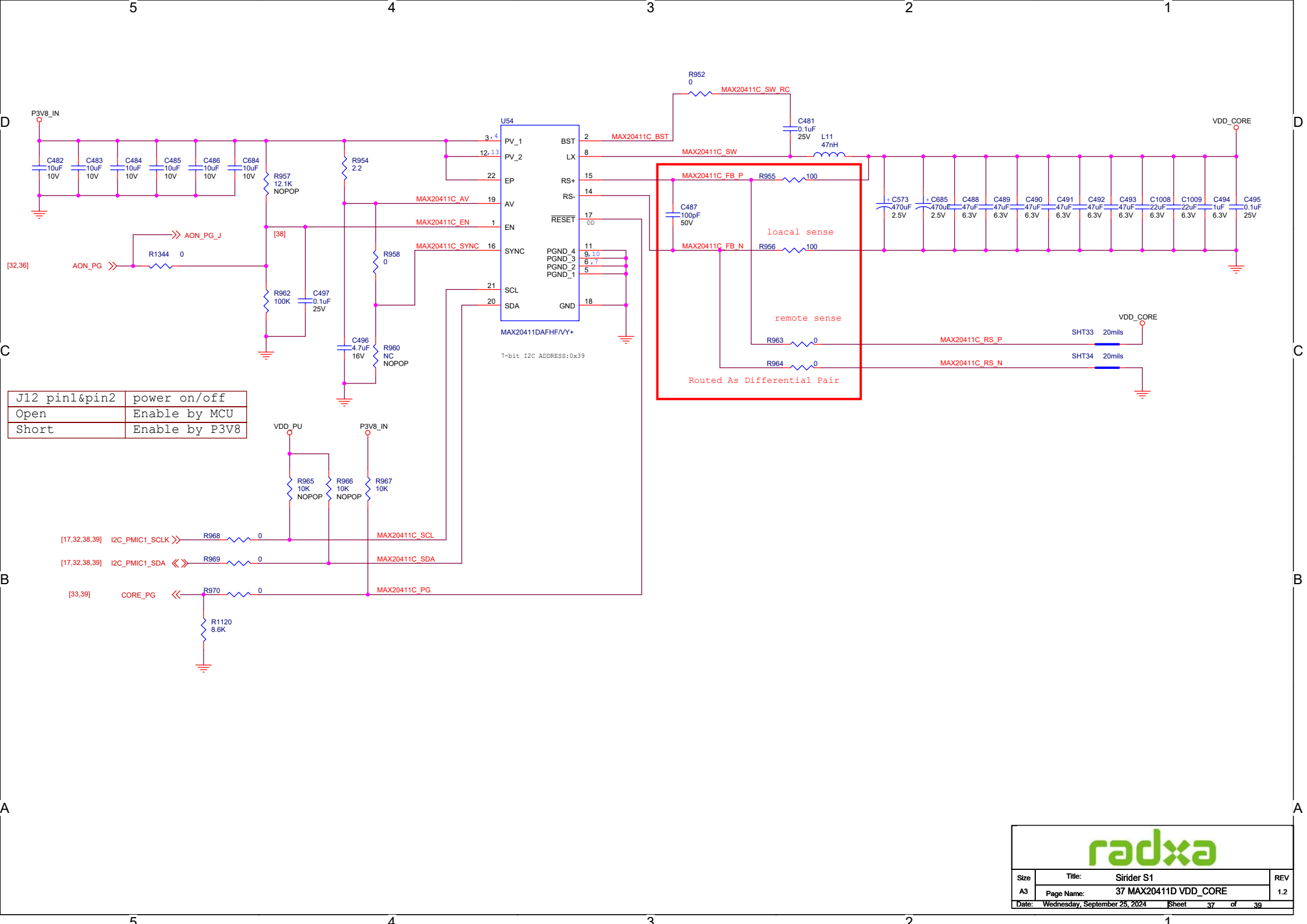
[36] MAX25300B\_PG<<  
OD



Size	Title: Sirider S1	REV
A3	Page Name: 35 MAX25300B VDD1_DDR	1.2
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Size	Title:	Sirider S1	REV
A3	Page Name:	36 MPQ2167 VDD2_DDR	1.2
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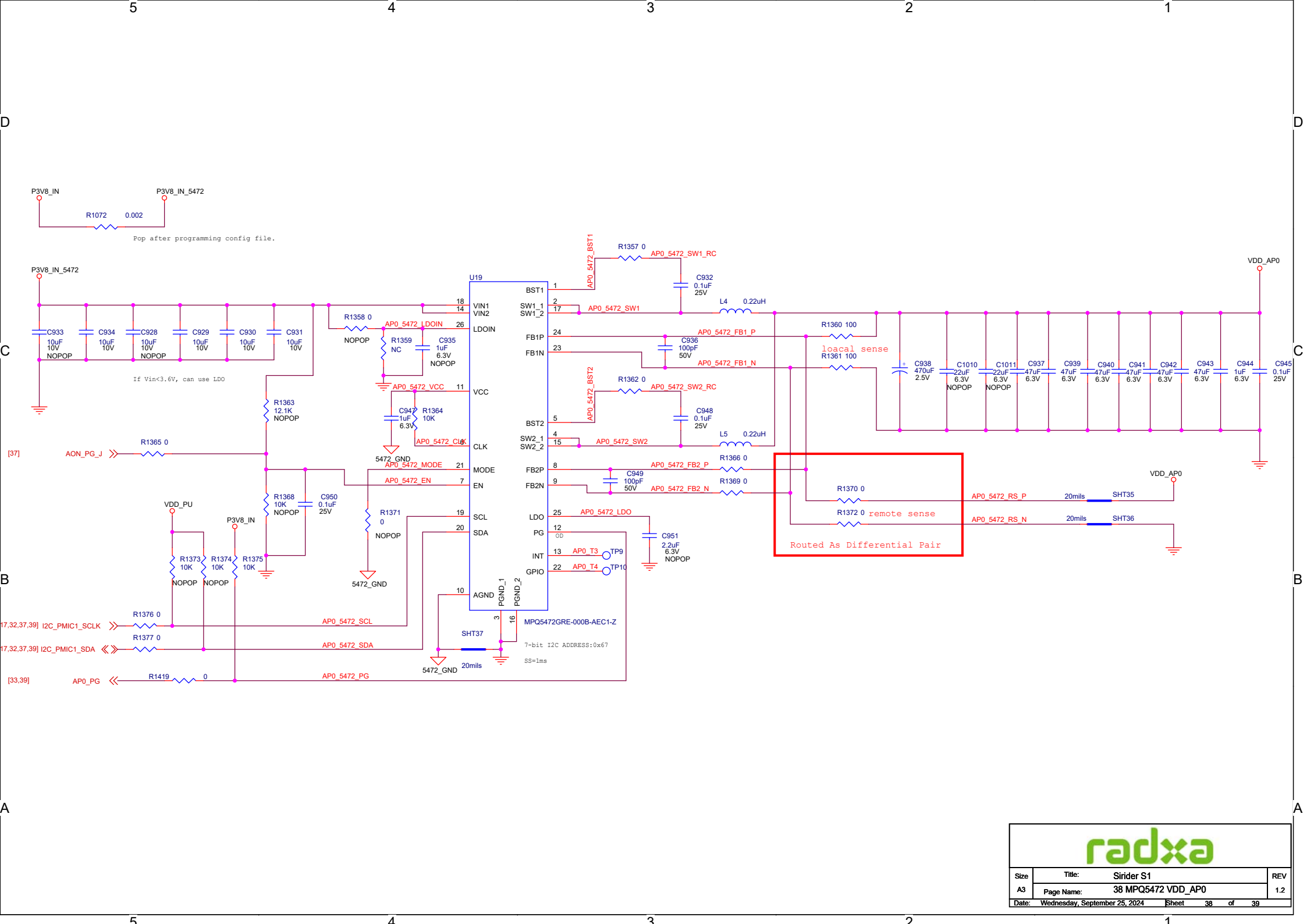
[32,36]

J12 pin1&pin2	power on/off
Open	Enable by MCU
Short	Enable by P3V8

[17,32,38,39]

[17,32,38,39]

[33,39]



P3V8\_IN\_5472

R1072 0.002

Pop after programming config file.

P3V8\_IN\_5472

C933 10uF 10V NOPOP

C934 10uF 10V NOPOP

C928 10uF 10V NOPOP

C929 10uF 10V NOPOP

C930 10uF 10V NOPOP

C931 10uF 10V NOPOP

If Vin<3.6V, can use LDO

[37] AON\_PG\_J

R1365 0

VDD\_PU

P3V8\_IN

R1373 10K NOPOP

R1374 10K NOPOP

R1375 10K NOPOP

R1368 10K NOPOP

C950 0.1uF 25V

[7,32,37,39] I2C\_PMIC1\_SCLK

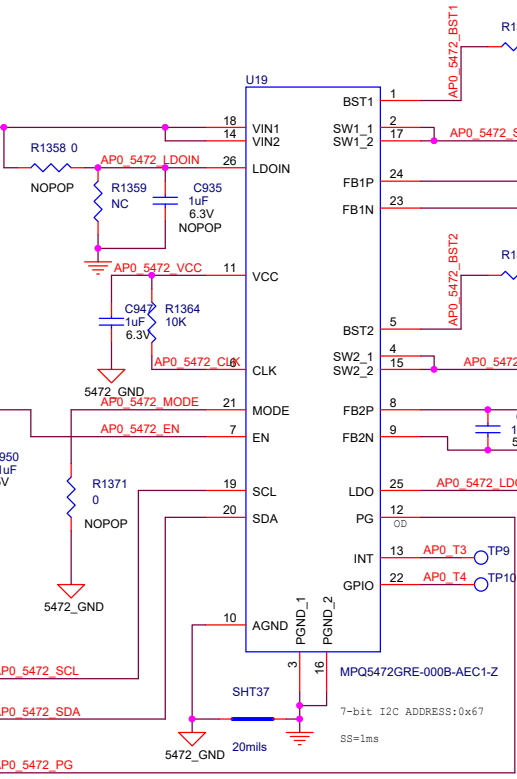
R1376 0

[7,32,37,39] I2C\_PMIC1\_SDA

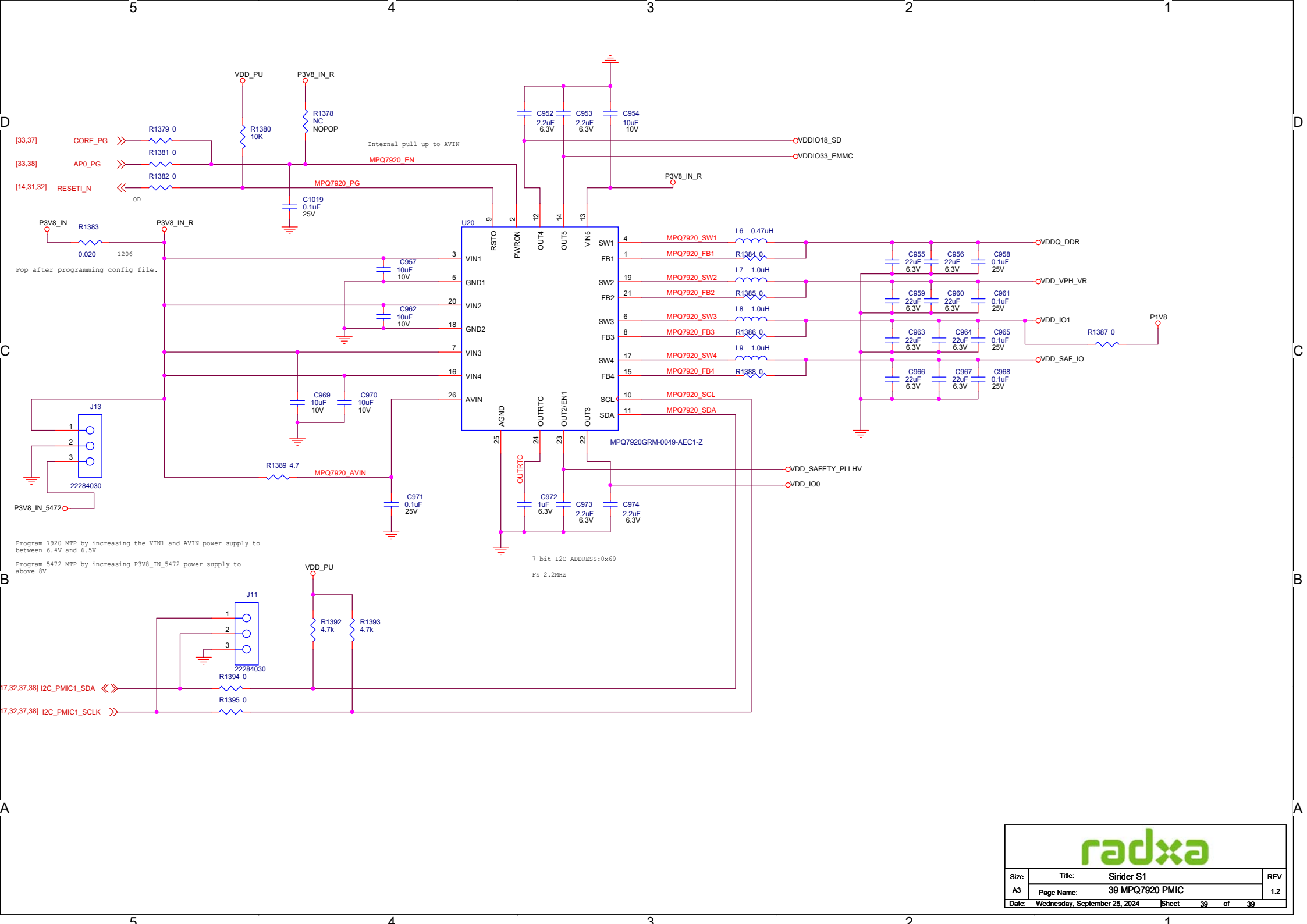
R1377 0

[33,39] AP0\_PG

R1419 0



Routed As Differential Pair



[33.37] CORE\_PG >>  
 [33.38] AP0\_PG >>  
 [14.31,32] RESET\_N <<

Pop after programming config file.

Program 7920 MTP by increasing the VIN1 and AVIN power supply to between 6.4V and 6.5V  
 Program 5472 MTP by increasing P3V8\_IN\_5472 power supply to above 8V

[7.32,37,38] I2C\_PMIC1\_SDA <<  
 [7.32,37,38] I2C\_PMIC1\_SCLK >>

Size	Title: Sirider S1	REV
A3	Page Name: 39 MPQ7920 PMIC	1.2
Date: Wednesday, September 25, 2024	Sheet 39	of 39