



# Radxa X4

schematic

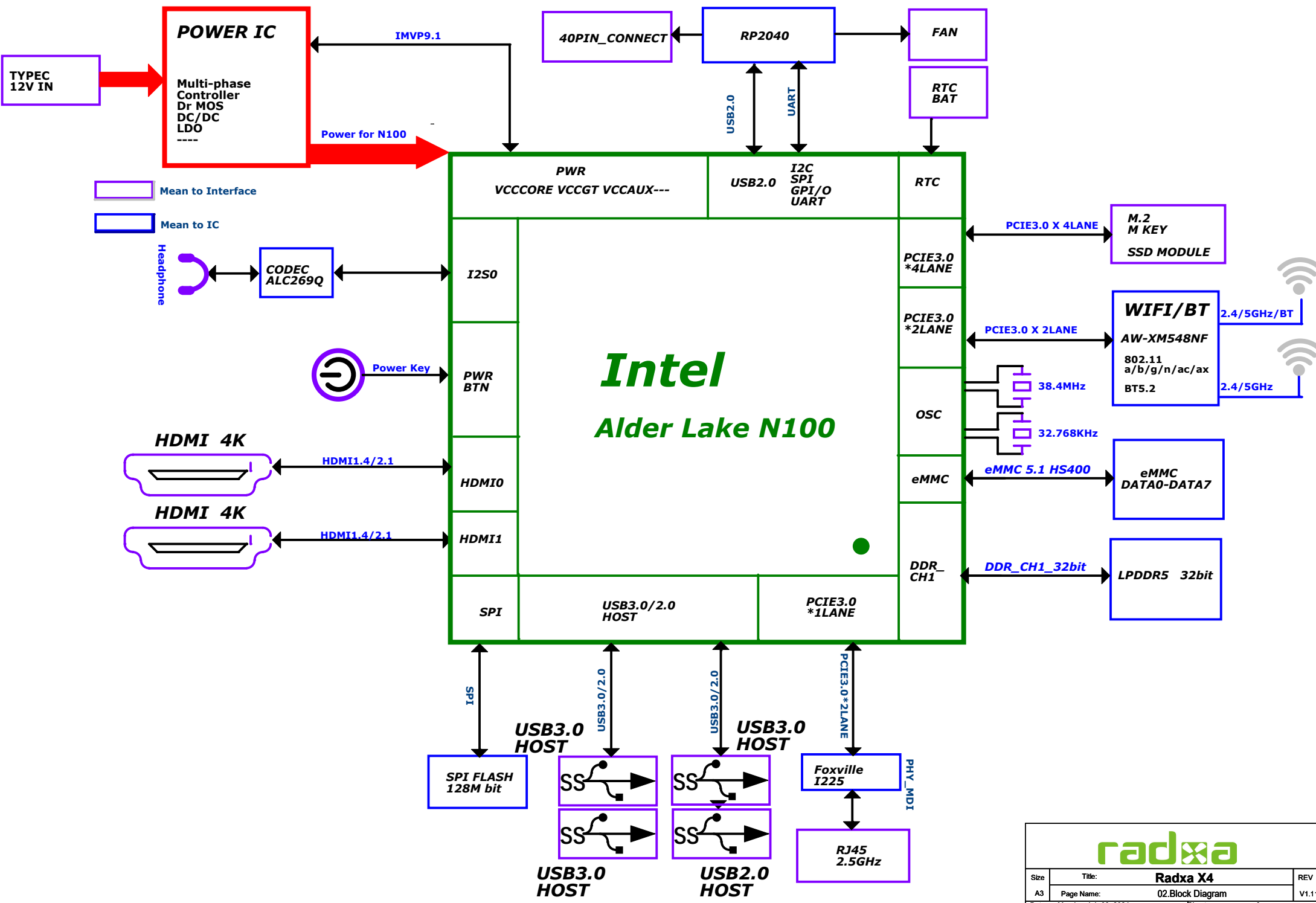
V1.11

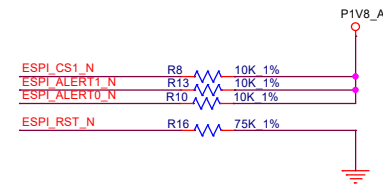
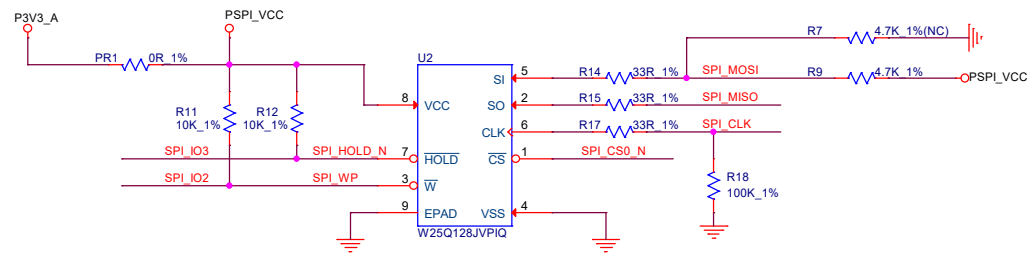
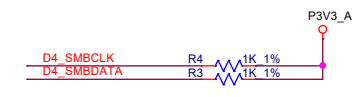
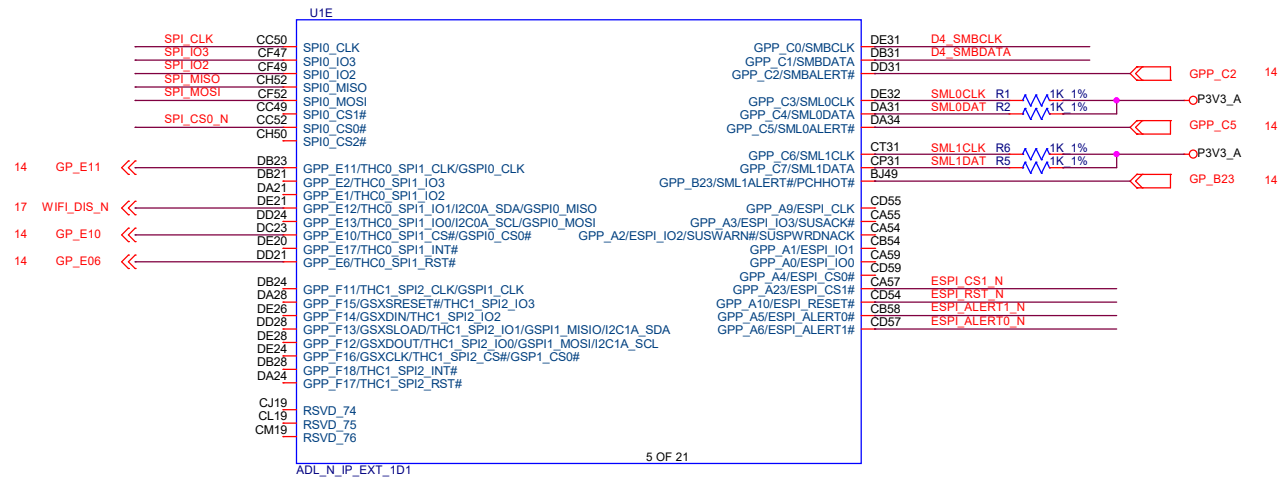


## Table of Content

Page 1	01.Index and Notes
Page 2	02.Block Diagram
Page 3	03 SPI AND JTAG
Page 4	04 CPU DDRC
Page 5	05 DISPLAY
Page 6	06 PSE_GBE
Page 7	07 CLK/HDA
Page 8	08 PCIE_USB3
Page 9	09 MSIC_EMMC
Page 10	10 CFG
Page 11	11 POWER
Page 12	12 GND
Page 13	13 LPDDR5
Page 14	14 Strap SOC
Page 15	15 Decap
Page 16	16 DUAL HDMI
Page 17	17 KEY M*2&WIFI
Page 18	18 USB PORT
Page 19	19 LAN_2G5
Page 20	20 EMMC
Page 21	21 RS2040
Page 22	22 ALC269Q-VB6
Page 23	23 VCCIN
Page 24	24 VCCGT
Page 25	25 VDDQ
Page 26	26 DC POWER
Page 27	27 VCCST_CPU
Page 28	28 Histroy

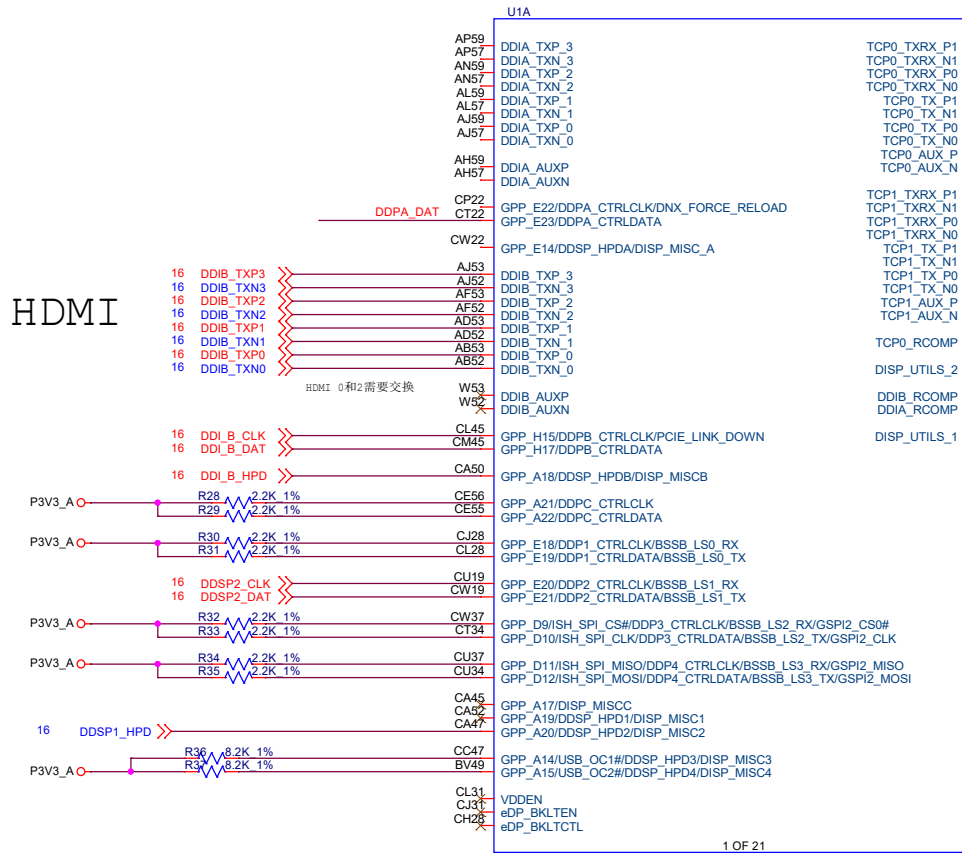




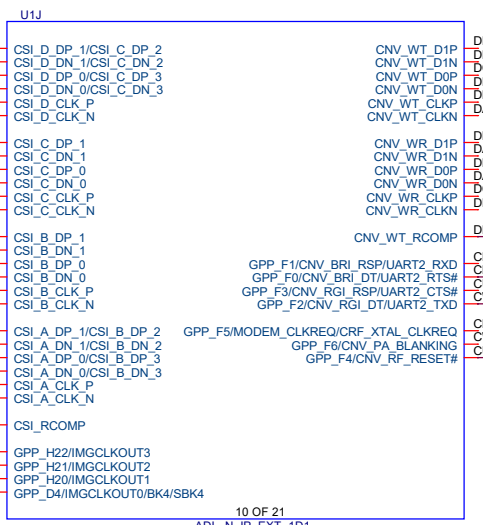




# HDMI

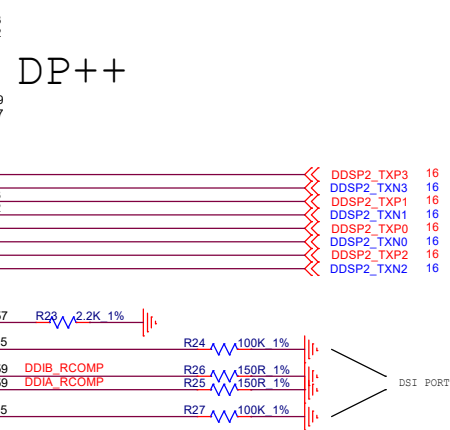


1 OF 21  
ADL\_N\_IP\_EXT\_1D1



10 OF 21  
ADL\_N\_IP\_EXT\_1D1

## DP++

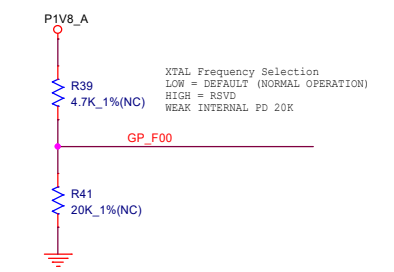
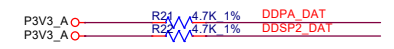


TCP Port Signal Mapping for HDMI / DP

TCP	HDMI	DP
TX0	DATA2	LANE0
TX1	DATA0	LANE2
TXR0	DATA1	LANE1
TXR1	CLK	LANE3


DDI Port Signal Mapping for HDMI / DP

DDI	HDMI
TX0	DATA2
TX1	DATA1
TX2	DATA0
TX3	CLK

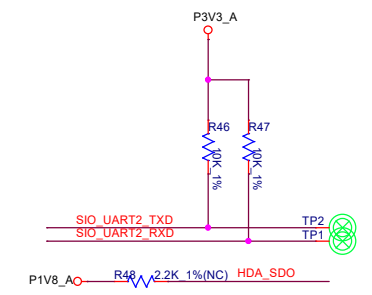
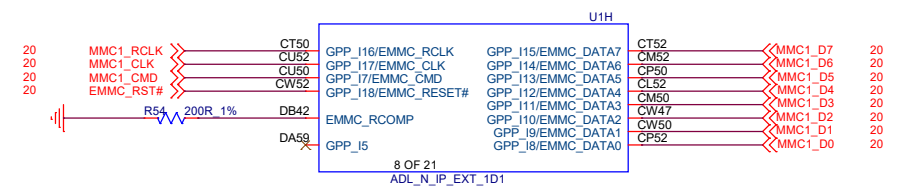
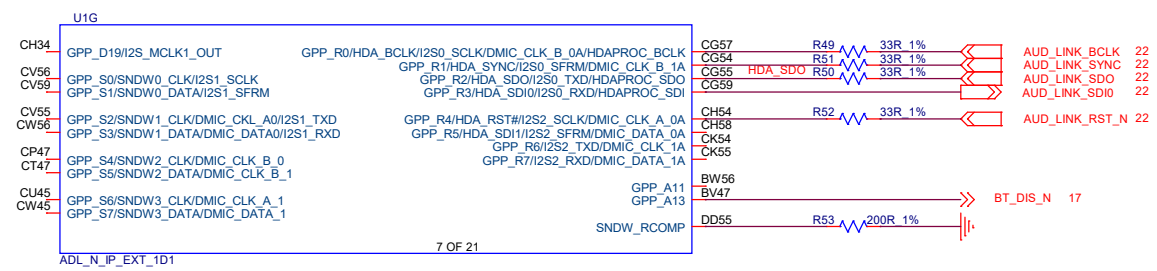
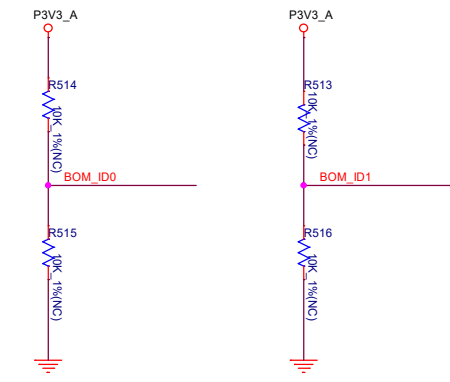
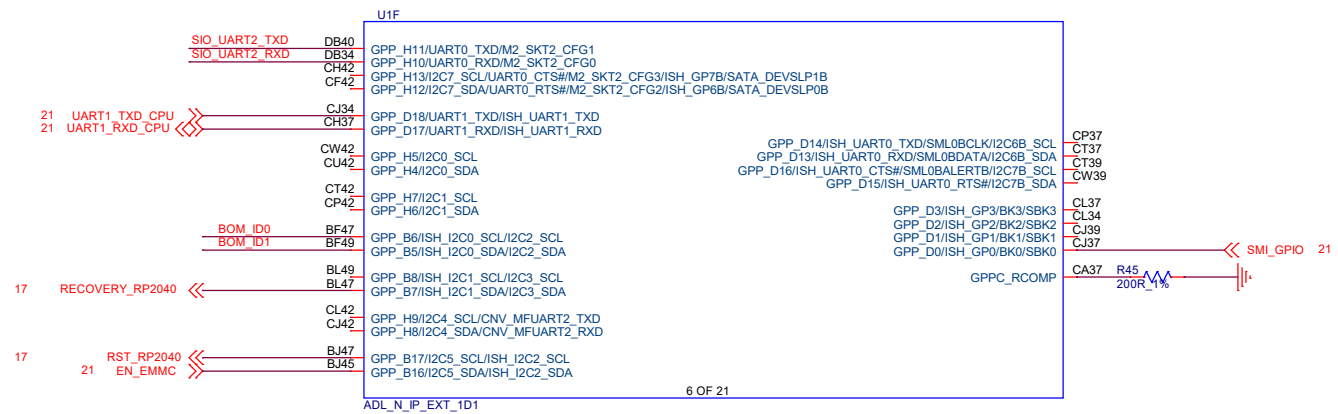


M.2 CNVI MODES  
LOW -> INTEGRATED CNVI ENABLE  
HIGH -> INTEGRATED CNVI DISABLE  
NO INTERNAL PU/PD SAMPLING - RSMRSTB



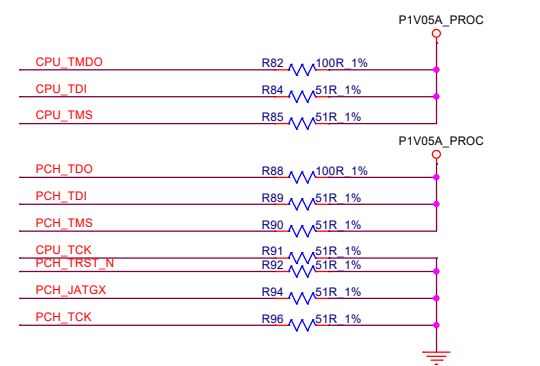
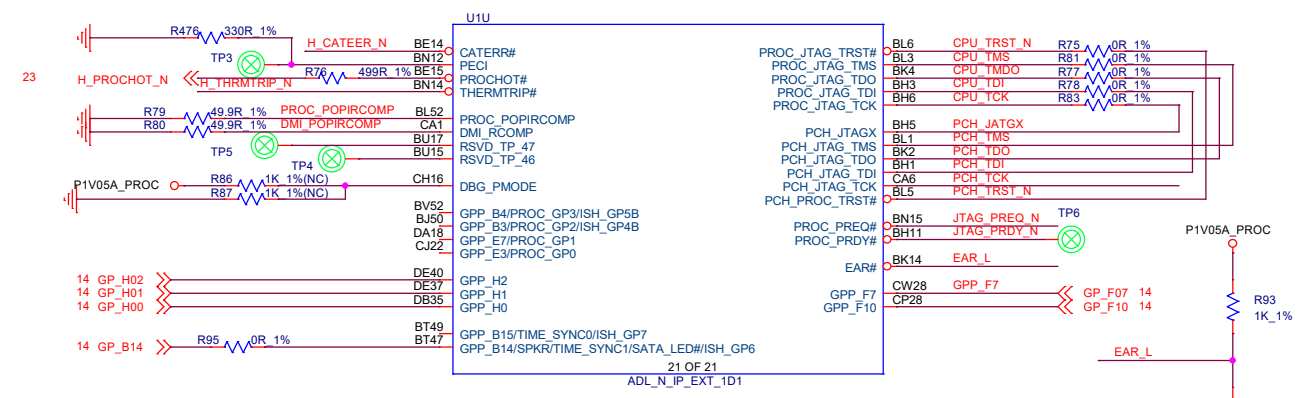
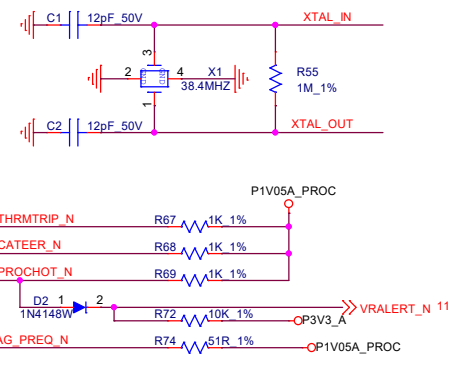
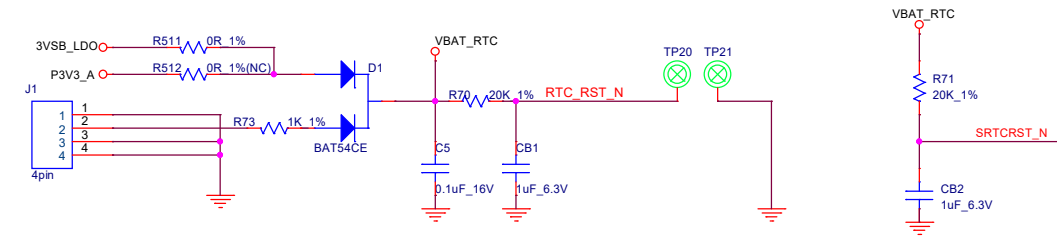
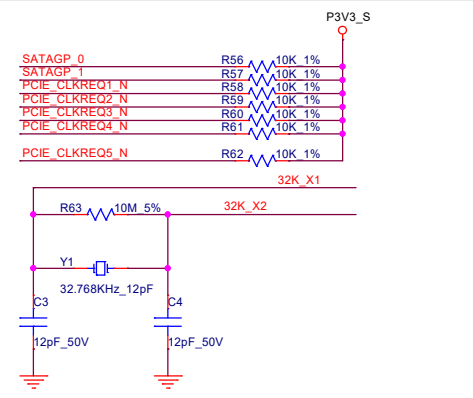
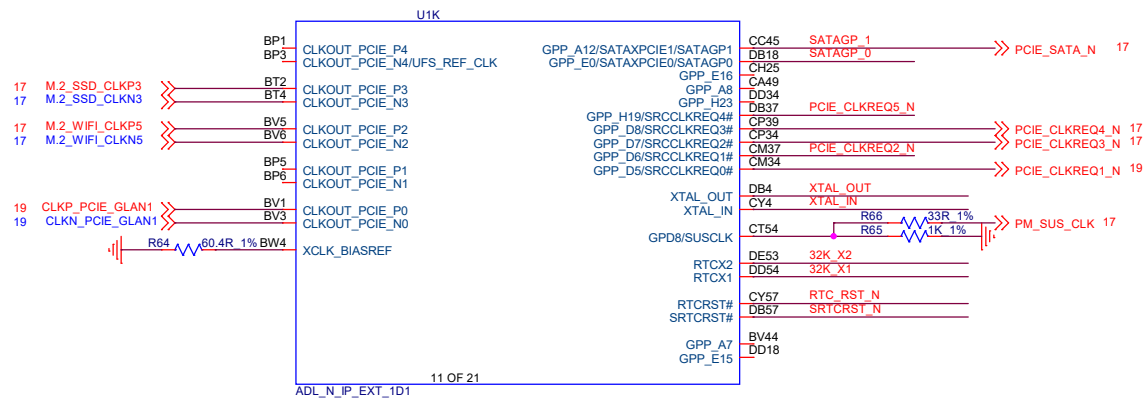


Size	Title: Radxa X4	REV
A3	Page Name: 05 DISPLAY	V1.11
Date: Monday, July 08, 2024	Sheet 5 of 27	



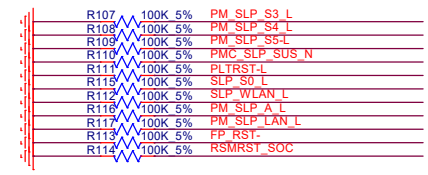
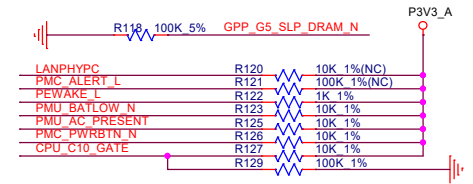
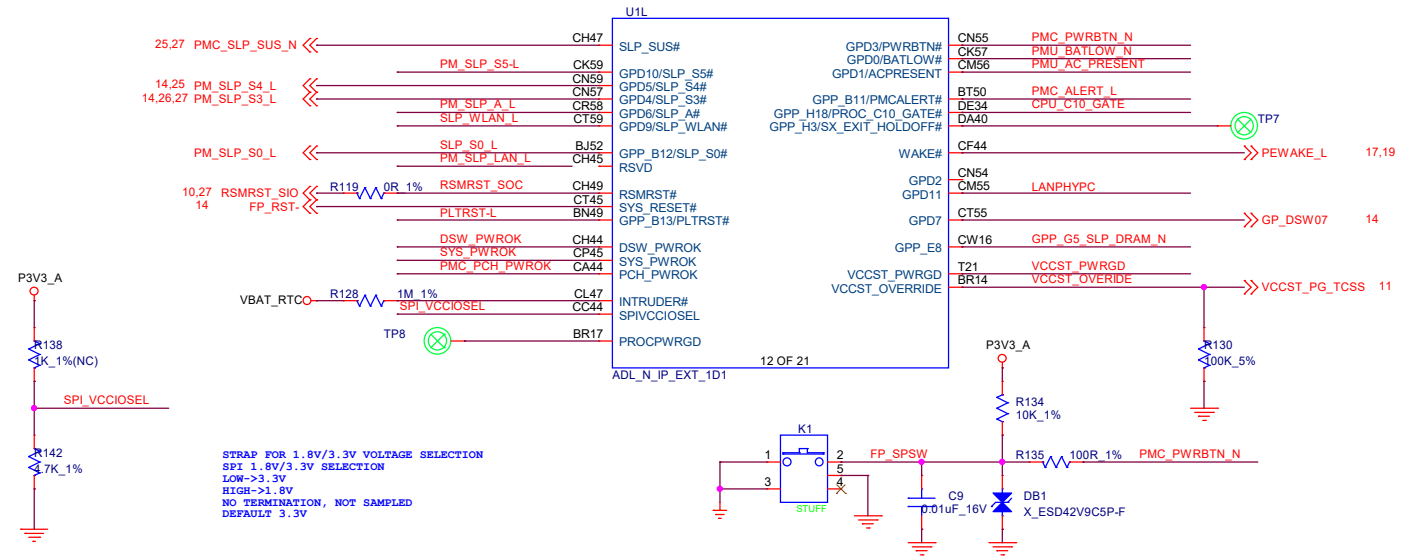
**radxa**

Size	Title:	Radxa X4	REV
A3	Page Name:	06 PSE_GBE	V1.11
Date:	Monday, July 08, 2024	Sheet	6 of 27

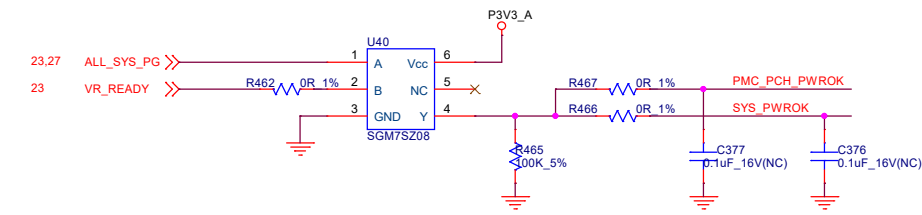
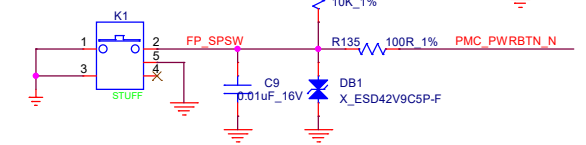




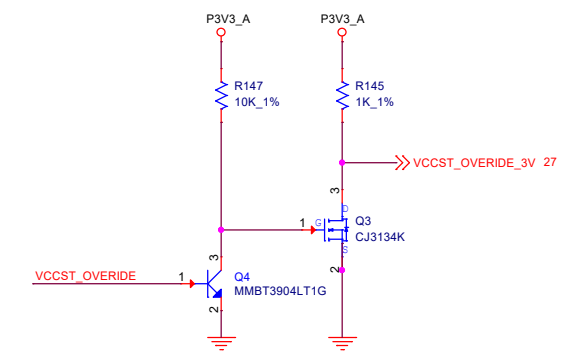
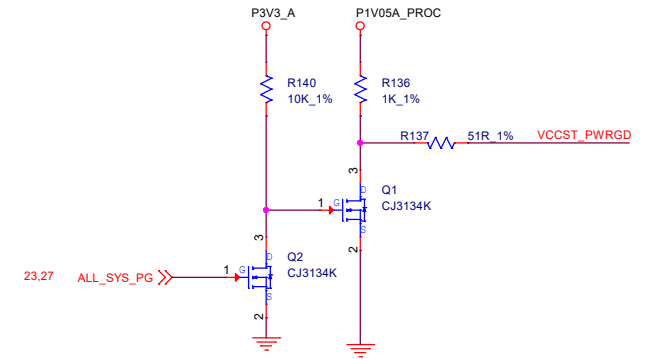
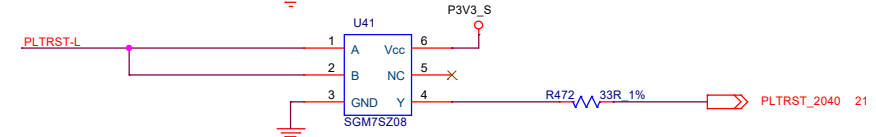
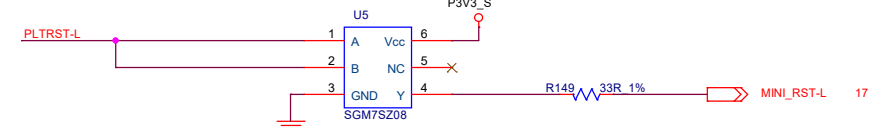
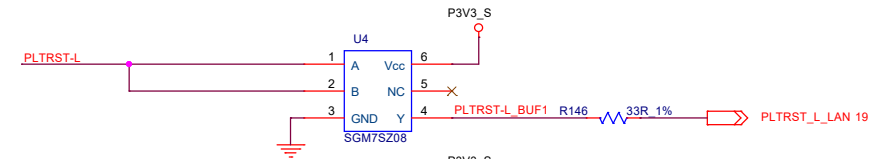
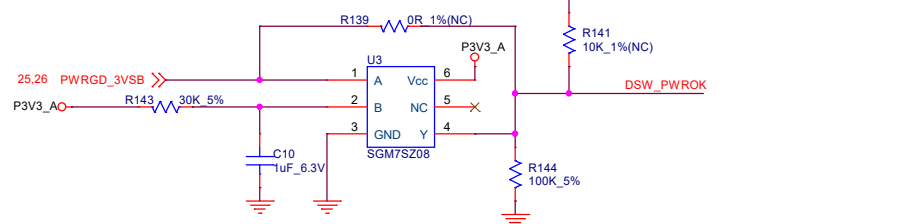


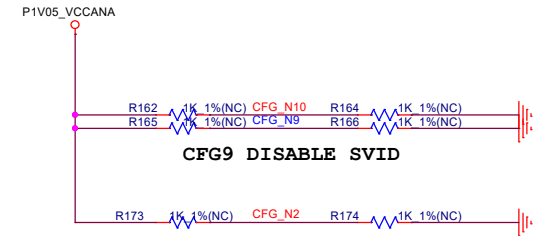
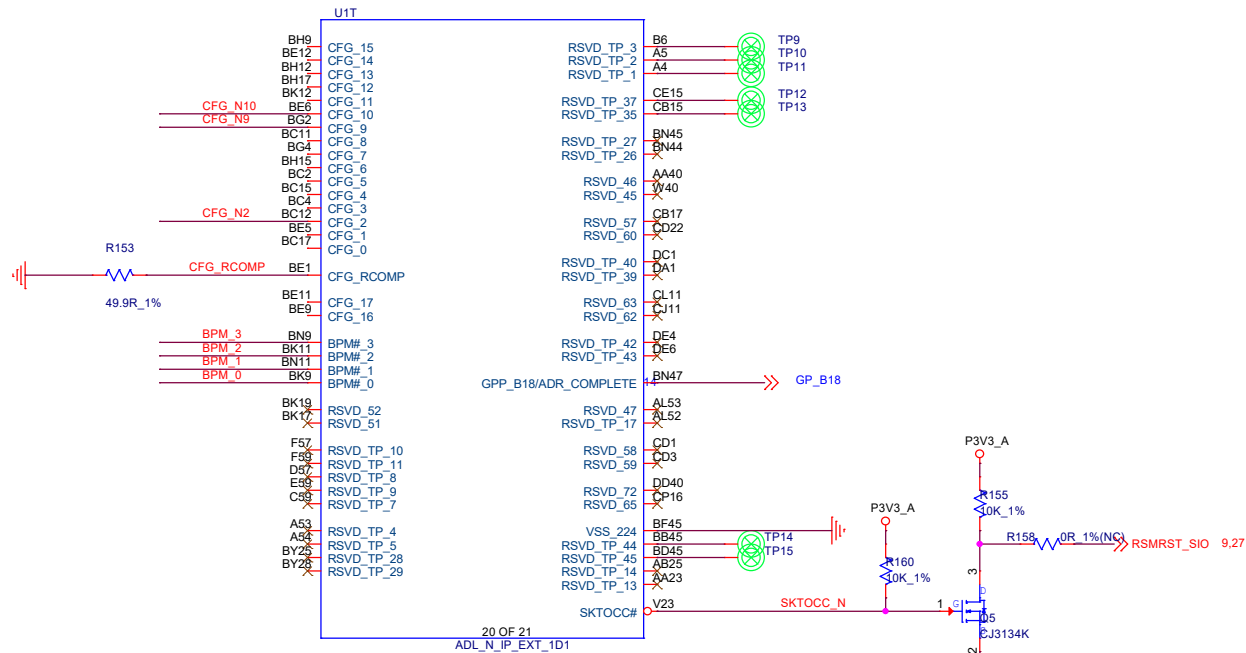
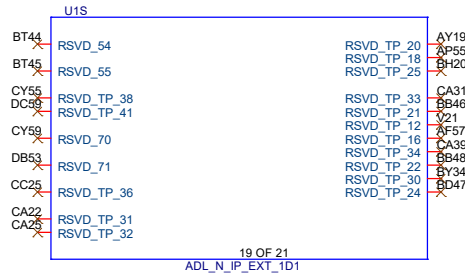


STRAP FOR 1.8V/3.3V VOLTAGE SELECTION  
 SPI 1.8V/3.3V SELECTION  
 LOW->3.3V  
 HIGH->1.8V  
 NO TERMINATION, NOT SAMPLED  
 DEFAULT 3.3V

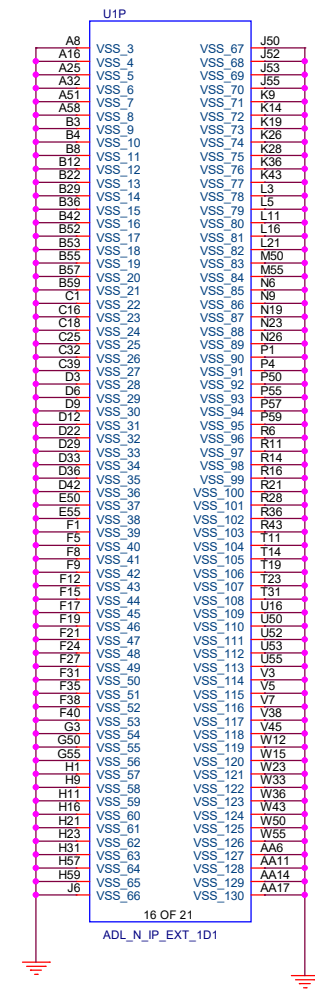
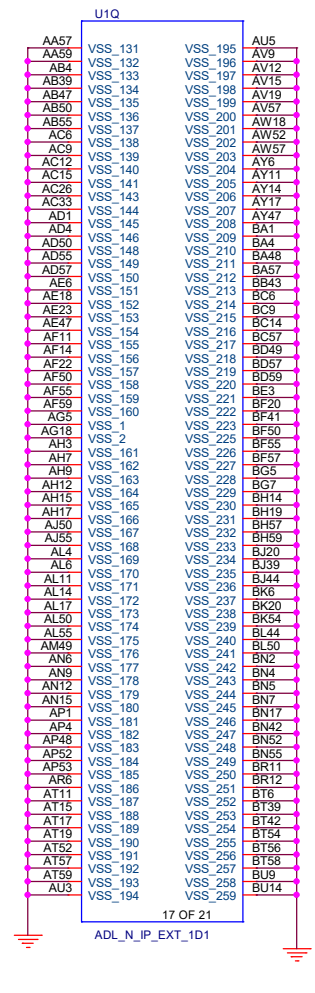
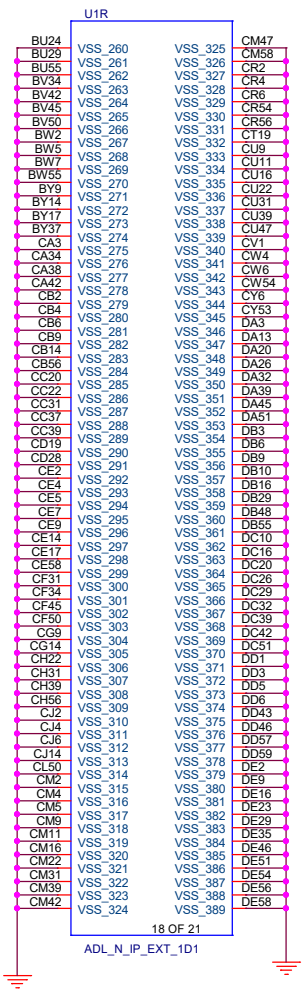



**PDG\_646929\_P535 delay 10ms**

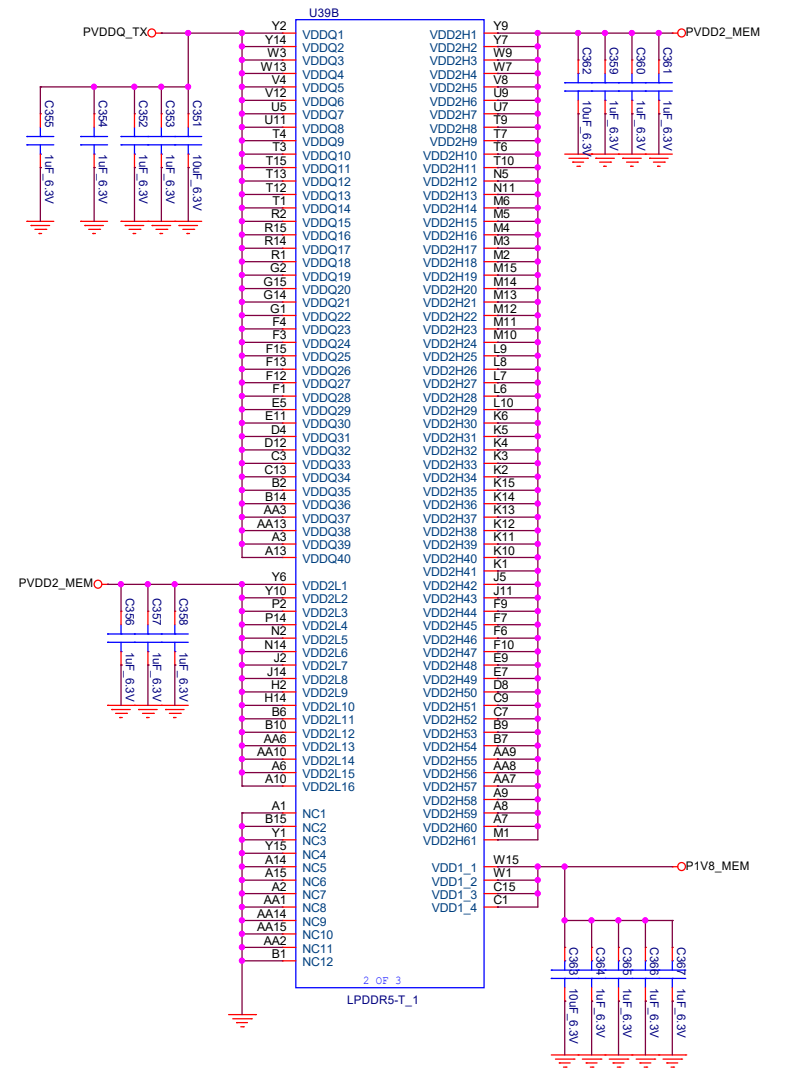
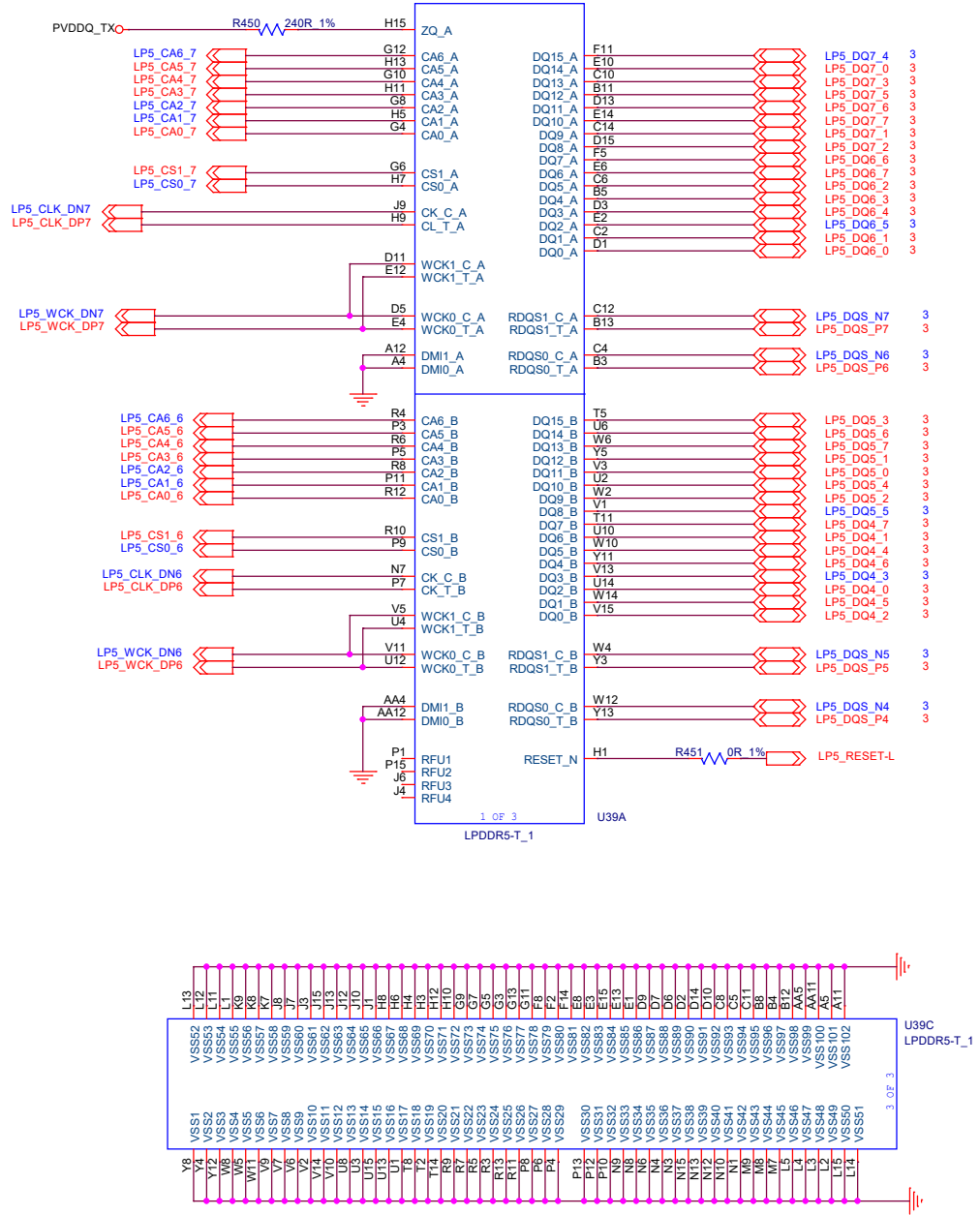


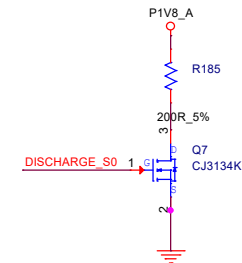
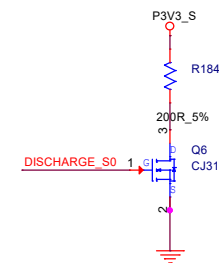
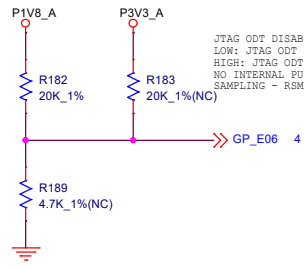
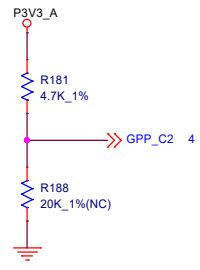
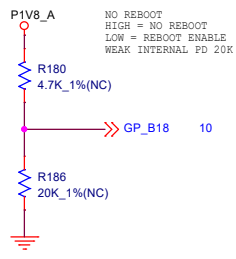
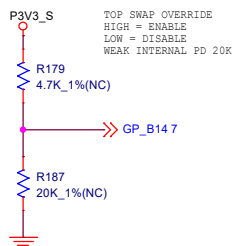




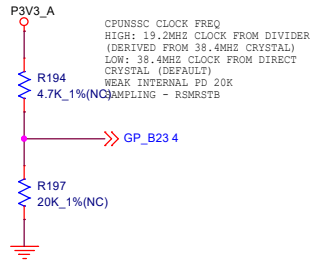
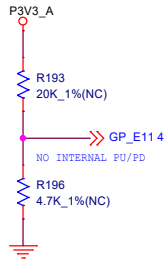
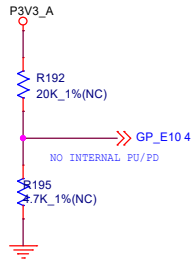



Size	Title:	Radxa X4	REV
A3	Page Name:	12 GND	V1.11
Date:	Monday, July 08, 2024	Sheet	12 of 27



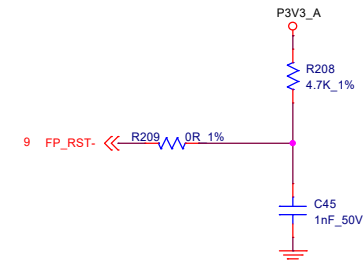
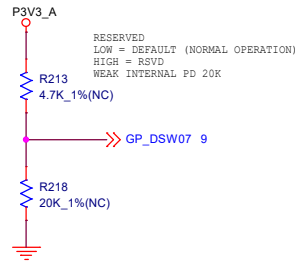
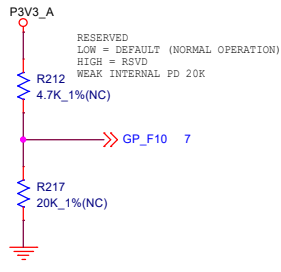
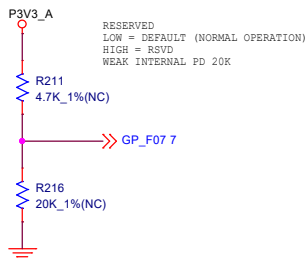
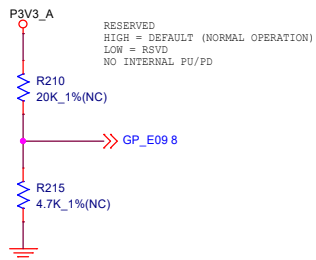
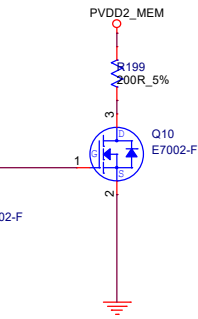
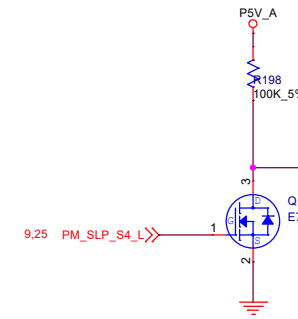
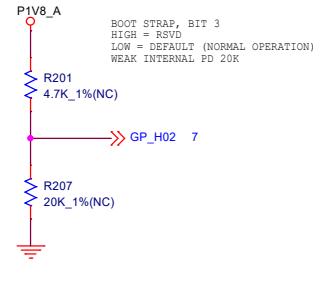
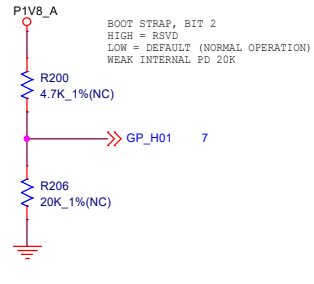
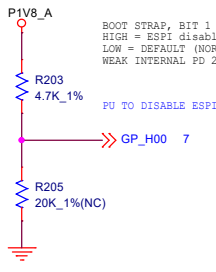
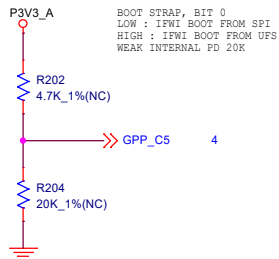
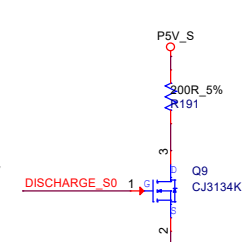
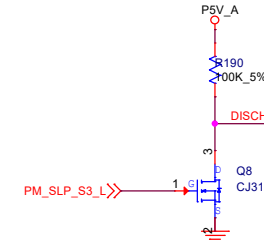


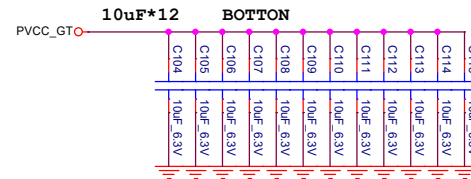
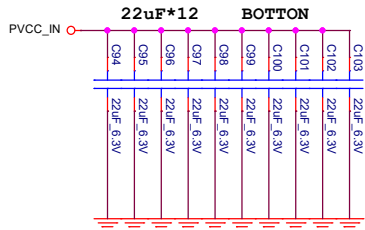
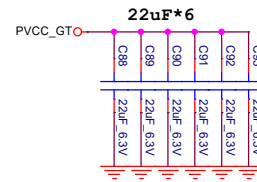
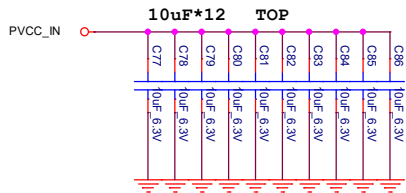
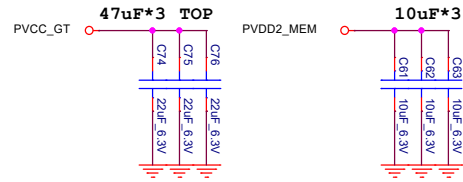
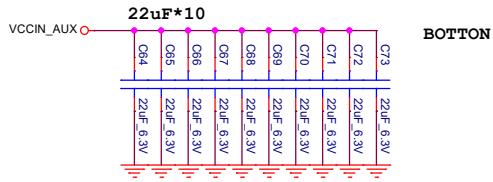
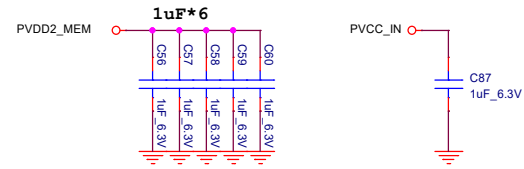
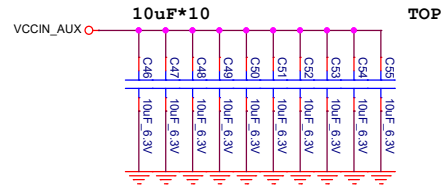
TLS Confidentiality  
 0=>Disable Intel? CSME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)  
 1=>Enable Intel? CSME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel? AMT with TLS  
 WEAK INTERNAL PD 20K



GP_E10	GP_E11	DDR
0	0	4GB
0	1	8GB
1	0	16GB
1	1	32GB

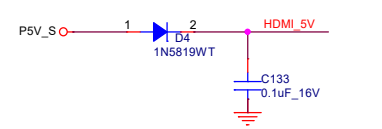
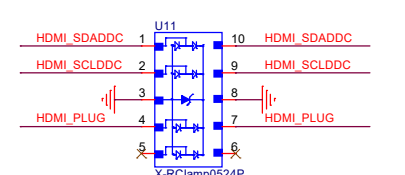
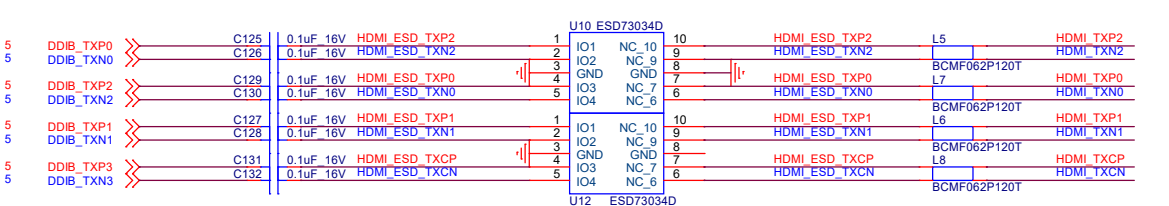
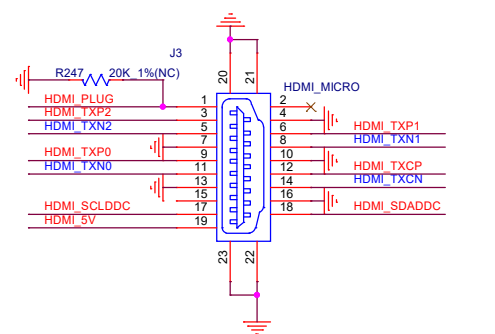
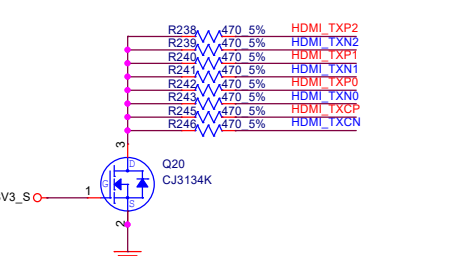
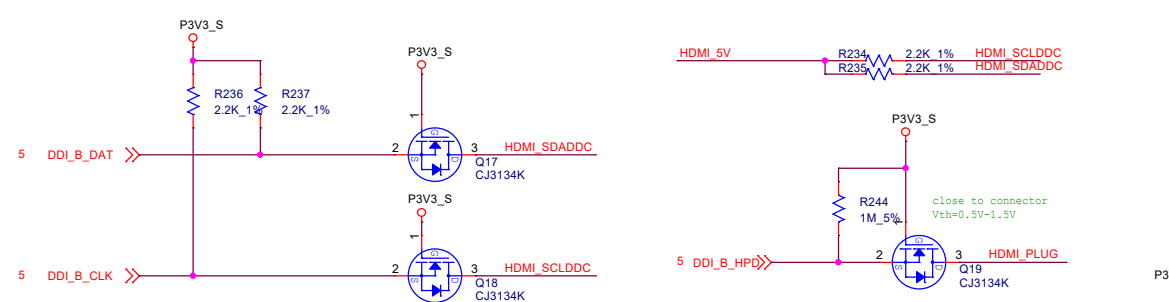
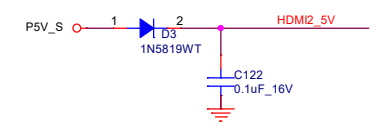
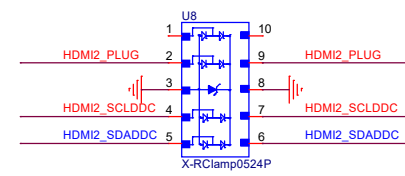
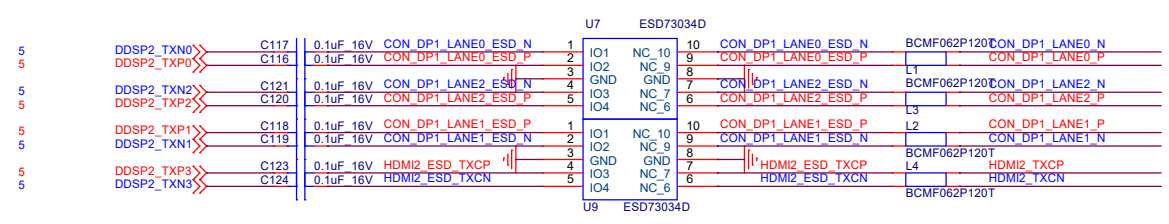
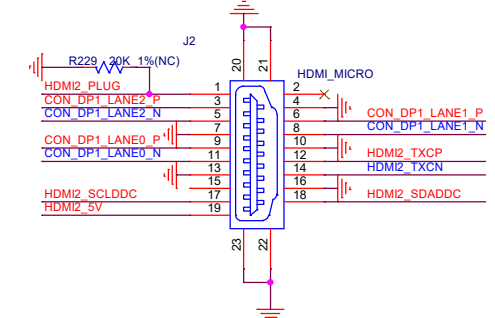
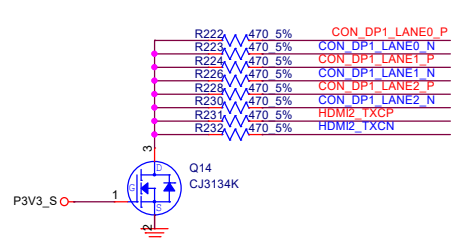
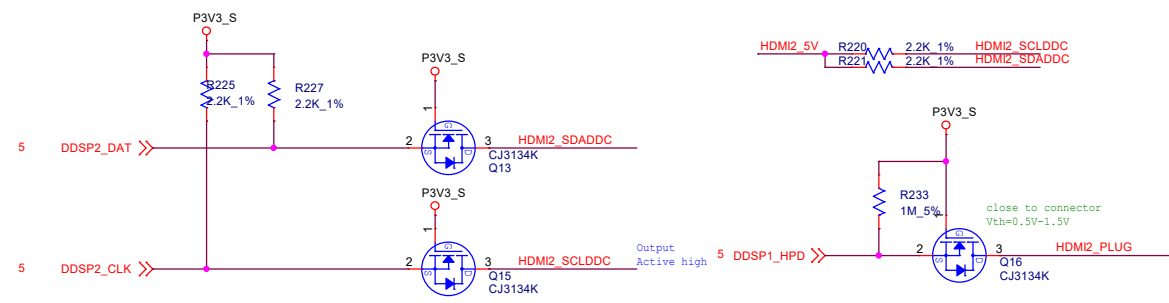
9.26.27



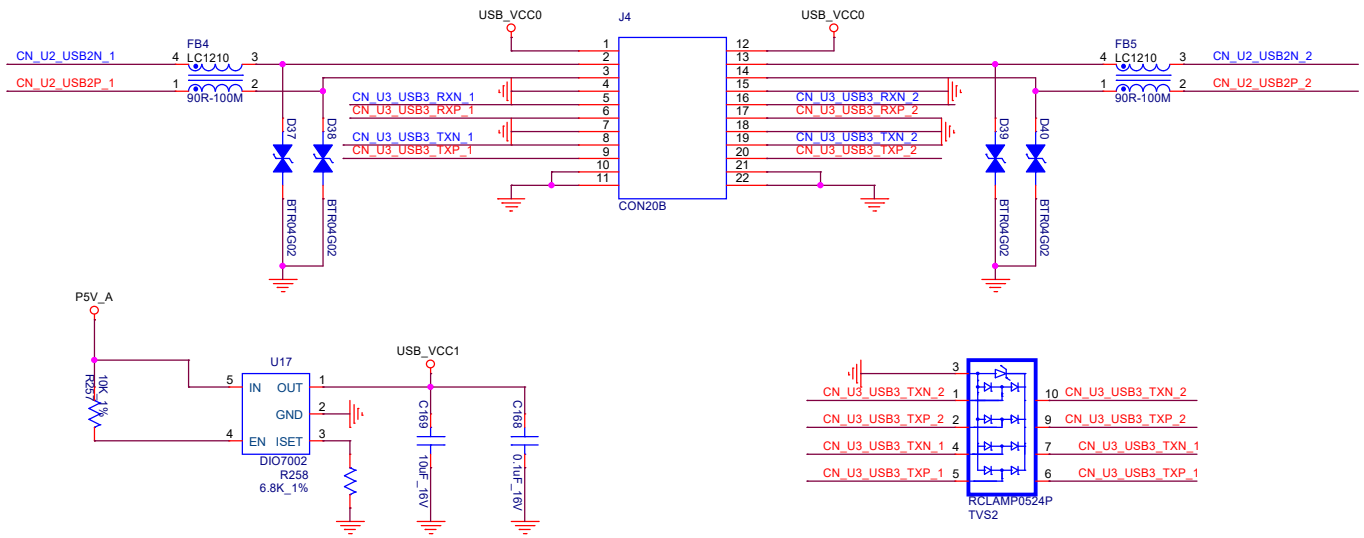


Size	Title: Radxa X4	REV
A3	Page Name: 15 Decap	V1.11
Date: Monday, July 08, 2024	Sheet 15 of 27	

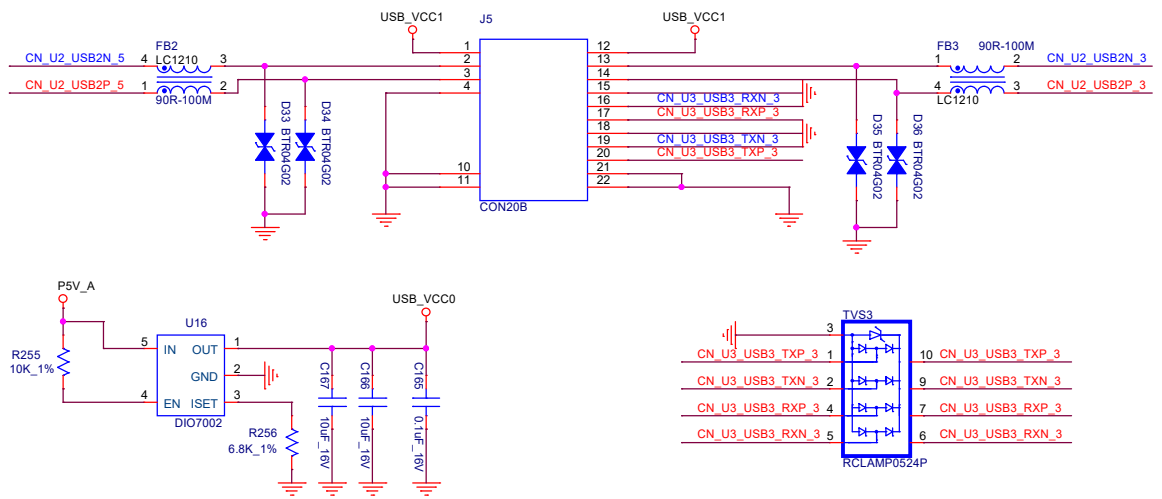
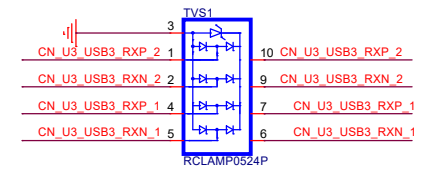
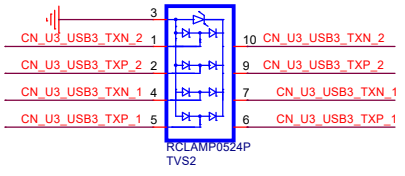




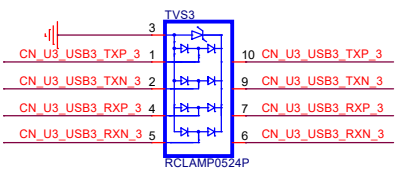




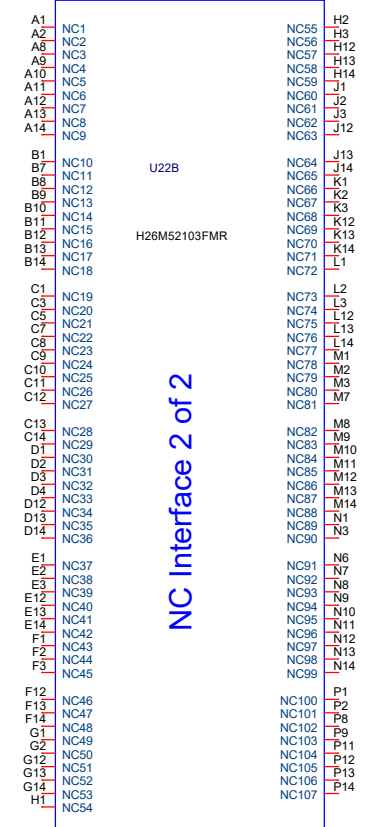
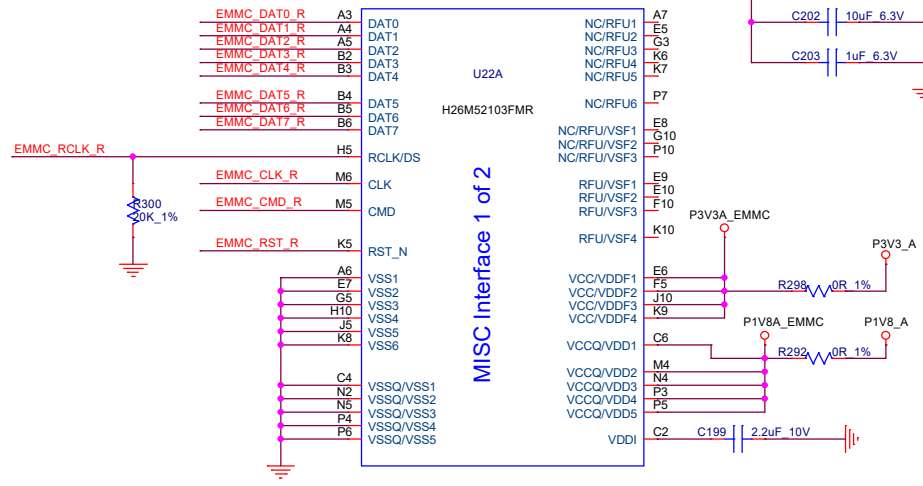
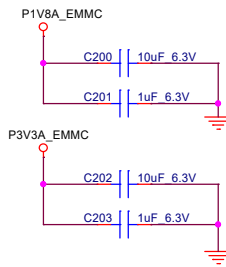
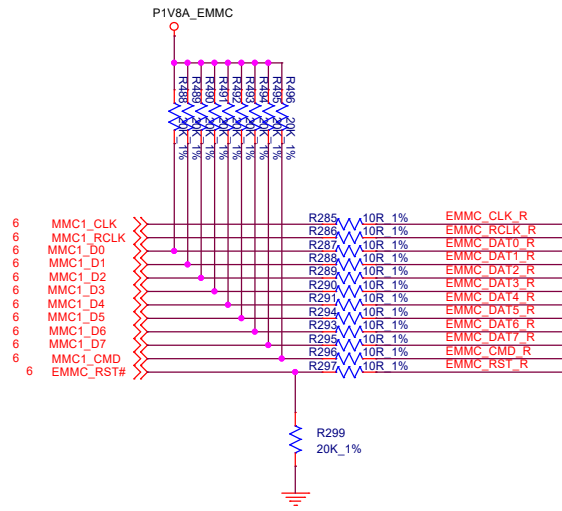
CN U3_USB3_TXP_1	C161	0.1uF 16V	U3_USB3_TXP_1
CN U3_USB3_TXN_1	C162	0.1uF 16V	U3_USB3_TXN_1
CN U3_USB3_RXP_1			U3_USB3_RXP_1
CN U3_USB3_RXN_1			U3_USB3_RXN_1
CN U2_USB2P_1			U2_USB2P_1 8
CN U2_USB2N_1			U2_USB2N_1 8
CN U3_USB3_TXP_2	C163	0.1uF 16V	U3_USB3_TXP_2
CN U3_USB3_TXN_2	C164	0.1uF 16V	U3_USB3_TXN_2
CN U3_USB3_RXP_2			U3_USB3_RXP_2
CN U3_USB3_RXN_2			U3_USB3_RXN_2
CN U2_USB2P_2			U2_USB2P_2 8
CN U2_USB2N_2			U2_USB2N_2 8



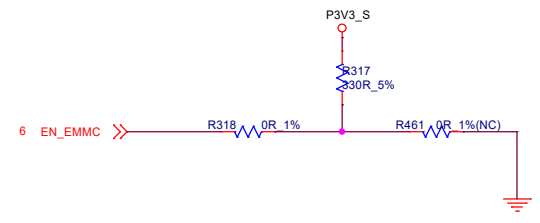
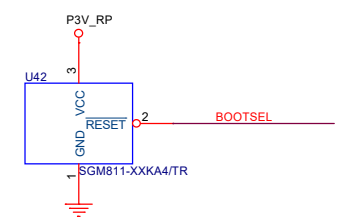
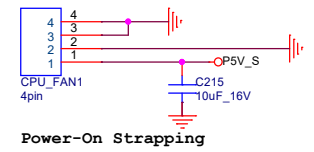
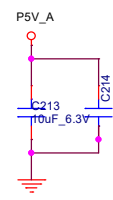
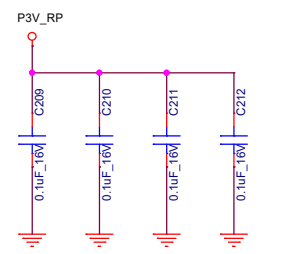
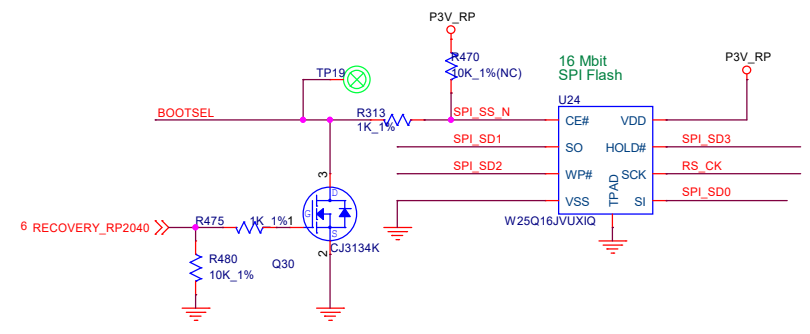
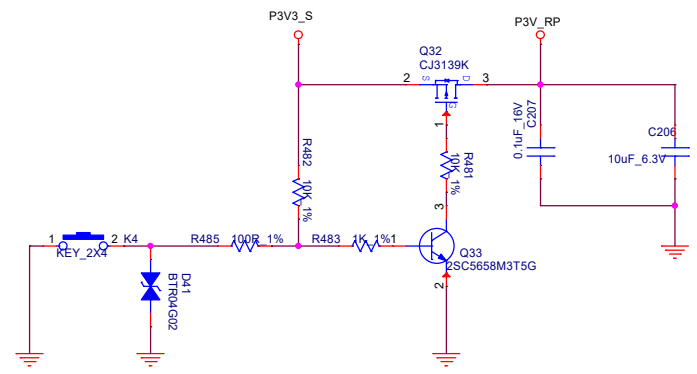
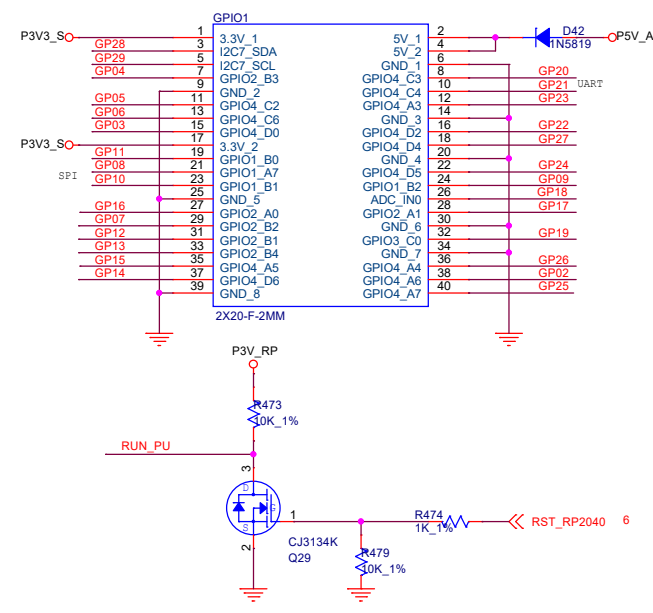
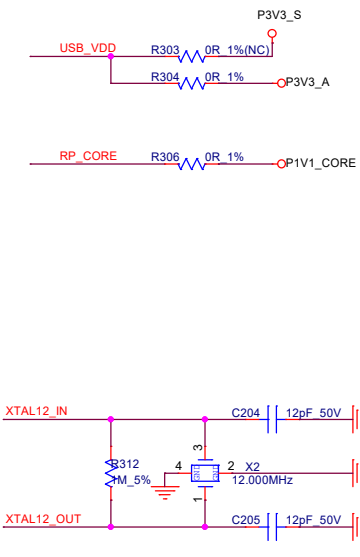
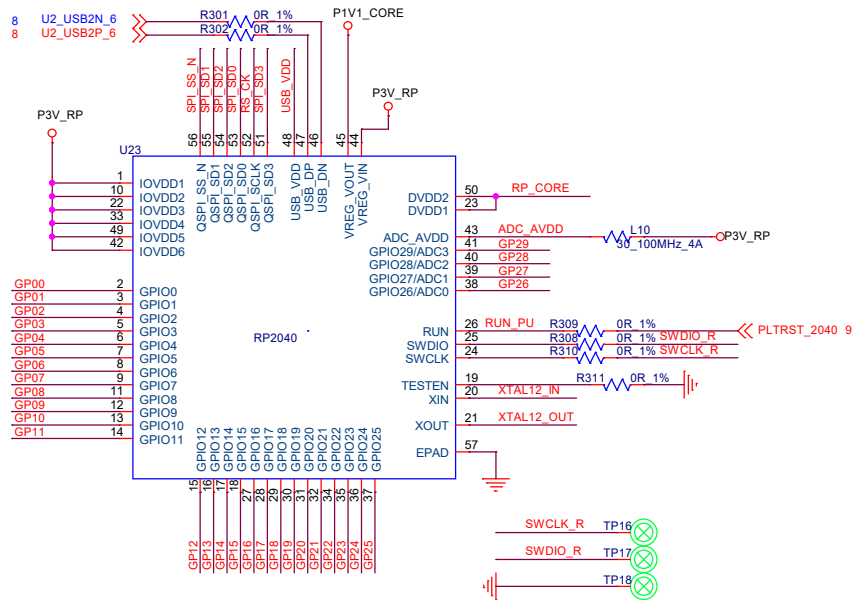
CN U3_USB3_TXP_3	C170	0.1uF 16V	U3_USB3_TXP_3
CN U3_USB3_TXN_3	C171	0.1uF 16V	U3_USB3_TXN_3
CN U3_USB3_RXP_3			U3_USB3_RXP_3
CN U3_USB3_RXN_3			U3_USB3_RXN_3
CN U2_USB2N_3			U2_USB2N_3 8
CN U2_USB2P_3			U2_USB2P_3 8
CN U2_USB2N_5			U2_USB2N_5 8
CN U2_USB2P_5			U2_USB2P_5 8

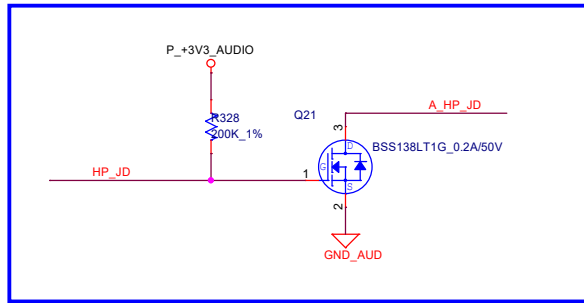




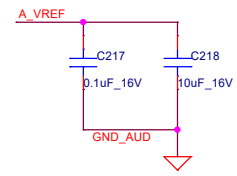
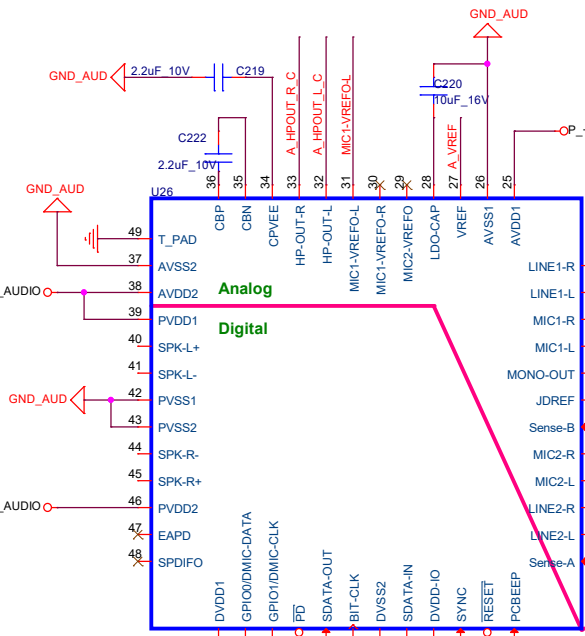
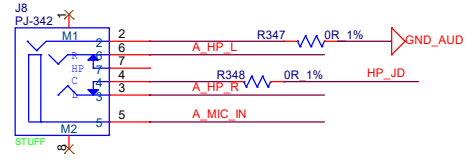
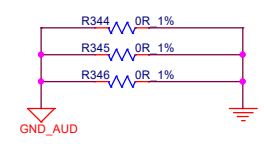
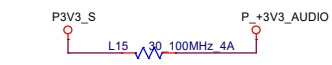
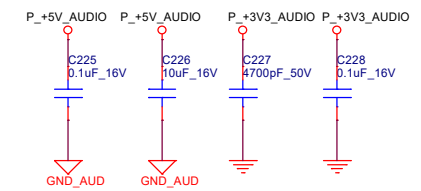
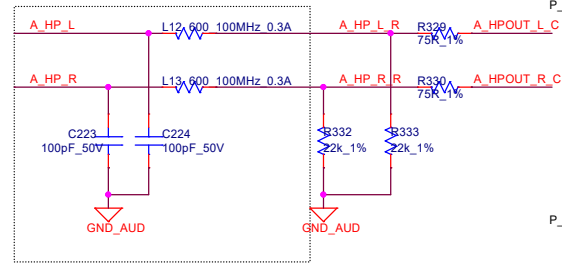


NC Interface 2 of 2

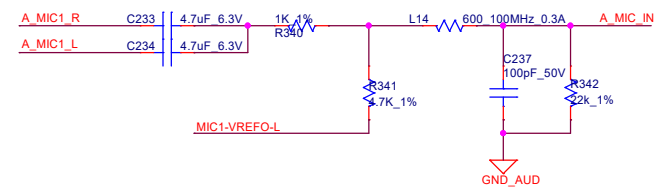
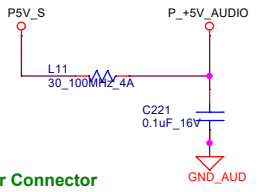




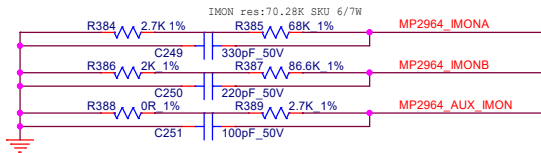
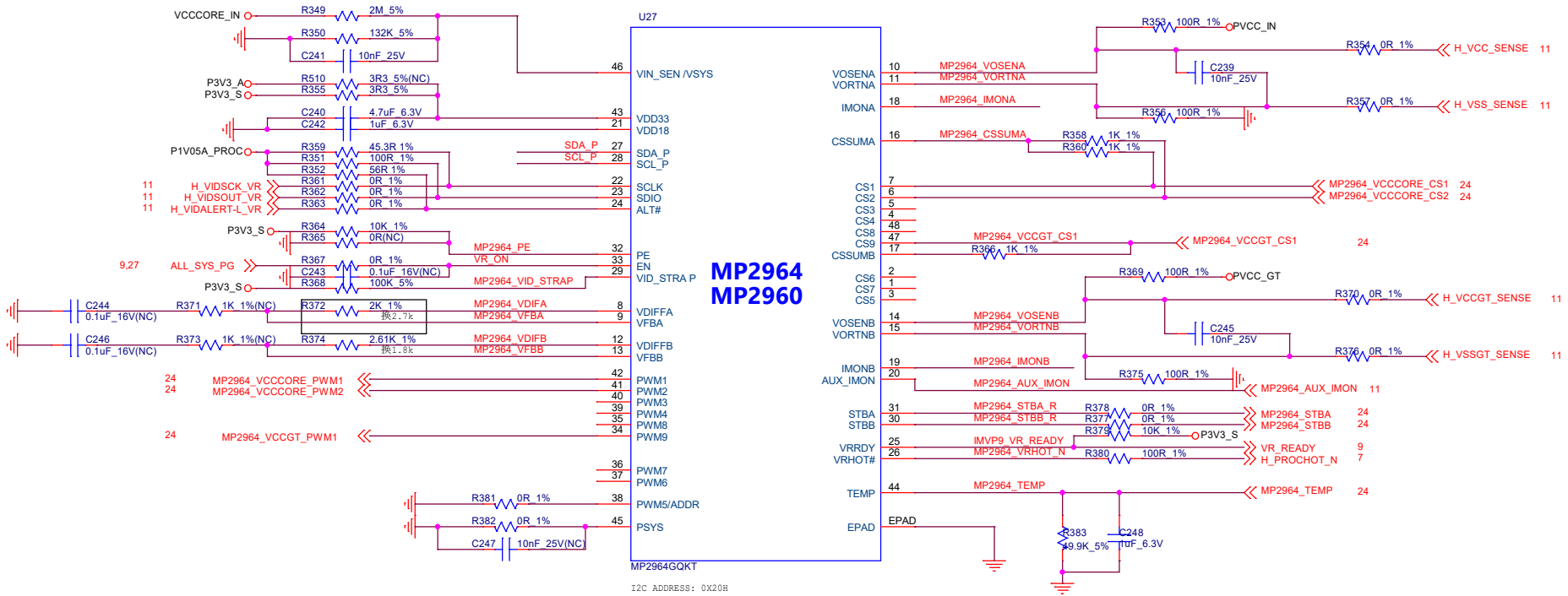
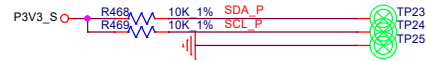
Near Connector



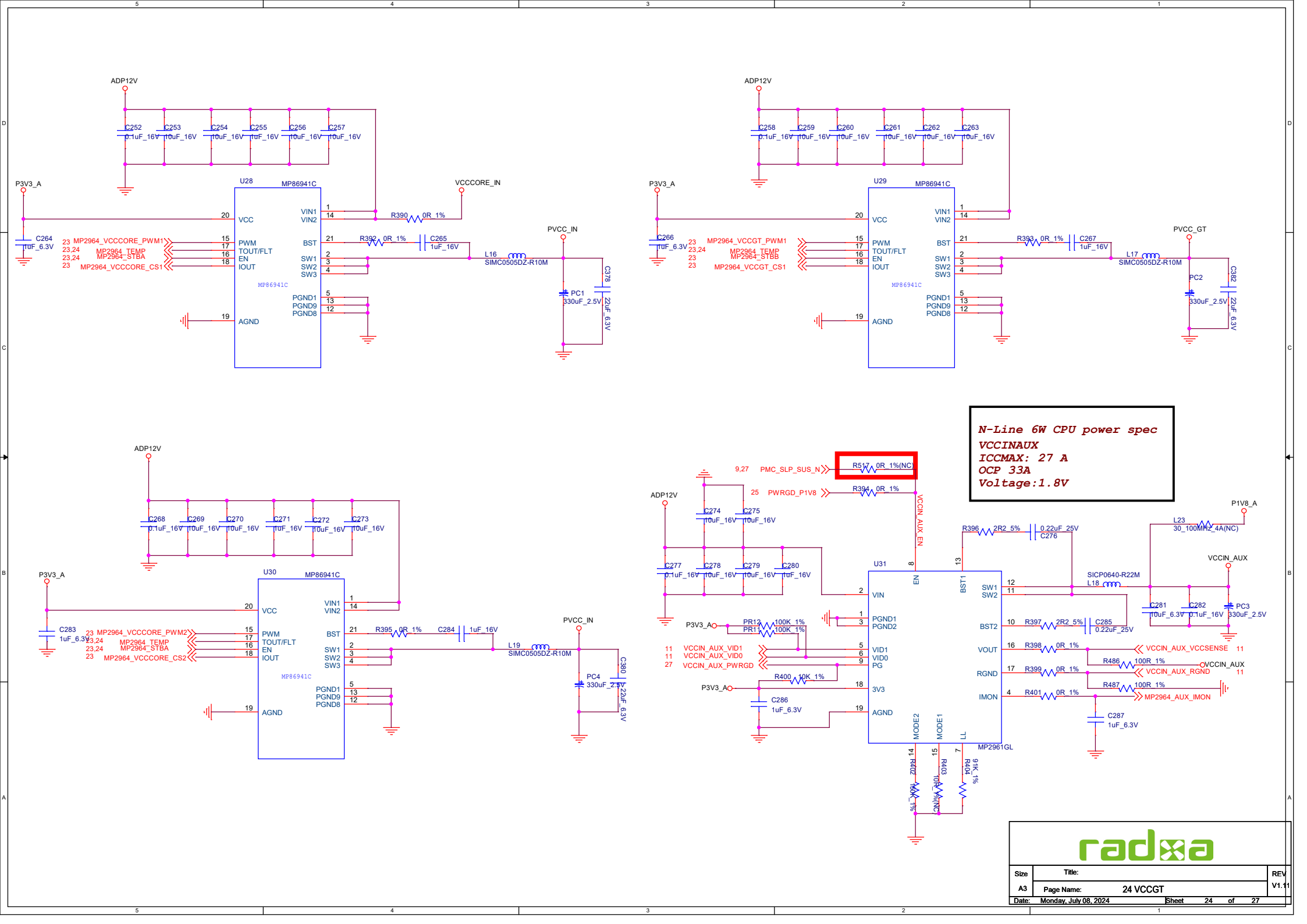
Near Connector



RAIL	RES	CAP	ICCMAX
VCCCORE	70.28K	330PF	37A
	53.97K	330PF	53A
VCCGT	82.75K	220PF	29A
VCCIN_AUX	11K	220PF	27A



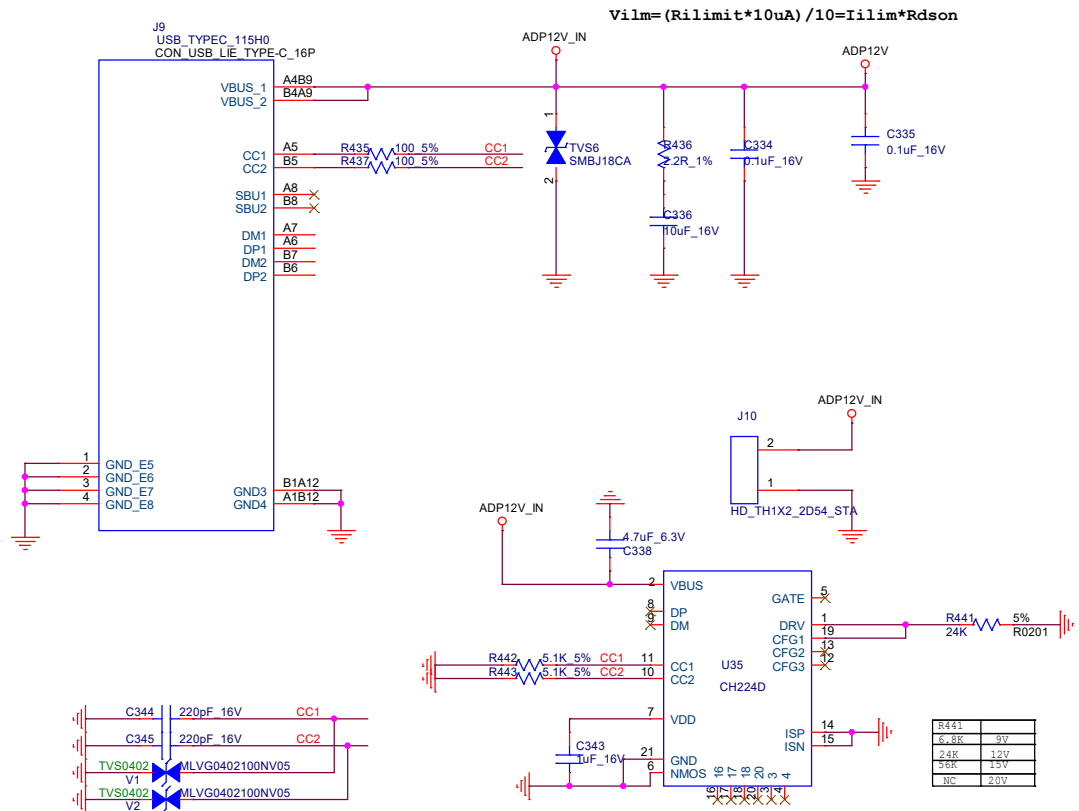
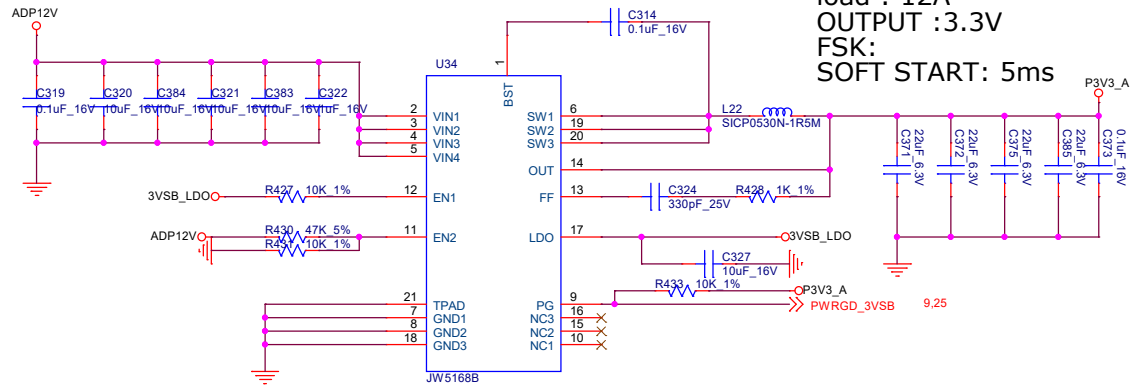
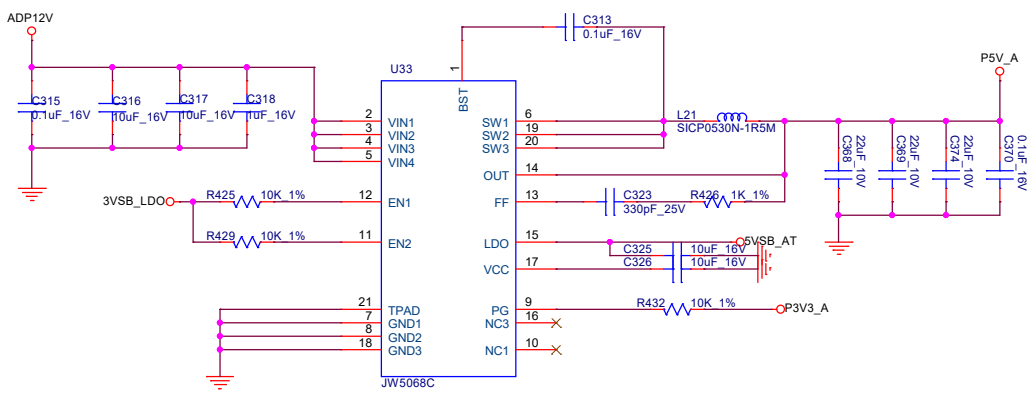




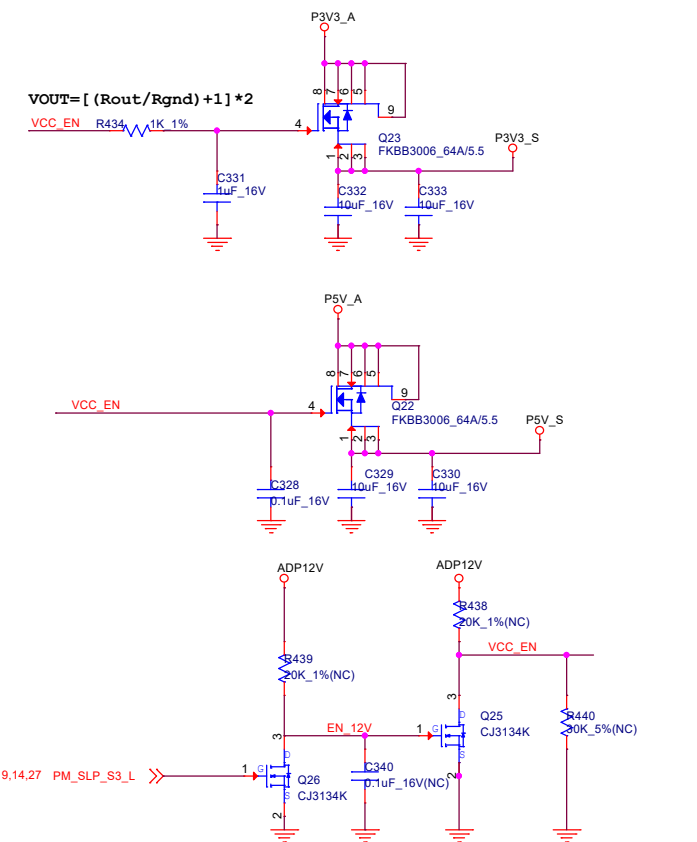
**N-Line 6W CPU power spec**  
**VCCINAUX**  
**ICCMAX: 27 A**  
**OCP 33A**  
**Voltage: 1.8V**



OCP : 19A  
 load : 12A  
 OUTPUT : 3.3V  
 FSK :  
 SOFT START: 5ms



$$V_{OUT} = [(R_{out}/R_{gnd}) + 1] * 2$$



Size	Title:	REV
A3	Page Name: 26 DC POWER	V1.11
Date: Monday, July 08, 2024	Sheet 26 of 27	

